Single-Switch DC-DC Converter With Fault-Tolerant Capability Under Open- and Short-Circuit Switch Failures

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***Abstract*—This paper proposes fault tolerant operation of single switch DC-DC converter under switch failure. In order to improve the reliability in critical applications, fault tolerant operation is mandatory to guarantee service continuity. Fault tolerant operation of a power system can be performed in three steps: fault diagnosis (detection and identification) and remedial actions.**

In the case of a switch failure, suitable fault detection is essential to avoid its propagation to the whole system. This study is based on a fast and efficient open and short circuit switch fault diagnosis. Both types of switch failure can be detected, identified and handled in real time by implementing fault diagnosis and reconfiguration strategies on a $FPGA$ target. No additional sensor is required to perform the fault detection. A redundant switch and a bidirectional switch are needed for converter reconfiguration in post-fault operation. The results of Hardware-In-the-Loop (HIL) and experimental tests, which all confirm the good performances of the proposed approach, are presented and discussed.

***Index Terms*—DC-DC Converter, Switch Failure, Fault Tolerance, Diagnosis, Hardware in the Loop.**

I. Introduction

NOWADAYS, DC-DC converters are widely used in many industrial applications such as aerospace, ships, electric vehicles and renewable energy power systems [1], [2]. Moreover, reliability in such embedded systems and in safety critical applications has been improved with the integration of fault diagnosis and fault tolerant architectures. Fault tolerance in a power converter requires three steps: fault detection, fault identification (also known as "fault diagnosis") and remedial actions [3]. The two first steps are used to identify the location and nature of the fault. The remedial actions are the process to first isolate the faulty device, if needed, and then reconfigure the converter to guarantee the service continuity.

The two most critical elements in DC-DC converters are aluminum electrolytic capacitors and semiconductors. More than 50% of malfunctions and breakdowns are reported to be due to aluminum electrolytic capacitor failures [4] and 34% due to semiconductor failure and soldering joints failure in power devices [5] and [6].

This contribution focuses on fault tolerance in single switch DC-DC converters under Open Circuit Fault (OCF) or Short Circuit Fault (SCF) on the semiconductor switch.

Several papers have proposed switch fault detection methods in power electronic converters and fault tolerant converter topologies. Switch fault diagnosis with fault-tolerant schemes for isolated phase-shifted full-bridge (PSFB) DC-DC converters are presented in [7] and [8]. For an OCF in [7] the primary voltage of the transformer is used as the diagnosis criterion, which has been obtained by adding an auxiliary winding. In [8], the DC-link current and transformer primary voltage, combined with switch gate-driver signal, are treated as diagnosis criteria to detect the switch SCF. The reconfiguration strategies are also predicted for the post-fault operation. In [9], an OCF detection method based on comparison of the duty cycle with the inductor current slope is proposed for Hybrid Electric Vehicles (HEV). Besides, a multi-mode bi-directional DC-DC converter is used for fault compensation. In [10], a fast FPGA-based switch fault (OCF and SCF) detection method for single-ended non-isolated DC-DC converters is studied. In this paper, the inductor current slope is used as fault diagnosis criterion; no additional sensor is required and the failure can be detected in less than two switching periods. In [11], a fault tolerant H-bridge DC-DC converter based on redundancy is discussed. For post-fault operation, a new control strategy, an extra leg and a bidirectional selector switch are added to the original converter. A fault diagnosis method of PWM DC-DC converters by using the magnetic component voltage is presented in [12] . In this method an auxiliary winding in the magnetic core is used to measure the inductor voltage. In [13] , an alternative OCF diagnosis method for boost interleaved DC-DC converters operating in unidirectional power flow is studied. This method is based on features of the DC-link current derivative sign during fault and healthy operations [13]. An OCF diagnosis and fault-tolerant scheme for a three-level boost converter in a PV power system is presented in [14] . The control variables used for maximum power point tracking and output DC-link capacitor voltage balance are treated to fault diagnosis. By adding a few components to the original converter, it can be partly reconfigured into a two-level boost converter for post-fault operation. A MOSFET faults diagnosis

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based on the integral and peak values of the DC-link current for a zero voltage-switching DC-DC converter is proposed in [15]. It should be noticed that the fault detection methods cited in references [7]–[15] can generally detect only one type of fault (OCF or SCF). Among them, the methods in [8] and [12] are as fast as the one proposed in this paper, while in [12] an analog circuit is used to fault detection.

This paper is started from our previous research, firstly introduced in a precedent introductory paper [10]. The initial Fault Detection Algorithm (FDA) is improved in term of fault diagnosis (OCF or SCF); moreover, remedial actions, such as converter reconfiguration for post-fault operation, are also treated in this contribution.

The new proposed FDA is capable to identify the type of the failure which is mandatory for fault isolation and converter reconfiguration in post fault operation. To guarantee the service continuity, a Fault Tolerant (FT) DC-DC converter topology based on redundancy is then considered. According to the type of the failure (OCF or SCF), two different strategies for system reconfiguration are proposed. This study is particularly dedicated to single switch DC-DC converters. Fig.1 summarizes this family which consists on buck, boost, buck-boost, Cuk, SEPIC, and dual SEPIC converters.

As shown in Fig.1, in these converters, the inductor current (i) behaviour is the same. Because of this similarity, the proposed fault detection method is applied to the particular case of a boost converter. Nevertheless without losing generality, this method can be applied to any other topology. In the following sections, the proposed FDA and FT converter topology are presented; some HIL simulations and experimental results are provided. Both HIL and experimental results confirm the effectiveness of the proposed FDA and FT topology. It is shown that by using this fault detection method, both types of switch failure can be detected and discriminated. Then, two different reconfiguration strategies have been successfully performed. Thanks to $FPGA$ implementation, these actions may be performed in less than one switching period. This minimal needed time is due to the natural delays in the system. One can notice that, in the worst case, two switching periods are needed (in case of OCF). In case of SCF, the system reconfiguration will be done after the fault clearance time.

II. FAULT DIAGNOSIS

The fault diagnosis method proposed in this paper can detect both OCF and SCF and also announces the type of the fault which is mandatory for converter reconfiguration. This new FDA is based on two algorithms which use the switch command signal (switch gate-driver signals) and the sign of the inductor current slope to detect the switch failure. The primary algorithm $FDA1$ is faster than the secondary one $FDA2$ but is less robust for detecting in critical values of duty cycle d (small d in OCF or large d in SCF) or in high switching frequencies. The secondary algorithm is more robust: it efficiently detects faults in any conditions, but it is not as fast as $FDA1$. Both algorithms work on parallel to detect switch failure. It can be said that $FDA2$ is used when the fault could not be detected by $FDA1$ in less than two switching periods. The proposed algorithms are described in the following.

A. Primary algorithm ($FDA1$)

As shown in Fig.2, when the switch SW is turned on, the diode is reverse biased and is off. During $d.T_{sw}$, the input voltage (v_i) is applied across the inductor, where T_{sw} is the switching period and d is the duty cycle. Consequently, the inductor current i ramps up linearly (ignoring the effect of inductor resistor) increasing the energy stored in the inductor. During this cycle (so called cycle1) d (the switch command) is equal to '1'.

When the switch SW is turned off (during $(1-d)T_{sw}$), the stored energy in the inductor flows to the load and forces the diode to conduct. As a result the inductor current i decreases. During this cycle (so called cycle2) d is equal to '0'.

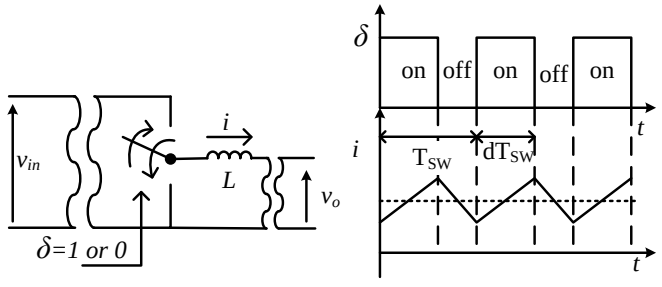

Fig. 1. Single switch DC-DC converters principal scheme.

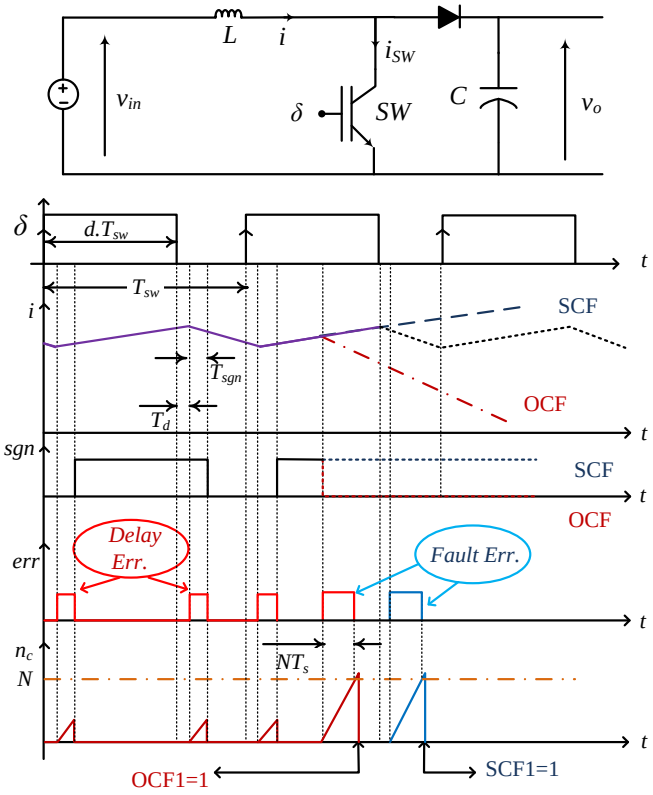

Fig. 2. Principle of $FDA1$ algorithm for a boost converter.

Fig. 3 presents the general scheme of the primary algorithm ($FDA1$). This algorithm needs the slope of the inductor current ('sgn' signal). In order to avoid a more complex algorithm, the exact value of the derivative of the inductor current is not used in this study. The 'sgn' signal is obtained by comparing the value of $i(t)$ with its value at T_{sgn} before, i.e. $i(t - T_{sgn})$, as follows:

$$\begin{cases} \Delta i = i(t) - i(t - T_{sgn}) > 0 => sgn = 1 \\ \Delta i = i(t) - i(t - T_{sgn}) < 0 => sgn = 0 \end{cases} \quad (1)$$

T_{sgn} should be chosen by considering some parameters of the setup, such as ADC precision versus conversion time and used sampling period, and then validated by some experimental tests. In our case, it is fixed at $4T_s$ (T_s is the sampling period).

In ideal conditions, when there is no switch failure, the two signals ('sgn' and 'd') have the same value; thus the signal 'err' is equal to '0', as described in (2). When a failure is occurred, the conditions (2) cannot be satisfied, thus 'err' will be equal to '1'.

$$\left.\begin{cases} \Delta i > 0 => sgn = 1 \\ \delta = 1 \end{cases} \right\} \Rightarrow err = sgn \oplus \delta \quad (2)$$
$$\left.\begin{cases} \Delta i < 0 => sgn = 0 \\ \delta = 0 \end{cases} \right\}$$

It should be noted that, as a result of non-ideal behaviour of power switches, delays and dead times are inevitable. Therefore, as shown in Fig. 2, even in a healthy operation of the converter, the error signal will be momentarily unequal to zero. That is why a time criterion is employed to take into account for these delays and dead times.

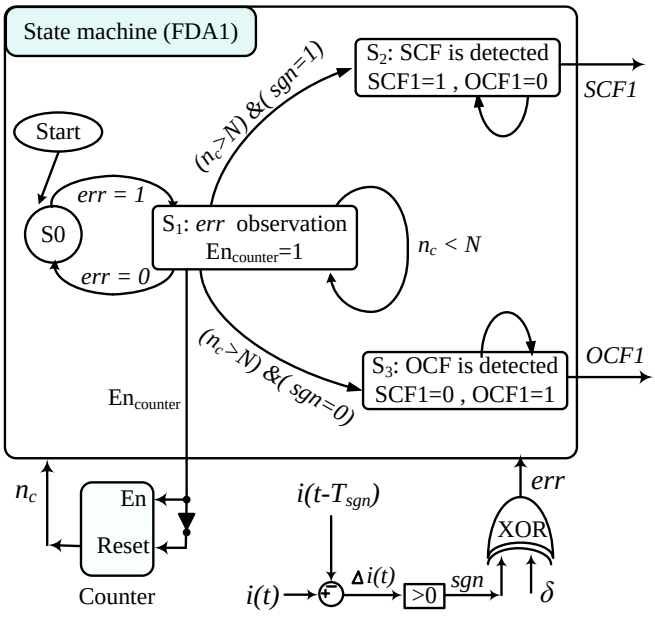

Fig. 3. Primary fault detection algorithm ($FDA1$).

Let us now detail the state machine of $FDA1$ (Fig. 3). This machine has four states starting from $S0$. The machine stays in $S0$ as far as the signal 'err' is '0'. When 'err' passes to '1', a transition to $S1$ occurs. In this state, the signal 'Encounter' is activated and the counter starts to increase 'n_c' (counter's output). In state $S1$ the signal 'err' is observed and if it always remains in state '1' for a long enough time, more than observation periods equal to NT_s , i.e. $n_c > N$, then it is concluded that there is a fault. According to the value of 'err' and 'sgn', three transitions can occur:

1) If 'err' resets to '0' after some sampling periods ($n_c < N$), the state machine returns to S0 and the counter is reset.
2) In the case of a SCF, i increases regardless of the switch command ($\Delta i(t) > 0$ and 'sgn'$= 1$) and then 'err' stays in '1' for a few sampling periods. When n_c becomes bigger than N, a transition to $S2$ occurs; $SCF1$ goes to '1' and SCF is declared.
3) Under OCF condition, i decreases disregarding of the switch command ($\Delta i(t) < 0$ and 'sgn'$= 0$). As a result 'err' remains in '1' for a long enough time ($n_c > N$). Then a transition to $S3$ occurs; $OCF1$ goes to '1' and OCF is declared.

The mentioned observation time (NT_s) should be longer than the overall delays caused by the sensors, drivers, controllers and switches ($NT_s > T_d$); otherwise the inherent but normal delay of the system may be interpreted as a fault (Fig. 2).

The $FDA1$ is very fast and detects a fault after its occurrence within N sampling periods. However, the fault detection time in $FDA1$ depends on several parameters such as duty cycle (d) and switching frequency. For example, for an OCF, it may be seen that with small values of d ($dT_{sw} \leq NT_s$) or in high switching frequency cases, fault detection with $FDA1$ may not be possible. In these cases, the time period during which the 'err' signal is equal to '1' is always shorter than the observation time (NT_s). Therefore the counter nc could not reach the predefined value of N and then the fault cannot be detected. For a SCF, with large value of d or small T_{sw}, the fault cannot be also detected by $FDA1$. For these reasons, a secondary algorithm ($FDA2$) is proposed (Fig. 4).

B. Secondary Algorithm ($FDA2$)

As described before, there are two cycles (cycle1 and cycle2) per period for a conventional boost converter. In cycle1, the inductor current increases while in cycle2, it decreases. According to Fig. 5, the inductor current i increases and then decreases during one healthy switching period. Therefore, if i is always increasing or decreasing in a switching period, it can be concluded that a failure has occurred. This detection is computed by using a '$Trig$' signal providing a pulse on each positive front of the command signal, corresponding to the beginning of the switching period (Fig. 5).

As shown in Fig. 4 , for fault diagnosis by $FDA2$, a state machine with five states is used. In initial state $S0$, the converter is in cycle2 of operation, i.e. $\delta = 0$, and stays in this state until '$Trig$' passes to '1' and then a transition to state

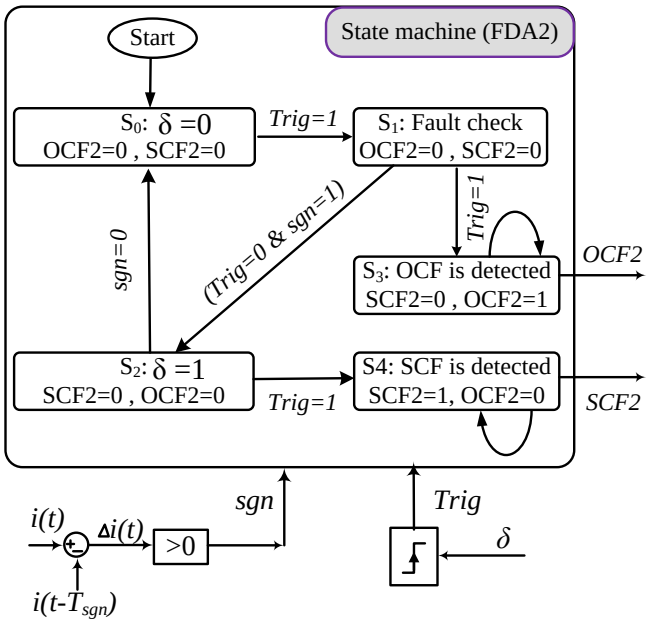

Fig. 4. Secondary fault detection algorithm ($FDA2$).

$S1$ occurs. In state $S1$, according to the converter conditions, two transitions can occur:

1) If no failure has happened, the switch SW is turned on, i increases and 'sgn' goes to '1', thus a transition to state $S2$ occurs.
2) In the case of an OCF, i decreases and 'sgn' becomes '0'. The conditions for the transition from $S1$ to state $S2$ are not satisfied. The system remains in $S1$ until the next '$Trig$' pulse, and then a transition to $S3$ occurs: the $OCF2$ is set to '1' and the fault is declared.

The state $S2$ corresponds to cycle1 of operation, i.e. $\delta = 1$. In this state two transitions are possible:

1) In healthy conditions, the system stays in $S2$, and when 'δ' becomes '0', i decreases and 'sgn' passes to '0', then a transition to $S0$ occurs.
2) In SCF condition, when 'δ' passes to '0', the switch cannot be turned off; no transition occurs to $S0$ until the next '$Trig$' pulse, and then a transition to $S4$ occurs: the $SCF2$ is set to '1' and the fault is declared.

$FDA2$ is slower than the primary algorithm ($FDA1$) but can detect the faults in any conditions, for any 'd' and any switching frequency.

Fig. 6 shows the general scheme of the fault detection algorithm; the general FD (Fault Detection) signal is set to '1' when one of the algorithms ($FDA1$ or $FDA2$) detects a fault.

As described in this section, the proposed fault detection algorithm can detect and identify OCFs as well as SCFs very quickly, without adding any extra current or voltage sensors in the DC-DC converter. This is interesting because additional sensors affect the reliability, cost and weight.

In the following sections, this fault diagnosis method will be used to detect and identify switch failures in a fault tolerant DC-DC converter topology.

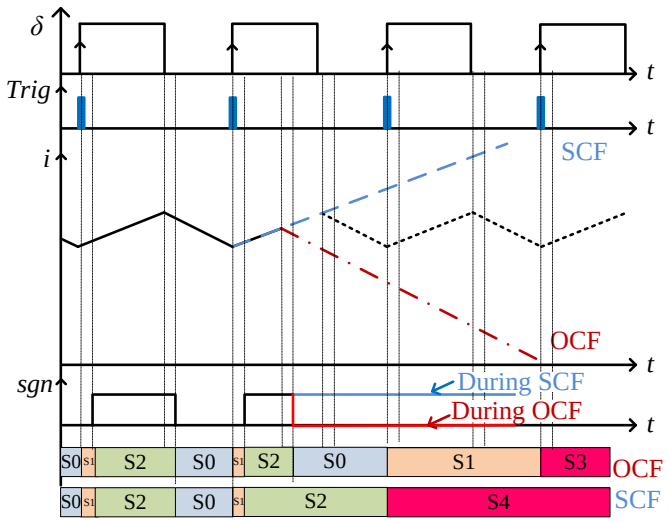

Fig. 5. $FDA2$ signals and states.

III. FAULT TOLERANT OPERATION

A. Fault tolerant converter topology

To ensure service continuity of the studied DC-DC converter for post-fault operation, a fault tolerant topology is proposed (Fig. 7). After fault detection and isolation, the faulty switch (SW) will be replaced by SW_R via a bidirectional switch T (a Triac in this study). Then, the converter can operate in normal conditions, not in degraded mode but without redundancy [3]. Note that, this fault tolerant topology is particularly cost optimized for the systems with multiple parallel converters connected to a common bus (Fig. 8).

This fault tolerant topology can be used in a multi-source power system where the sources are connected to a DC common bus through DC-DC converters [16] . An example for this system is given in Fig. 8. In this case, for each converter, a fault detection block (as in Fig. 6) must be considered. Each block observes the signals i_k and switch command δ_k, $k = 1, 2, \ldots n$ of the concerned converter. When a fault is occurred in the converter k, the fault detection block detects and identifies the failure. Then, by using the chosen converter reconfiguration strategy, the faulty switch (SW_k) can be replaced by the redundant switch (SW_R) via the bidirectional switch T_k. The proposed fault detection

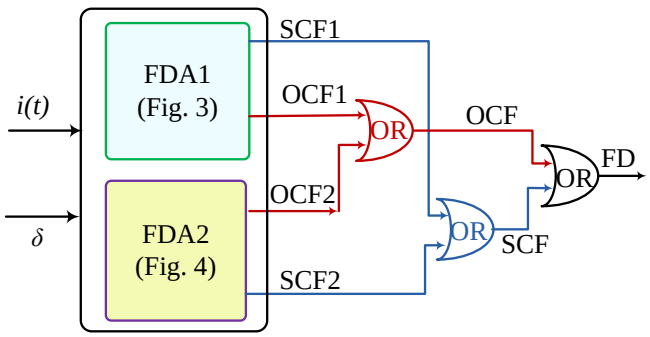

Fig. 6. Fault detection block.

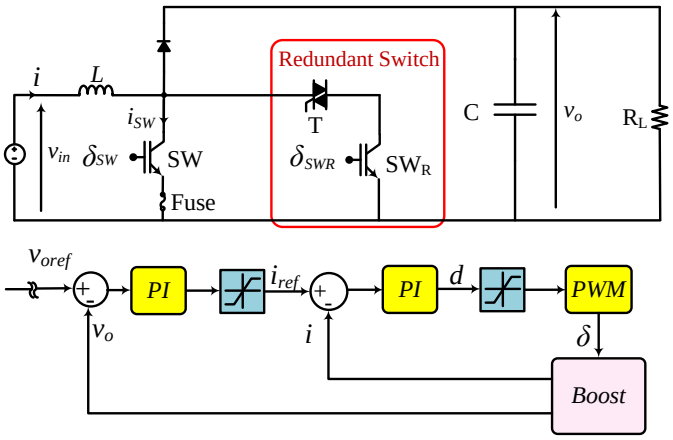

Fig. 7. Fault tolerant converter with redundant switch and the control loops.

method does depend on neither the type of converter (in single switch DC-DC converters) nor the number of converters in parallel in the system. This fault tolerant topology can be also used in modular DC-DC converters [17] and [18] . The proposed topology requires k bidirectional switches and only one redundant switch for the whole system. Also no additional sensors are needed. According to the type of switch failure, different reconfiguration strategies are used which are explained in the following.

B. Fault isolating and reconfiguration

As mentioned before, the second step in fault tolerant systems consists on fault isolating and system reconfiguration. According to the type of the switch failure (OCF or SCF), this step might be differently applied to the system. The studied FT converter with its control loops have been shown in Fig. 7. If an OCF occurs on the switch SW, after fault identification by FDA block, the faulty switch can be immediately replaced by the redundant switch SW_R via the bidirectional switch T. But, in case of SCF on SW, as far as the SCF is present on the switch, SW cannot be replaced by the redundant switch.

In fact, in case of SCF, after fault detection, first the faulty switch should be isolated by means of fuse protection [19]. To reconfigure the converter, FT algorithm observes the current i_{sw} (switch current in Fig. 7) indirectly through the sign of the 'sgn' signal. When i_{sw} becomes zero this means that the faulty switch is removed by the fuse. To avoid adding a new current sensor per boost in the system, i_{sw} is observed indirectly. In case of a SCF, the inductance current (i) increases during the presence of the fault, then the sign of current slope ('sgn') is equal to '1'. After fuse breaking, the switch SW is disconnected from the converter and i_{sw} becomes zero. The inductor current (i) passes through the diode and starts decreasing, thus 'sgn' will be '0'. At this time the faulty switch can be replaced by SW_R.

The reconfiguration strategy is shown in Fig. 9. According to this figure, the redundant switch can replace the faulty switch when the signal FT is '1' and then the converter's service continuity is guaranteed.

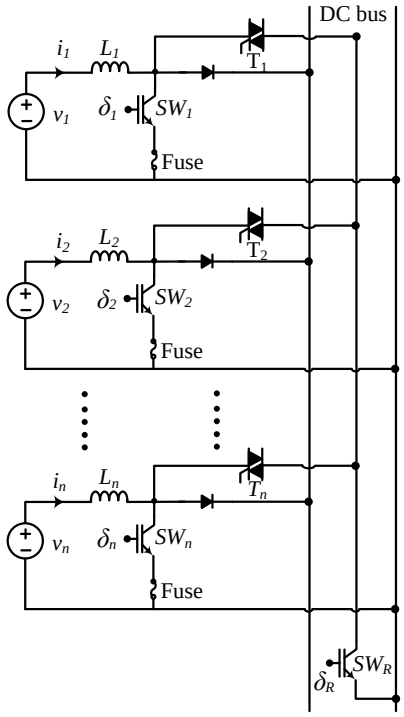

Fig. 8. Multi-converter system with redundant switch.

IV. FAULT-TOLERANT AND CONTROL IMPLEMENTATION ON A $FPGA$ CHIP

The traditional model-based simulation has the disadvantage of being unable to exactly replicate real operational conditions. It does not take into account the limitations of the digital controller, like saturation of values in fixed point format during the intermediate calculations and the finite resolution of registers. Also, the fully experimental tests may not be always possible or may lead to serious system damage, particularly when fault tolerant operation is tested. One interesting solution to test the digital controller in a realistic manner is Hardware-In-the-Loop (HIL) analysis. It reduces design time and allows control algorithm and power converter development avoiding the risk of damaging of the real prototype [20] and [21]. It is especially interesting for testing fault tolerant systems. In this paper a design methodology based on $FPGA$ rapid prototyping so called "$FPGA$ in the loop", is used to test experimentally the proposed fault tolerant operation. In this method, the controller and fault tolerant algorithm are implemented in only one $FPGA$. In order to carry out the $FPGA$

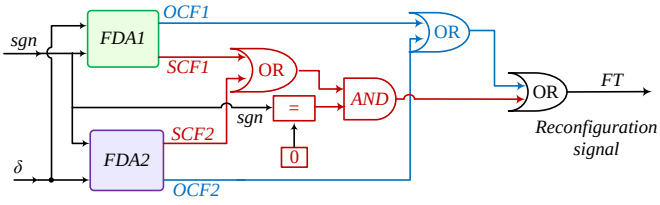

Fig. 9. Reconfiguration strategy.

implementation for HIL experiments, three following steps are considered.

A. Functional simulation

The first step is the functional simulation. In this stage, the power circuit (plant) and the sensors are modelled using Matlab/SimPowerSystems. The interfaces and controllers are done using Simulink toolbox. The studied system is first modelled in continuous-time and then in discrete-time mode [21].

B. Mixed simulation

After having checked and validated the system by functional simulation, it must be modelled with binary synthesizable format. In this step, the Simulink blocks are removed and replaced by proper DSP Builder blocks, in the same Simulink environment. This software integrates HDL (Hardware Description Language) development tools by combining the algorithm development, simulation and verification capabilities of the Matlab/Simulink system-level design tools with the $VHDL$ (Very high speed integrated circuits Hardware Description Language) design flow including Quartus II (Altera) software. Quartus II software provides a comprehensive design, synthesis, and analysis environment for PLDs (Programmable Logic Devices) applications. DSP Builder allows creating the hardware representation of the required digital signal processing functions using Matlab/Simulink user-friendly algorithm-development environments, for shorter design and implementation cycles. Matlab functions and native Simulink blocks can be combined with DSP Builder library blocks to create $FPGA$ designs which can be simulated under Simulink. It should be noted that some complex functions and Simulink blocks do not have corresponding blocks in the DSP Builder library. As a result, these functions or blocks should be constructed from the basic blocks or imported using HDL programming. The power part of the system is remained unchanged in this step, modelled by using SimPowerSystems blocks. Appropriate DSP Builder input and output blocks are necessary to convert the Simulink signals in fixed point signals for DSP Builder [21].

C. HIL simulation

The final step is dedicated to the hardware implementation, the verification and the validation of the digital control algorithm in a HIL-based reconfigurable platform. To achieve these objectives, the digital controller, modelled by DSP Builder blocks, are translated into a synthesizable $VHDL$ model. This is done by using the Signal Compiler block available in DSP Builder library. After the generation of the $VHDL$ files, a single HIL block replaces all DSP Builder blocks. Then, the HIL block is compiled to provide for a programming object file which will be used for HIL simulation. Finally the development board that contains the $FPGA$ can be programmed and used in the HIL simulation.

The development board is linked to a PC via a Joint Test Action Group ($JTAG$) connection. This interface performs communication between the digital control algorithm (implemented in $FPGA$) and the plant (emulated by the PC with Matlab/SimPowerSystems). In the proposed HIL-based reconfigurable platform, at each time-step, the plant model is simulated using Matlab/SimPowerSystems and then the output signals are exported to the $FPGA$ placed in the development board. When the $FPGA$ receives signals from Simulink, it executes the implemented program for one sample interval. The $FPGA$ returns control signals, computed during this step, to Simulink. At this point, one sample cycle is performed.

If the results obtained from the HIL simulation are not correct or the goals are not met, the mixed simulation and the HIL simulation steps must be performed again with the modified digital controller model. Fig. 10 shows the "$FPGA$ in the loop" prototyping. The $FPGA$ implementation procedure is based on a methodology for rapid prototyping, detailed in [21]. In our case, a $Stratix\ DSP\ S80$ development board is used, which includes the $Stratix\ EP1S80B956C6\ FPGA$ chip. Results of functional and mixed simulations are verified before HIL simulation, but in this paper only the results of HIL and experimental tests are presented. They are commented in the following.

V. HARDWARE-IN-THE-LOOP RESULTS

For HIL experimentation, the converter given in Fig. 7 is considered. The controller and fault tolerant schemes are implemented on the same $FPGA$ chip and the power system is modelled in MATLAB/Simulink environment using the SimPowerSystems toolbox. The system parameters are given in TABLE I, which are the same as in the experimental bench.

HIL scenarios consider the converter operating in normal conditions before the occurrence of a switch fault. The FDA detects the failure very quickly and the converter can follow to operate in normal conditions after being reconfigured.

First, the validity of the fault tolerant operation in case of an OCF is verified. Fig. 11 shows fault detection and converter reconfiguration when $FDA1$ detects the fault. In this case the

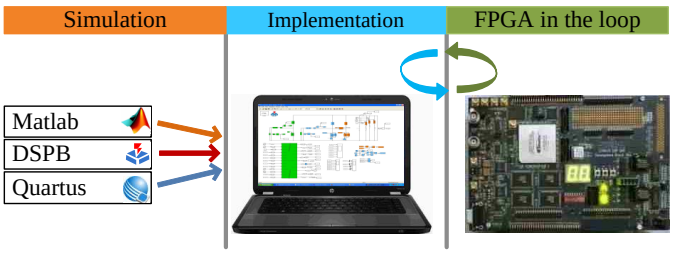

Fig. 10. FPGA in loop prototyping.

TABLE I
PARAMETERS OF THE STUDIED SYSTEM

L	$9mH$
C	$1100\mu F$
R_L	75Ω
V_{out}	$150V$

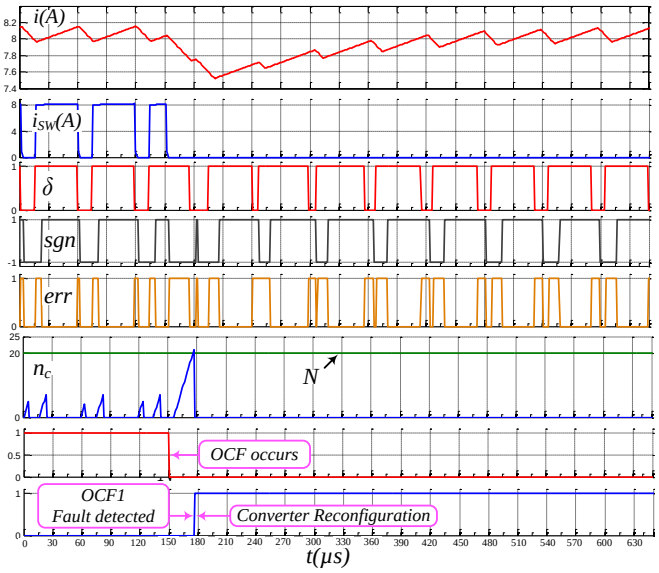

Fig. 11. OCF detection by $FDA1$ and reconfiguration when d is large ($V_{in} = 30V, V_o = 150V, d = 80\%$).

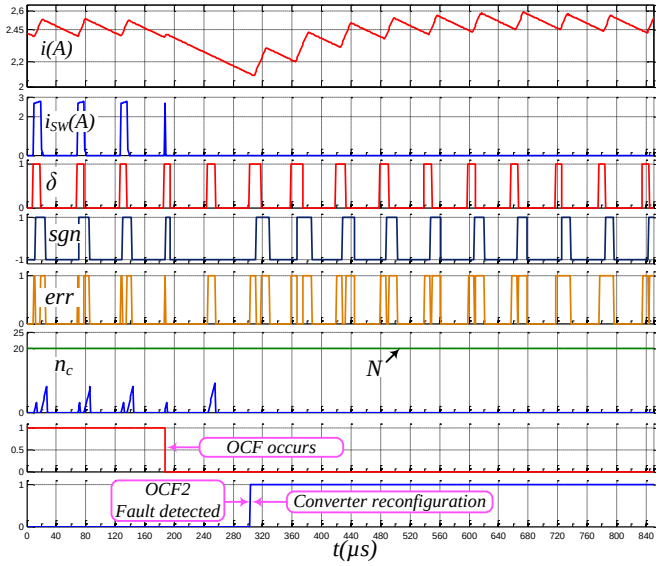

Fig. 12. OCF detection by $FDA2$ and reconfiguration when d is small ($V_{in} = 120V, V_o = 150V, d = 20\%$).

duty cycle (d) is large enough, and then $FDA1$ can detect the failure in 23 μs after fault occurrence. The redundant switch takes the place of the faulty switch, immediately after fault detection.

Fig. 12 shows the HIL results for an OCF when d is small. The fault is detected by $FDA2$ after two switching periods and then fault tolerant operation is performed successfully by converter reconfiguration.

Fig. 13 presents the HIL results for a SCF when d is around 50%. In this case, the fault is detected in one switching period, but the converter reconfiguration is performed after fuse breaking (500 μs after fault occurrence in this study which stands for fuse breaking time). When i_{sw} and 'sgn' become zero the faulty switch is replaced by the redundant

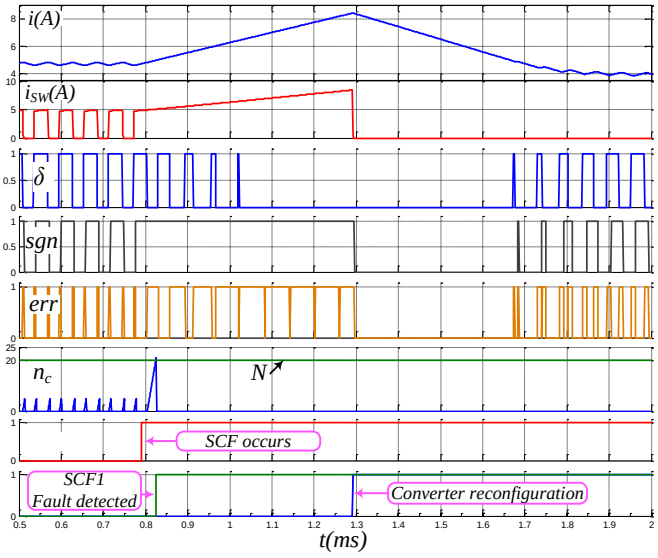

Fig. 13. SCF detection by $FDA1$ and reconfiguration when $d = 50\%(V_{in} = 75V, V_o = 150V)$.

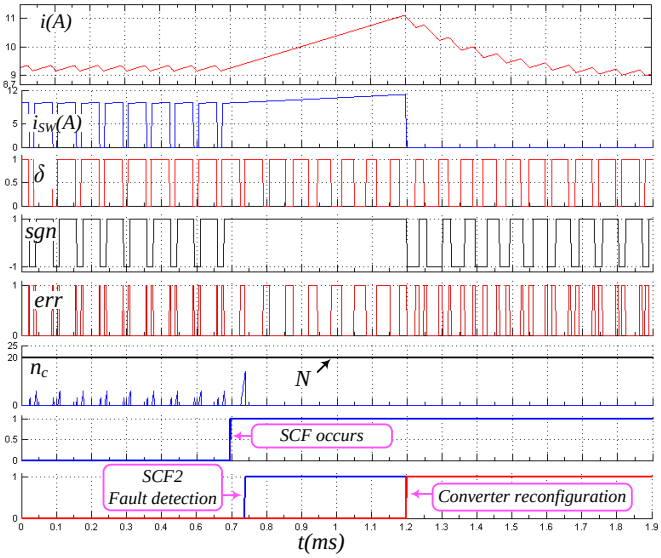

Fig. 14. OCF detection by $FDA2$ and reconfiguration when d is large ($V_{in} = 30V, V_o = 150V, d = 80\%$).

switch.

Fig. 14 presents the HIL results in case of SCF when d is large. The failure is detected by $FDA2$ in the following switching period, but the reconfiguration is done after the fuse action.

The obtained HIL results confirm that the fault detection method can detect both SCF and OCF, also the service continuity of the converter is guaranteed by the fault tolerant operation.

VI. EXPERIMENTAL RESULTS

Experimental tests are carried out, based on a boost converter with a redundant switch, as depicted in Fig. 7. The experimental set-up is given in Fig. 15. It consists on a $Stratix\ DSP\ S80$ development board, an interface card, a

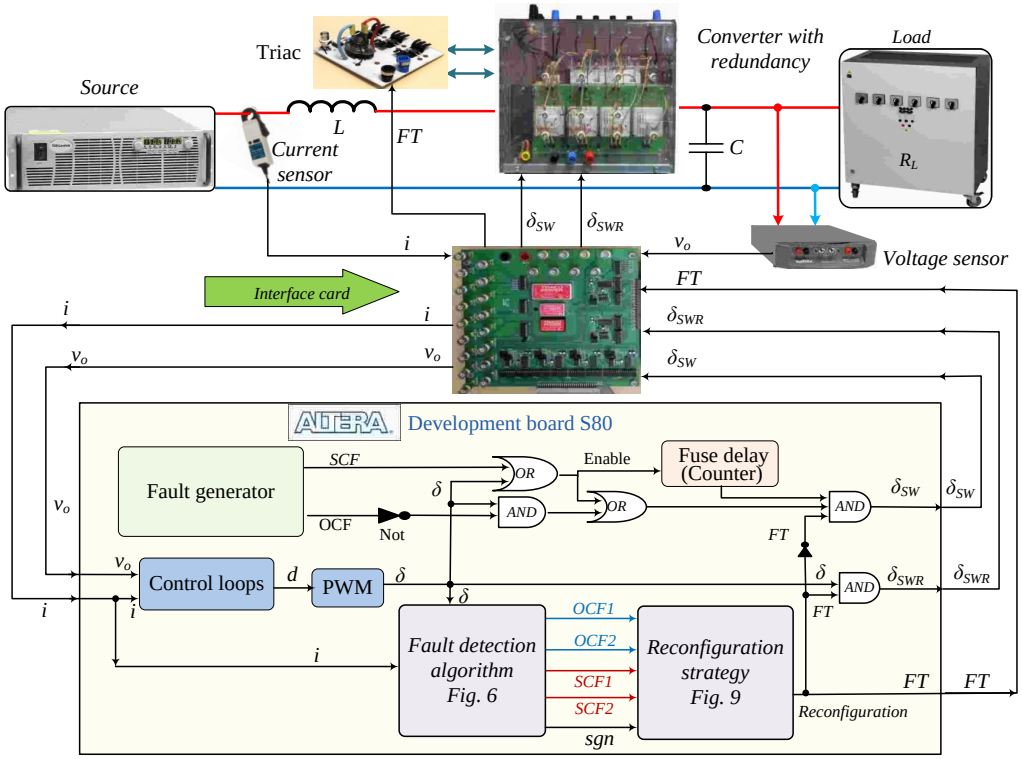

Fig. 15. Synoptic of experimental test bench.

resistive load and a programmable TDK source. The switches are $IGBT$s, $SEMIKRON\ SKM50GB123D$ devices.

The experimental results for an OCF with a duty cycle around 50% are shown in Fig. 16. The switch SW is kept opened by forcing 'δ' to '0' (Fault generator bloc Fig. 15). As Fig. 16 shows, in this test, OCF is occurred when the switch SW is off. When the switch is turned on, the current continues to decrease and then the fault is detected after 20 μs by $FDA1$ ($N = 20$).

Fig. 17 shows the results for an OCF with duty cycle around 13%. As mentioned previously, when d is small, $FDA2$ detects the fault successfully before $FDA1$, in less than two switching periods.

As shown in Figs. 16 and 17, after fault detection by one of the $FDA1$ or $FDA2$, the redundant switch SW_R takes the place of the faulty switch SW and the service continuity of the converter is guaranteed.

It should be noted that the laminated wiring of the converter supplied by $SEMIKRON$ does not allow to easily add a fuse in series with SW. In this study, SCF is "artificially" generated by means of the switch command δ_{SW} (applied switch command (δ_{SW}) different from δ produced by the control loop). Therefore, the fuse is emulated by means of $FPGA$ programming. For this, 500 μs after SCF generation, the switch command δ_{SW} which has been artificially set to '1' is reset to '0'. This reset to '0' imitates the fuse breaking time and therefore, the end of permanent switch short circuit. Fig. 18 shows the results for a switch SCF when d is around 50%. In this case, the fault is detected by $FDA1$ in less than one switching period. After 500 μs the SCF is removed and then the reconfiguration signal (FT) is activated. As illustrated in Fig. 18, reconfiguration is performed and the converter operates in the same conditions as pre-fault.

As mentioned before, in case of SCF when d is large $FDA1$ cannot detect the SCF successfully and $FDA2$ de-

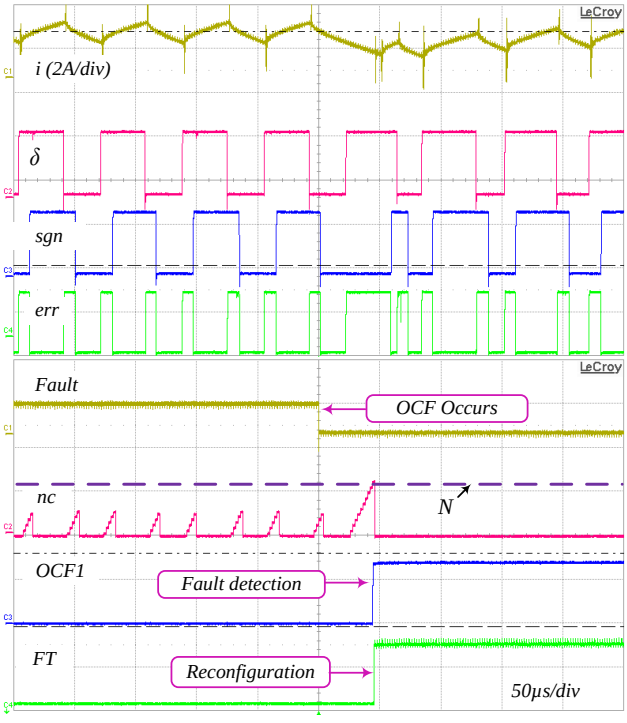

Fig. 16. OCF detection by $FDA1$ and reconfiguration when $d = 50\%$ ($V_{in} = 75V, V_o = 150V$).

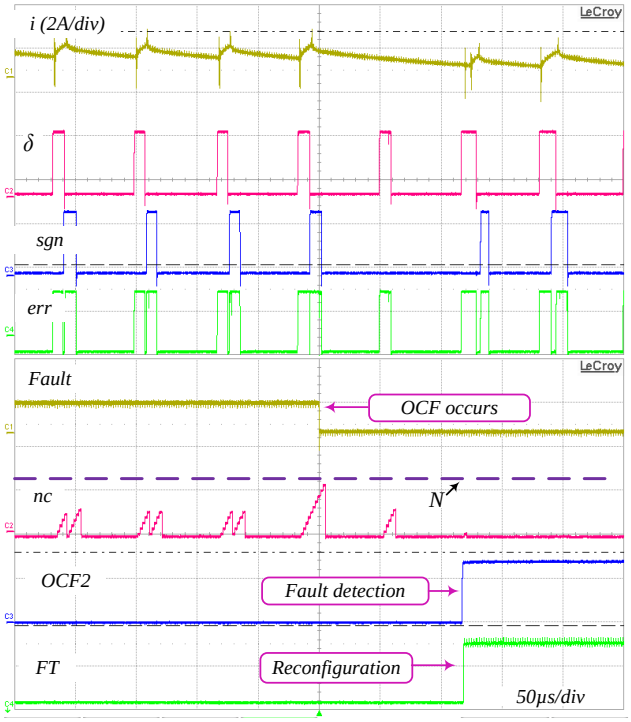

Fig. 17. OCF detection by $FDA2$ and reconfiguration when d is small ($V_{in} = 120V, V_o = 150V, d = 20\%$).

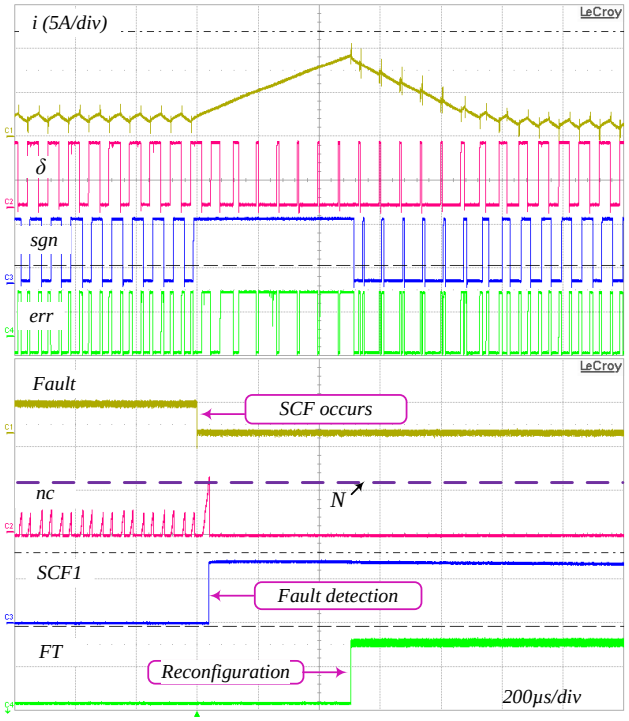

Fig. 18. SCF detection by $FDA1$ and reconfiguration when $d = 50\%(V_{in} = 75V, V_o = 150V)$.

tects the fault in less than one switching period. Fig. 19 shows the experimental results for this case. The SCF is detected in less than one switching period, but reconfiguration is done after the fuse action. The converter performs in normal conditions after being reconfigurated.

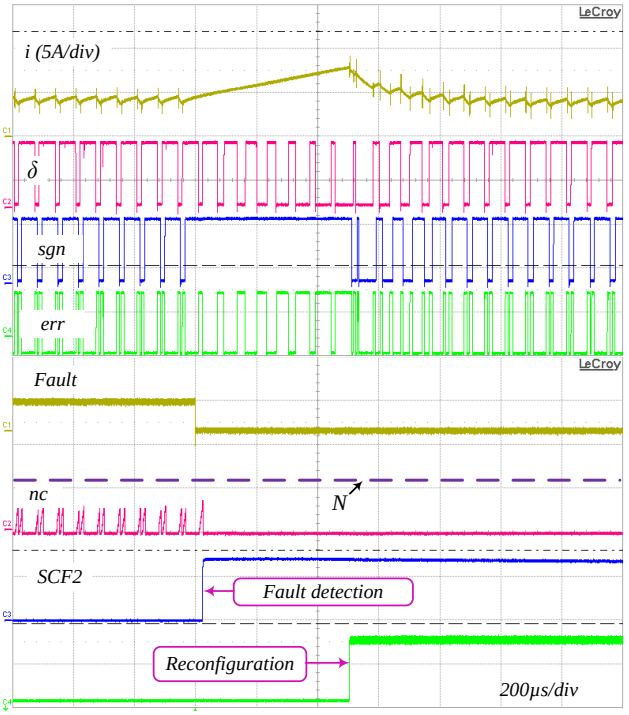

Fig. 19. SCF detection by $FDA2$ and reconfiguration when d is large ($V_{in} = 30V, V_o = 150V, d = 80\%$).

These results show that the proposed fault detection algorithm can always detect and identify open and short circuit faults correctly. In the worst conditions, the maximum detection time is equal to two switching periods. Also effectiveness of the fault tolerant topology is confirmed by these experimental tests. It should be remembered that in real systems, for the short circuit fault, the system reconfiguration will be realized after the reaction of the protection fuse (see Fig. 7).

It is noticeable that for any other type of the DC-DC converter, the proposed FDA can correctly detect switch faults but the FT topology might be adapted according to the converter architecture.

VII. CONCLUSION

This paper has proposed a fault tolerant operation of a single switch DC-DC converter based on a fast $FPGA$-based diagnosis method for open and short circuit switch failures.

In this contribution, the fault detection method first introduced in [10] is improved in order to be used in a fault tolerant topology. The proposed fault detection algorithm can identify and declare the type of the fault (OCF or SCF) which is not always proposed in similar methods. The inductor current and switch command are only used to detect the failures. The method is consisted of two subsystems which work in parallel: $FDA1$ which is fast and $FDA2$ which is robust. $FDA1$ directly compares the switch command and measured value of the sign of the inductor current's slope. $FDA2$ is based on the fact that in normal operation of the converter, during a switching period, with restricted duty cycle, the inductor current cannot always increase or decrease.

Also the fault tolerant topology based on redundancy is introduced. Thanks to the proposed fault detection method, according to the type of the switch failure (OCF or SCF), two different strategies for the converter reconfiguration are proposed. In case of an OCF, the faulty switch can be replaced by the redundant switch immediately after the fault detection. But in case of a SCF, the converter reconfiguration can be done after the faulty switch is disconnected physically by a protection element such as a fuse [19]. The proposed fault detection algorithm and fault tolerant converter do not require any additional sensor. In fact, the current sensor for inductor current measurement is the same used for control loops. By this way, without additional current sensor, fault detection, fault identification and converter reconfiguration, even in SCF case, are performed.

HIL and experimental results presented in this paper prove excellent performances of the proposed fault tolerant operation for both open and short circuit switch faults.

To the best of our knowledge, the fault tolerant capability proposed in this paper is one of the fastest fault detection and reconfiguration for single switch DC-DC converter service continuity, in both open and short circuit cases.

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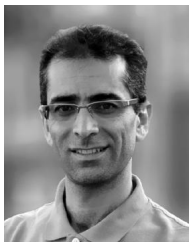

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