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Photovoltaic Systems Reliability Improvement by Real-Time FPGA-Based Switch Failure Diagnosis and Fault-Tolerant DC-DC Converter

Ehsan Jamshidpour, *Member, IEEE*, Philippe Poure, *Member, IEEE*, and Shahrokh Saadate, *Member, IEEE*,

Abstract—The increased penetration of Photovoltaic (PV) systems in different applications with critical loads such as in medical applications, industrial control systems and telecommunications has highlighted pressing needs to address reliability and service continuity. Recently, distributed Maximum Power Point Tracking (MPPT) architectures, based on DC-DC converters, are being used increasingly in PV systems. Nevertheless, DC-DC converters are one of the important failure sources in a PV system. Since the semiconductor switches are one of the most critical elements in these converters, a fast switch Fault Detection Method (FDM) is a mandatory step to guarantee the service continuity of these systems. This paper proposes a very fast FDM based on the shape of the inductor current associated to Fault Tolerant (FT) operation for boost converter used in PV systems. By implementing fault diagnosis and reconfiguration strategies on a single FPGA target, both types of switch failure (open and short circuit, so called OCF and SCF) can be detected, identified and handled in real time. The FDM uses the signal provided by the current sensor dedicated to the control of the system. Consequently, no additional sensor is required. The proposed FT topology is based on a redundant switch. The results of Hardware-In-the-Loop (HIL) and experimental tests, which all confirm the excellent performances of the proposed approach, are presented and discussed. The obtained results show that a switch fault can be detected in less than one switching period, typically around 100 microseconds in medium power applications, by the proposed FDM.

Index Terms—Photovoltaic system, Reliability, Real-Time fault detection, Switch fault diagnosis, Fault tolerant DC-DC converters.

I. INTRODUCTION

IN the past decades, because of the environmental concerns and the reduction of fossil fuels, many research works have targeted the use of Renewable Energy Sources (RES) as an alternative resource. Among the RES, PV systems have a remarkable growth and a significant penetration in many applications such as space systems, telecommunication, solar battery charging stations, electric vehicles, residential and

commercial installations, as well as parts of hybrid power systems. These systems also find wide use in isolated sites such as desert regions.

Fig.1 shows different structures which are commonly used in PV systems [1]. Among these ones, the multi-string and module distribution structures are suitable for PV grid-connected applications because they can keep high efficiency based on MPPT and reduce the energy losses due to mismatch; while, individual modules, controlled by their own conditioners, are advisable for applications such as residential rooftop [2].

PV systems have a complex structure and are vulnerable to faults. Generally, the principal parts of a PV system are PV modules, power electronic converters, MPPT controllers and energy storage devices. A failure may occur in any part of the system such as PV panel, power converter or sensor. To ensure service continuity and power quality in PV systems with critical loads, a reliability study (diagnosis, supervision and fault detection) is mandatory. In the recent years, the scientific researches in PV reliability studies are focused on storage devices and power electronic converters which are usually the most critical parts in terms of failure rate, lifetime and maintenance cost [3]. The converter failures, caused by semiconductor faults account for 21% of the total failures in power converters [4], [5]. According to a survey [6], semiconductor and soldering joints failures in power devices take up 34% of power electronic system failures. On the other hand, the DC-DC step-up converters are usually used to perform MPPT in PV systems [7], [8]. Based on reliability

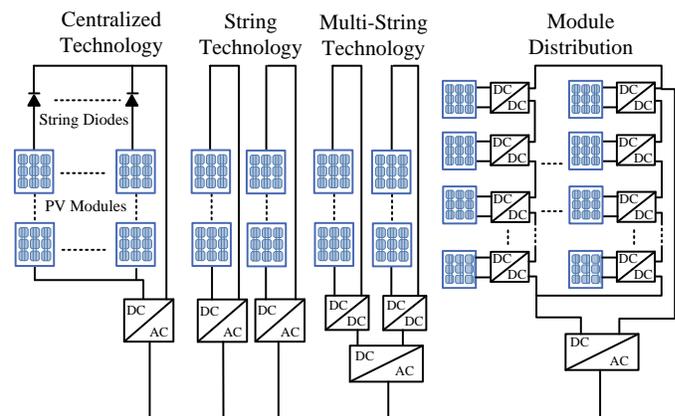


Fig. 1. Different structures used in PV systems [1].

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Ehsan Jamshidpour and Shahrokh Saadate are with the University of Lorraine, GREEN laboratory, Faculté des Sciences et Technologies, BP 70239, 54506 Vandoeuvre-les-Nancy, France (ehsan.jamshidpour@univ-lorraine.fr, shahrokh.saadate@univ-lorraine.fr).

Philippe Poure is with the University of Lorraine, Institut Jean Lamour, UMR 7198 CNRS, Faculté des Sciences et Technologies, BP 70239, 54506 Vandoeuvre-les-Nancy, France (philippe.poure@univ-lorraine.fr)

study in grid-connected PV systems, the failure rate of DC-DC boost converter is 41% [9]. Therefore, a fast FDM and FT operation for these converters should be proposed in PV systems reliability studies.

A few works have studied switch fault detection for isolated DC-DC converter and associated FT topologies, especially based on H-bridge as in [10]–[14]. In [15], Ribeiro *et al* have proposed a switch FDM in DC-DC converters and FT converter topologies dedicated to PV systems. An OCF diagnosis and FT scheme for a three-level boost converter are presented. The control variables used for MPPT and output DC-link capacitor voltage balance are treated for fault diagnosis. By adding a few components to the original converter, it can be partly reconfigured into a two-level boost converter for post-fault operation. In [16], an OCF detection method based on comparison of the duty cycle with the inductor current slope is proposed for Hybrid Electric Vehicles (HEV). Besides, a multi-mode bi-directional DC-DC converter is used for fault compensation. In [17], a FPGA-based switch fault detection method for non-isolated DC-DC converter is proposed. This approach is based on the inductor current slope observation and contains two different algorithms working in parallel. This method can detect both types of fault (OCF and SCF) in two switching periods but cannot identify the type of failure. In [18], an alternative OCF diagnosis method for boost interleaved DC-DC converters operating in unidirectional power flow, using in PV system, is studied. This method is based on features of the DC-link current derivative sign during fault and healthy operations.

In this paper, switch OCF and SCF detection and fault tolerant operation for boost converter used in PV systems are studied and validated. The principle of the proposed FDM, is also based on the sign of the inductor current slope. To realize this FDM, only one algorithm is used (instead of two algorithms in [17]) and the limitations over the duty cycle or switching frequency are also decreased. The proposed FDM is faster than the methods presented in [16]–[18], and contrary to these ones it is capable to identify both types of failure (OCF and SCF).

To improve the reliability of the PV systems, FT converter by applying this FDM, is then studied. It requires only a very few additional components to the original converter. According to the identified failure (OCF or SCF), two different strategies for system reconfiguration are proposed.

In the following sections, the proposed FDM and FT converter topology are presented; some HIL (Hardware in the Loop) and experimental results are provided. Both HIL and experimental results confirm the effectiveness of the proposed FDM and FT topology. Thanks to FPGA implementation and algorithm performances, the fault can be detected in less than one switching period. The system reconfiguration, in case of OCF, may be performed immediately after fault detection. But, in case of SCF, the system reconfiguration must be realized after fault clearance.

II. FAULT DIAGNOSIS

Fault tolerance in a power converter requires three steps: fault detection, fault identification and remedial actions. The

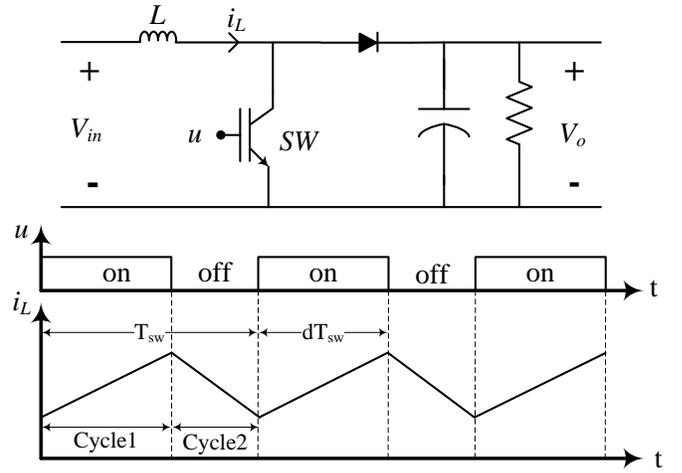


Fig. 2. Boost converter and operation cycles.

proposed FDM has the capability to do the first two steps (detection and identification) simultaneously by using the switch command signal and the sign of the inductor current slope, provided by the current sensor used in the system control. The maximum detection time is one switching period. The proposed method is described in the following.

Fig. 2 shows a boost converter, its switch command signal (u) and inductor current $i_L(t)$; the effect of the inductor's resistor is ignored. According to Fig. 2, one switching period (T_{sw}) can be subdivided into two cycles of converter operation: Cycle1 for switch SW on and Cycle2 for switch SW off. The proposed algorithm is based on the fact that when the switch is on (Cycle1) the inductor current (i_L) increases and when the switch is off (Cycle2) it decreases (Fig. 2). If i_L is always increasing or decreasing during one switching period, it can be concluded that a failure has occurred.

To realize the proposed fault detection method, a State Machine (SM) is used. The SM consists of five inputs (T_1 , T_2 , T_3 , T_4 and the sign of the inductor current slope (sgn signal)), eight states and two outputs (SCF and OCF), as shown in Fig. 3. To generate T_1 and T_2 , a $15kHz$ triangular signal (carrier)

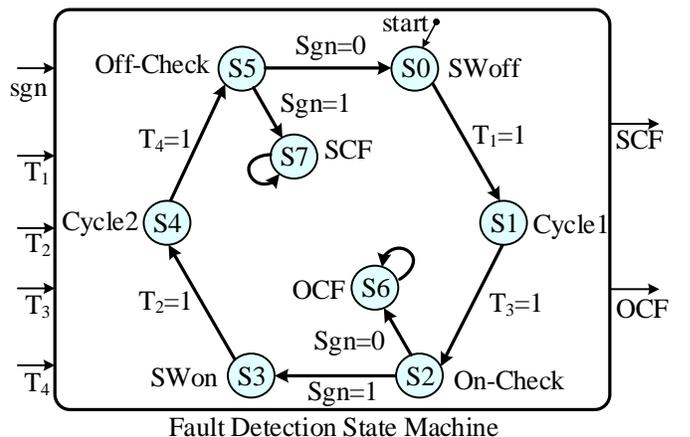


Fig. 3. The state machine used for FDM.

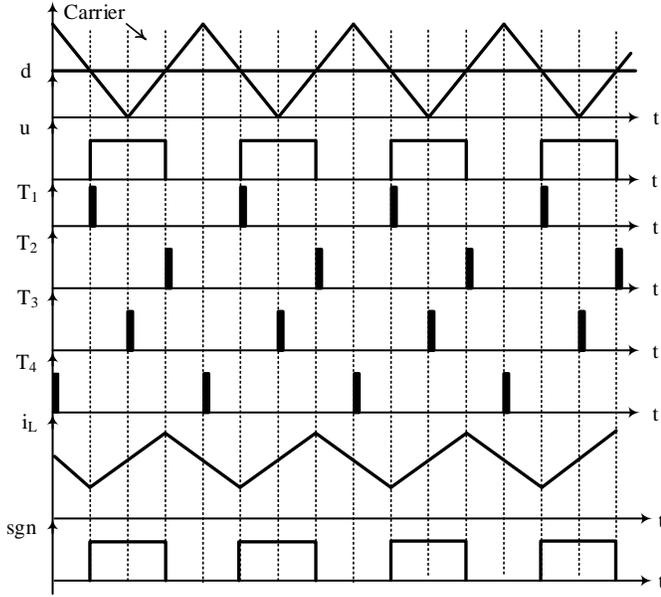


Fig. 4. Input signals of the State Machine.

with an amplitude equal to '1', is compared with the duty cycle d provided by the system control, which also generates PWM switch command (u), as shown in Fig. 4. According to this Figure, $T1$ and $T2$ are corresponding to rising-edges and falling-edges of the switching command (u) respectively. It is clear that by each pulse of $T1$, the inductor current i_L increases and by $T2$ this current decreases. The $T3$ and $T4$ signals are activated in the middle of Cycle1 and Cycle2 respectively. When the carrier signal is equal to zero $T3 = 1$ and $T4$ goes to '1' when the carrier is equal to '1'. Thus, these two signals ($T3$ and $T4$) are independent from the system controller and just depend on the carrier signal.

Besides, this algorithm needs only the sign and not the exact value of the inductor current slope. This one is obtained by comparing the value of $i_L(t)$ with its value at $T_{sgn} = 4T_s$ before, where T_s stands for the sampling period. When i_L increases, $sgn = 1$ and it is equal to '0' when the current decreases. The fault detection algorithm is detailed in the following.

A. Open Circuit Fault detection

As illustrated in Fig. 3, in initial state ($S0$), the switch is off, i.e. $u = 0$, and SM stays in this state until $u = 1$ and $T1 = 1$; then a transition to state $S1$ (Cycle1) occurs. In state $S1$, when $T3$ goes to '1', a transition to $S2$ occurs, this state allows to verify the on state of the switch SW.

In state $S2$ (On-Check), the converter is in the middle of Cycle1:

- If no failure has occurred, the switch SW should be on, i_L increases and $sgn = 1$ thus a transition to state $S3$ occurs.
- If an OCF has occurred, i_L decreases and $sgn = 0$. Therefore, a transition to $S6$ occurs and SM stays in this state.

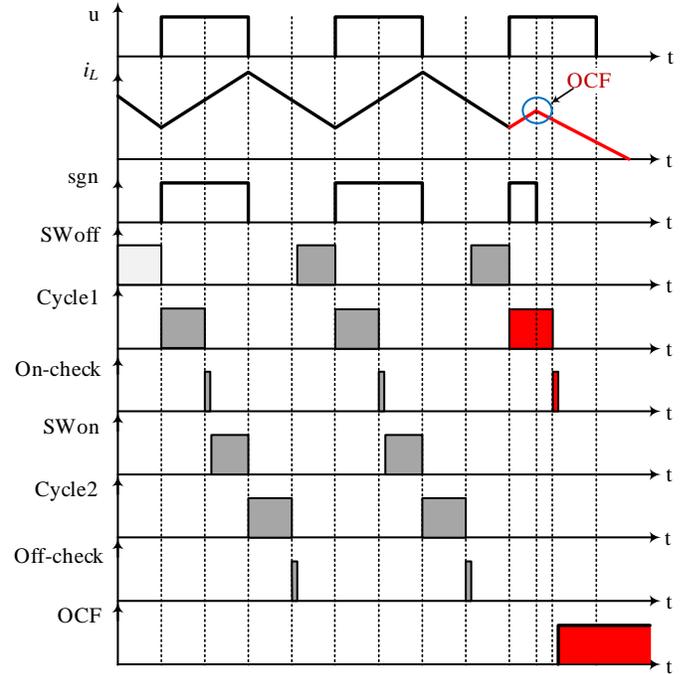


Fig. 5. OCF detection based on FDM signals.

In $S6$, the OCF signal (output of the SM) goes to '1' and an OCF is declared. Fig. 5 shows the signals and transitions for OCF detection.

B. Short Circuit Fault detection

For SCF detection, the SM transitions from $S0$ to $S2$ are the same as in OCF case. In $S2$ (On-Check), the converter is in the middle of Cycle1, if no failure has occurred (or in a SCF case), the switch SW is in on state, i_L increases and $sgn = 1$ thus a transition to $S3$ occurs. State $S3$ corresponds to the on state of switch SW, SM stays in this state until $u = 1$ and then a transition to $S4$ occurs when $T2 = 1$. According to Fig. 2, $S4$ coincides with Cycle2. In the middle of Cycle2, signal $T4$ goes to '1' and then a transition to $S5$ occurs.

In state $S5$ (Off-Check), the converter is in Cycle2 and the switch SW should be off:

- If no failure has occurred, i_L decreases and $sgn = 0$ thus a transition to $S0$ occurs.
- If a SCF has occurred, i_L increases and $sgn = 1$, thus a transition to $S7$ occurs and SM stays in this state.

In state $S7$ the signal SCF goes to '1' and a short circuit fault is declared. Fig. 6 shows the signals and SM transitions for SCF detection.

It should be noted that as a result of non-ideal behavior of power switches, delays and dead times are inevitable. Furthermore, a time (T_{delay}) to determine the sign of the inductor current (sgn) should be considered. Therefore, even in healthy operation of the converter, the sgn signal is delayed with respect to the switching commands. This is why the state (on or off) of the switch SW is verified right in the middle of Cycle1 ($S2$) and Cycle2 ($S5$) in order to take into account

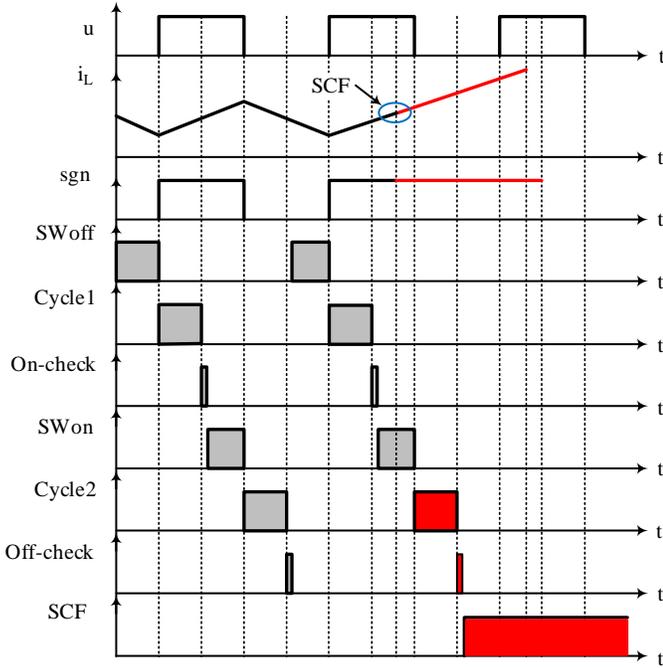


Fig. 6. SCF detection based on FDM signals.

these delays and dead times. The limitation which must be considered to avoid false fault detection is expressed in (1):

$$T_{delay} + T_{sgn} + T_s < \frac{d \cdot T_{sw}}{2} \quad (1)$$

By using FPGA, T_s is as low as $1\mu s$. So, according to (1), the limitation over the duty cycle (d) will be in the usual range of [10%; 90%].

The third step of FT operation (so called remedial actions) requires a FT topology and FT strategies which are described in the next section.

III. FAULT TOLERANT OPERATION

A. Fault tolerant converter

To ensure service continuity of the studied boost converter after a fault detection and identification, remedial actions are necessary. These actions consist of two parts: fault isolation and system reconfiguration which are explained in this section. The proposed FT topology is depicted in Fig. 7. After fault detection, identification and isolation, the faulty switch (SW) will be replaced by the switch SW_R . Then, the converter can operate in normal conditions.

Note that this fault tolerant topology is particularly cost optimized for systems with multiple parallel converters connected to a common bus. This is the case of module distribution and multi-string structures in PV systems [2], as well as in hybrid power systems where the sources (PV panels) are connected to a common DC bus through DC-DC converters.

An example for these systems is given in Fig. 8. In this case, for each converter, a fault detection and fault tolerant block (as described in Fig. 7) must be considered. Each block observes the signal sgn of the inductor current (i_k) and the

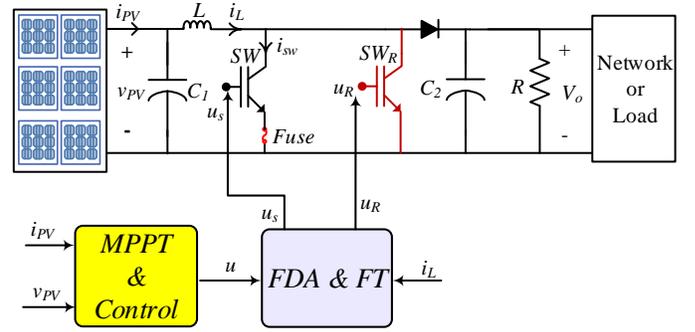


Fig. 7. Proposed FT boost converter topology.

switch command u_k , $k \in \{1, 2, \dots, n\}$. When a fault appears in the switch of a converter k (SW_k), the FT block of this converter detects, identifies the failure and according to the fault type, isolates the faulty switch (SW_k) and replaces it by the switch (SW_R) by switching on the bidirectional switch T_k . The proposed topology requires k bidirectional switches (T_k) and only one redundant switch (SW_R) for the whole system.

According to the type of switch failure (OCF or SCF), different reconfiguration strategies are considered, as explained in the following.

B. Fault isolation and reconfiguration

According to the type of the switch failure (OCF or SCF), this step has to be differently applied to the system. If an

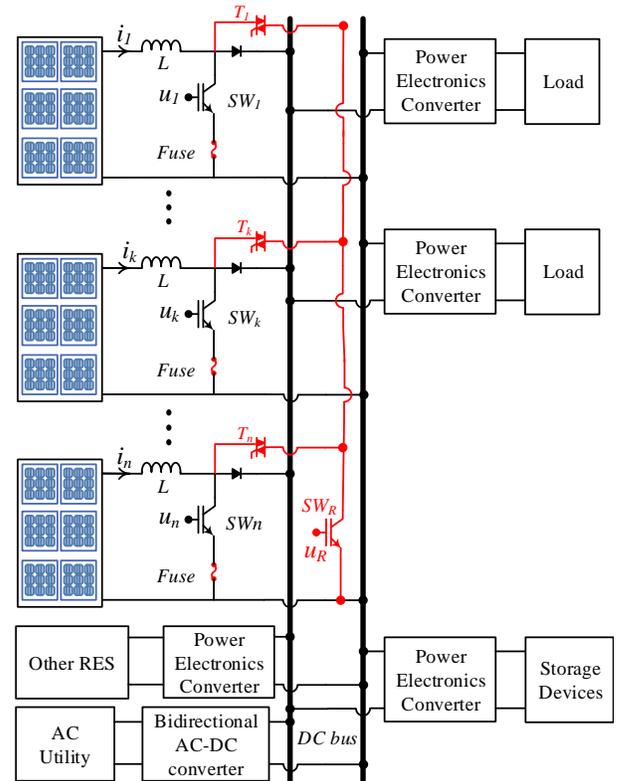


Fig. 8. Proposed FT topology for multiple parallel-connected DC-DC converters.

OCF occurs, after fault identification by FDM block, the faulty switch can be immediately replaced by the redundant switch SWR (Fig. 7). But, in case of SCF, as long as the SCF is present on the switch, SW cannot be replaced by the redundant switch. In fact, in SCF case, after fault detection, first the faulty switch should be isolated by means of fuse protection [19]. To reconfigure the converter, FT algorithm observes indirectly the current i_{sw} (switch current in Fig. 7) through the value of the 'sgn' signal. Thus no additional current sensor is needed. When i_{sw} becomes zero, this means that the faulty switch is removed by the fuse. In case of a SCF, the inductance current (i_L) increases during the fault, then the sign of current slope is positive and 'sgn' is equal to '1'. After fuse breaking, the switch SW is disconnected from the converter and i_{sw} becomes equal to zero. And then, the inductor current (i_L) starts decreasing, thus 'sgn' will be '0'. At this time, the faulty switch can be replaced by SWR.

The reconfiguration strategy is summarized in Fig. 9. According to this figure, the redundant switch can replace the faulty switch when the signal FT is '1'.

IV. FAULT-TOLERANT CONTROL IMPLEMENTATION ON A FPGA CHIP

Hardware-in-the-loop (HIL) approach is one of the preferred, reliable and cost-effective alternative in a virtual scenario for time-consuming, non-destructive and expensive tests on real devices [20]. This solution for fault tolerant systems, reduces design time and helps to evaluate the behavior of newly topology, fault detection methods, controllers, and protective devices in an effective and economic approach before applying them in a real system. HIL allows the validation of fault tolerant operation subjected to extreme (faulty) conditions in a non-destructive environment and an expedited manner [20]–[22].

In this paper, a design methodology based on FPGA (Field Programmable Gate Array) rapid prototyping, so called "FPGA in the loop" [23] is used to test experimentally the

proposed fault tolerant operation. Moreover, we can notice that FPGAs are used in recent PV applications in order to embed many advanced control functions [4]. In this work, the controller, the proposed FDM and FT strategies are implemented in a single FPGA chip, as presented in Fig. 10. Before FPGA implementation for HIL experiments, the studied system has been modeled and successfully simulated in Matlab/simulink environment, in continuous-time and then in discrete-time. Then, the control, FD and FT blocks are translated into a synthesizable VHDL model. Finally, the development board which contains the FPGA can be programmed and used in the HIL simulation.

The FPGA development board is linked to a PC via a Joint Test Action Group (JTAG) connection. This interface performs communication between the FPGA (which implements the controller, the fault detection and fault tolerant scheme) and the system (emulated by the PC with Matlab/SimPowerSystems). When the FPGA receives signals from the PC, it executes the implemented program for one sample interval. The FPGA returns control signals, computed during this step, to the PC. At this point, one cycle is performed.

After validation of the control and fault tolerant method by HIL results, the FPGA can be programmed and the fully experimental tests can be performed (Fig. 10). In our case, a Stratix DSP S80 development board is used, which includes the Stratix EP1S80B956C6 FPGA chip.

V. HARDWARE-IN-THE-LOOP RESULTS

For HIL experimentation, the converter given in Fig. 7 is considered. A classical PI controller is used to control the converter. The system parameters are given in TABLE I, which are the same as in the experimental bench.

In a PV system, the operation point of the system changes with a slow dynamic compared with the FDM's dynamic. Based on this hypothesis, for HIL and experimental tests, the PV source is replaced by a programmable voltage source.

Fig. 11 shows detailed HIL results for an open circuit fault detection. At $t = 240\mu s$ an OCF occurs. At this time, the SM is in state $S1$ corresponding to Cycle1. When $T3$ goes to '1' a transition to $S2$ occurs, as in normal condition. But,

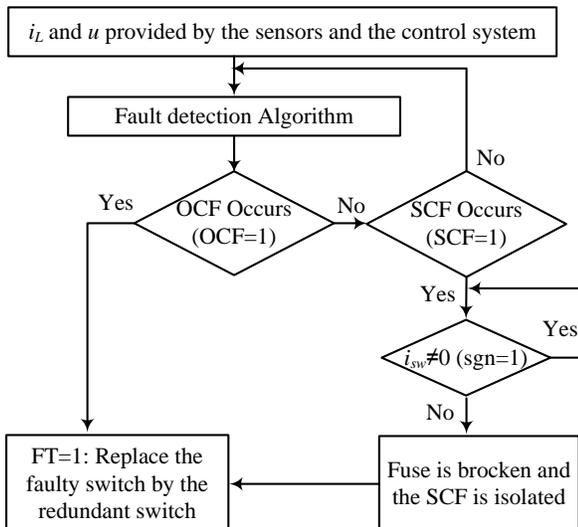


Fig. 9. Reconfiguration strategies in SCF and OCF cases.

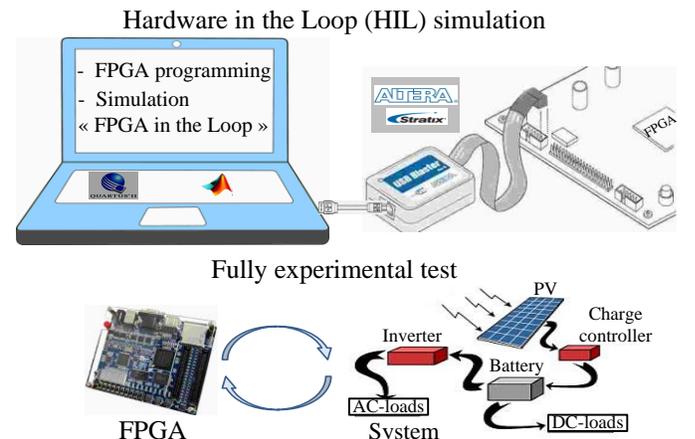


Fig. 10. "FPGA in the Loop" prototyping and fully experimental test.

TABLE I
PARAMETERS OF THE BOOST CONVERTER

| Elements | Value |
|---------------------|--------------|
| L | 9mH |
| C_1 | 1100 μ F |
| C_2 | 50 μ F |
| Switching frequency | 15 kHz |

because of the OCF, the current (i_L) decreases ($sgn = 0$) thus the SM cannot move to $S3$ and must generate a transition to the state $S6$. In this state, the output signal OCF goes to '1' and the fault is detected successfully at $t = 253\mu s$. The fault detection time is $13\mu s$ which is less than one switching period (here $T_{sw} = 67\mu s$).

The HIL results for a SCF detection are depicted in Fig. 12. At $t = 240\mu s$ when the SM is in state $S1$ a SCF occurs. The transitions from $S1$ to $S5$ occur normally. In state $S5$, because of the SCF, the current i_L increases and consequently sgn is equal to '1', thus a transition to $S7$ occurs. In $S7$ the output signal SCF goes to '1' and the SCF is detected at $t = 287\mu s$. The fault detection time in this case is $47\mu s (< 67\mu s)$.

All these results confirm the validity of a very fast fault detection method.

VI. EXPERIMENTAL RESULTS

Experimental tests are performed, based on a boost converter with a redundant switch, as depicted in Fig. 7. A synoptic of the experimental set-up is given in Fig. 13. It

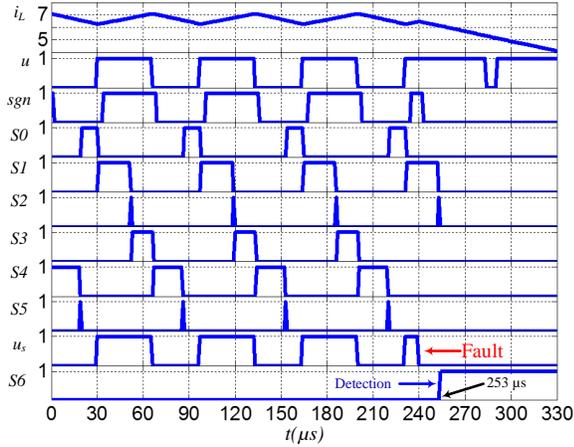


Fig. 11. Detailed HIL results for OCF detection case.

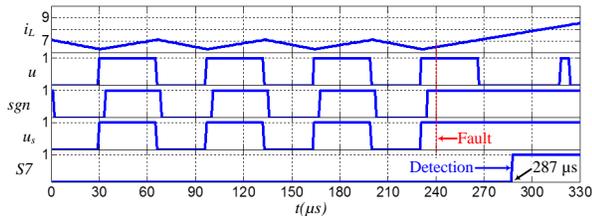


Fig. 12. HIL results for SCF detection.

consists on a Stratix DSP S80 development board, an interface card, a resistive load and a programmable TDK source which is used as a PV source for a fixed operating point. The switches are IGBTs, SEMIKRON SKM50GB123D devices. It is noticeable that the ' u_s ' is equal to ' u ' in pre-fault (healthy) operation. To simulate a switch fault, the ' u_s ' signal is forced to '0' for an OCF and '1' for a SCF. The ' u_R ' is the redundant switch command, which is equal to zero for pre-fault operation and copies ' u ' for post-fault operation.

First, let us verify the validity of the FDM. The experimental results for an OCF are shown in Fig. 14. The switch SW is kept off by forcing ' u_s ' to '0'. As shown in Fig. 14, in this test, the OCF appears when the switch SW is on and the SM is in state $S1$. When $T3$ goes to '1', a transition to $S2$ occurs. In state $S2$, because of the OCF, the current decreases and thus $sgn = 0$, therefore a transition to $S6$ is generated and the output signal OCF goes to '1'. Then, the OCF is declared. As illustrated in Fig.14, the fault is detected in $18\mu s$ by FDM.

Fig. 15 shows the results for SCF. The switch SW is kept on by forcing ' u_s ' (Fig.13) to '1'. The SCF appears when the switch SW is on and the SM is in state $S3$. At the time when the switch command (u) stepped up (or when $T2 = 1$), a transition to $S4$ occurs. The SM stays in state $S4$ until $T4 = 1$ and then a transition to $S5$ (off-check) occurs. In state $S5$, because of the SCF, the current i_l increases and therefore $sgn = 1$, thus a transition to $S7$ is generated and then the SCF is detected. As presented in Fig.15, the short circuit fault is declared after $26\mu s$ by FDM.

Second, the validity of the FT operation in case of an OCF is verified in Fig. 16. In this case, the OCF is detected after $66\mu s$. According to the proposed reconfiguration strategy (Fig. 9), the redundant switch replaces the faulty switch immediately after fault detection and then the system continues to operate in normal conditions.

Fig. 17 shows the same results for a SCF. According to these experimental results, the SCF is detected after $66\mu s$ but the current continues to increase until the end of the fuse action. As soon as the faulty switch is removed by the fuse

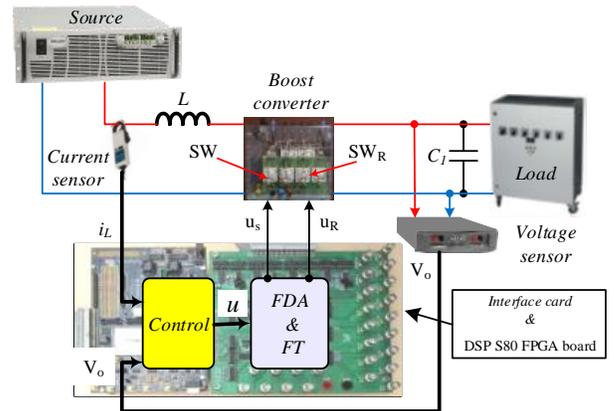


Fig. 13. Synoptic of the experimental test bench.

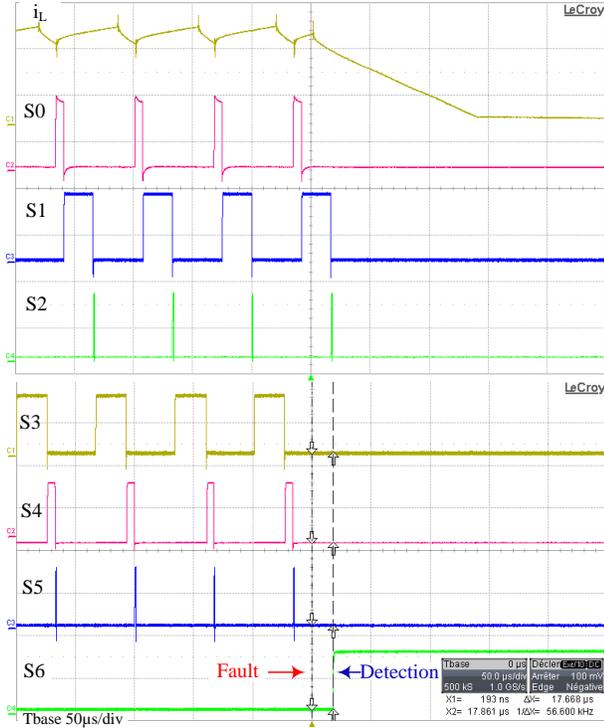


Fig. 14. OCF detection ($V_i n = 35V, V_o = 150V, d = 77%$) and SM transitions.

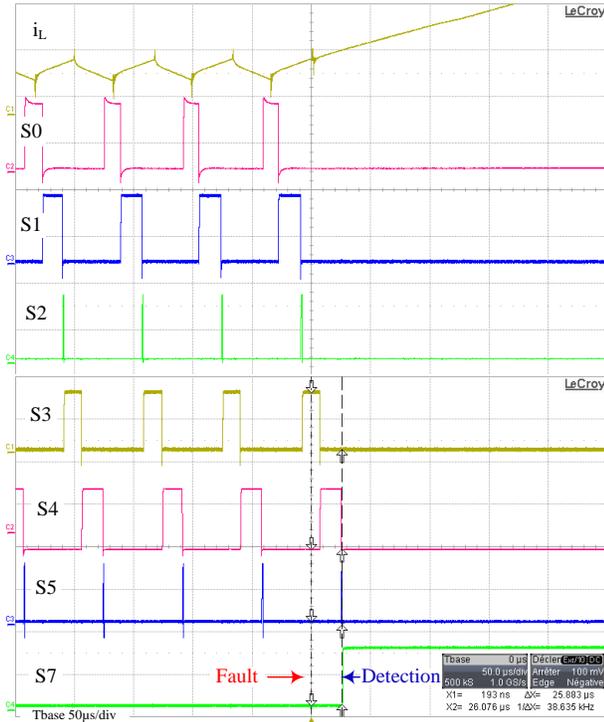


Fig. 15. SCF detection ($V_i n = 75V, V_o = 150V, d = 50%$) and SM transitions.

(after $500\mu s$), the current decreases ($sgn = 0$), the faulty switch is replaced by the redundant switch and then the system continues to operate normally.

These results show that the proposed FDM can always

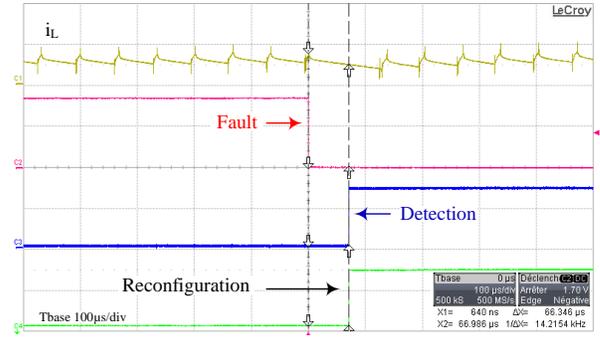


Fig. 16. OCF detection and reconfiguration ($V_i n = 135V, V_o = 150V, d = 10%$).

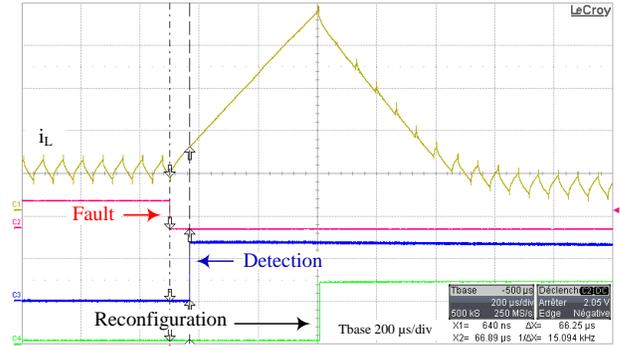


Fig. 17. SCF detection and reconfiguration ($V_i n = 75V, V_o = 150V, d = 50%$).

detect and identify open and short circuit switch faults correctly. Also, the effectiveness of the fault tolerant topology is confirmed by these experimental tests.

VII. CONCLUSION

This paper has focused on fault tolerant operation of boost converters used in PV systems. The fault detection is based on a fast FPGA-based diagnosis approach for open and short circuit switch failure. This new FDM can detect and identify the type of the fault (OCF or SCF) which is mandatory for fault isolation strategy and FT reconfiguration. The inductor current and switch command are only used to detect both failures. The maximum required time to detect a switch failure by this FDM is only one switching period.

Then a fault tolerant topology by adding a few components to a boost converter is introduced. Due to the proposed FDM, which declares the type of the switch failure (OCF or SCF), two different strategies for the converter reconfiguration are proposed. In case of an OCF, the converter reconfiguration can be applied immediately after the fault detection. But, in case of a SCF, the faulty switch can be replaced by the redundant switch when this one has been disconnected physically by a protection element such as a fuse. The current sensor which is considered for control loops is used also for FDM, thus no additional sensor is required. This approach can be applied on a system with several parallel DC-DC converters connected to a common DC bus. In this case only one redundant switch is needed for the whole system .

TABLE II
COMPARISON OF THE SWITCH FAULT DIAGNOSIS METHODS

| References | Detection parameter | Application | Detection time | Switching frequency | type of fault | Fault identification |
|------------|----------------------------------|-------------------------------|-----------------------|---------------------|---------------|----------------------|
| [10] | Transformer primary voltage | ZVS full-bridge converter | $2ms^{\dagger}$ | $50kHz$ | OCF | – |
| [11] | Magnetic component voltage | Most PWM converters | $< 1T_{sw}$ | $48kHz$ | OCF and SCF | Yes |
| [12] | DC-link current | ZVS full-bridge converter | $100ms^{\dagger}$ | * | OCF | – |
| [14] | Magnetic near field | Most converters | * | * | OCF and SCF | No |
| [15] | Output DC-link capacitor voltage | Three-level boost converter | $100ms^{\dagger}$ | $5kHz$ | OCF | – |
| [17] | Inductor current slope | Non-isolated single-switch | $< 2T_{sw}$ | $15kHz$ | OCF and SCF | No |
| [18] | DC-link current derivative sign | Interleaved DC-DC converter | $> 3T_{sw}^{\dagger}$ | $3kHz$ | OCF | – |
| This paper | Inductor current slope | Single switch DC-DC converter | $< 1T_{sw}$ | $15kHz$ | OCF and SCF | Yes |

In this table, T_{sw} is the switching period; "*" means that the detection time is uncertain and cannot be defined; † means that the detection time is deduced from experimental results.

Before carrying out experimental tests, an HIL simulation by using a rapid prototyping method based on FPGA ("FPGA in the Loop") has been performed; it allows to test the proposed fault tolerant operation in a non-destructive manner. The system control, the fault detection method and the fault tolerant operation strategies are implemented in a single FPGA chip. They have been all validated first through HIL. Then experimentations are carried out which prove excellent performances of the proposed FT operation for both open and short circuit switch failures. Furthermore, the system is capable to operate after reconfiguration without any performances degradation.

The method proposed in this study is particularly dedicated to boost converter. Nevertheless, it can be applied to any other topology of the single switch DC-DC converters family such as buck, buck-boost, Cuk, SEPIC, and dual SEPIC converters.

A comparison of the proposed fault detection method with other methods from the literature is presented in Table II. According to this table it can be noted that the proposed method is one of the best in term of real time fault detection in both OCF and SCF cases. Then the reliability and power quality in module distribution and multi-string structures with distributed MPPT in PV systems can be improved.

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Ehsan Jamshidpour (M'5) was born in Kermanshah, Iran, in 1975. He received the B.S. degree from University of Tabriz, Tabriz, Iran, in 1999, the M.S. degree from Sharif University of Technology, Tehran, Iran, in 2001 and Ph.D. in Electrical Engineering from University of Lorraine, Nancy, France, in 2014. From 2003 to 2010, he was an Assistant Professor in electrical engineering with the Institute for Energy and Hydro Technology, Kermanshah, Iran. He is currently with the University of Lorraine, Nancy, France. His research interests are, Renewable

energy, Power electronic converters and fault tolerant converters.



Philippe Poure (M'5) was born in 1968. He received the Engineer Degree and Ph.D. Degree in Electrical Engineering from INPL-ENSEM-GREEN, France, in 1991 and 1995 respectively. From 1995 to 2004, he was an Associate Professor and worked at the University Louis Pasteur of Strasbourg, France, in the field of mixed-signal System-On-Chip for control and measurement in Electrical Engineering. Since September 2004, he joined the Université de Lorraine, Nancy - France and works on fault tolerant power systems and FPGA based

real time applications.



Shahrokh Saadate (M'2) was born in Tehran/IRAN on May 6th, 1958, received his diplôme d'ingénieur (1982), DEA (1982), thèse de doctorat (1986) and Habilitation à diriger les recherches (1995) from ENSEM, INPL, GREEN laboratory Nancy / France. He has been the head of GREEN Laboratory (2009-2012) at the University of Lorraine in Nancy France. His main research domain is power systems reliability, power quality and renewable energies.