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Switch failure diagnosis based on inductor current observation for boost converters

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Face to the growing number of applications using DC-DC power converters, the improvement of their reliability is subject to an increasing number of studies. Especially in safety critical applications, designing fault tolerant converters is becoming mandatory. In this paper, a switch fault tolerant DC-DC converter is studied.

First, some of the fastest Fault Detection Algorithms (FDA) are recalled. Then, a fast switch FDA is proposed which can detect both types of failures; Open Circuit Fault (OCF) as well as Short Circuit Fault (SCF) can be detected in less than one switching period. Secondly, a fault tolerant converter which can be reconfigured under those types of fault is introduced. Hardware-In-the-Loop (HIL) results and experimental validations are given to verify the validity of the proposed switch fault tolerant approach in the case of a single switch DC-DC boost converter with one redundant switch.

Keywords: Fault Tolerant Converter, Fault Detection, FPGA, Semiconductor Switch Failure, Non-Isolated Single Switch DC-DC Converters.

1. Introduction

The last decades have shown a growing interest in DC-DC power conversion in industrial applications mainly in renewable energy power systems. In the same time, the number of applications where power availability is mandatory has increased significantly. Indeed, there are numerous power systems where service continuity is a requirement, especially in the case of embedded power systems and in safety critical applications (Wang et al. , 2013). For example, this is one of the main requirements in applications such as electric ships, hybrid electric vehicles (Park, T., Kim, T. , 2011) or trains (Song, Y., Wang, B. , 2013).

Failure in DC-DC power electronics has been subject to several studies (Wang et al. , 2013; Wolfgang , 2007), as well as reliability of power electronics (Song, Y., Wang, B. , 2013). Among the components of power electronic converters, it appears that the two critical elements are the electrolytic capacitors with around 50% of the malfunctions and breakdowns reported (Amaral et al. , 2012), followed

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by the semiconductors with more than 30% of the failures (Abdou, 2014; Wolfgang, 2007). Some diagnosis methods for the electrolytic capacitors have been proposed in (Amaral et al. (2012); Amaral et al. (2009)). This paper deals with the following aspect: the study of diagnosis and fault tolerance in case of switch failures.

In (Wu et al. , 2013), the authors give an overview of failures and fault-tolerant design of Insulated Gate Bipolar Transistors (IGBT) power electronic converters. A survey on fault diagnosis methods and protection of IGBT with special focus on those used in three-phase power inverters is presented in (Lu, B., Sharma, S. K. , 2009). More articles in the case of DC-DC conversion structures have proposed diagnosis methods for isolated DC-DC converter, especially based on H-bridge as in (Ambusaidi, et al. , 2010; Kim et al. , 2008; Pie et al. , 2012; Sheng et al. , 2012).

A few papers have proposed switch fault diagnosis method for non-isolated DC-DC power converters. A fast switch diagnosis method by adding an analogical and magnetic components on the DC-DC converter is presented in (Nie et al. , 2014). Using the analog circuit allows to perform the fault diagnosis in less than one switching period. Analogical additional circuit is also used in (Cho et al. , 2015), with a detection realized in less than two switching periods. However, considering the recent developments on digital data treatment, FPGA-based solutions are becoming more and more attractive, both in term of cost and opened possibilities, as reviewed in (Karimi et al. , 2008; Monmasson et al. , 2011). However, such digital technics could be time consuming compared to analog ones. Also, it must be explored much faster diagnosis methods with performances close to the one obtained analogically. In (Shahbazi et al. , 2013), a fast FPGA-based switch fault (Open Circuit Fault (OCF) and Short Circuit Fault (SCF)) detection method for single-ended non-isolated DC-DC converters is studied. In this paper, the inductor current slope is used as fault diagnosis criterion; no additional sensor is required and the failure can be detected in less than two switching periods. A switch fault detection method with fault-tolerant capability for non-isolated single switch DC-DC converters is proposed in (Jamshidpour et al. , 2015). This method which is based on FPGA, can detect and identify both fault types (OCF and SCF), and then proposes a reconfiguration strategy. In (Ribeiro et al. , 2014), an alternative OCF diagnosis method for boost interleaved DC-DC converters operating in uni-directional power flow is studied. This method is based on features of the DC-link current derivative sign during faulty and healthy operations. This method needs three switching periods to detect a fault.

In this paper, the inductor current is used as the fault detection criterion in the same manner as in (Jamshidpour et al. , 2015; Park, T., Kim, T. , 2011; Ribeiro et al. , 2014; Shahbazi et al. , 2013). The proposed FDA does not require additional current or voltage sensors. This method can be applied to non-isolated single-switch DC-DC power converters family, including buck, boost, buck-boost, Ćuk, SEPIC, and dual SEPIC converters. It is capable to detect and identify both types (OCF and SCF) in less than one switching period. A fault-tolerant topology based on redundancy is then proposed which allows to the converter to work as in pre-fault operation condition.

This paper is developed as follows. The first section describes the considered fault tolerant DC-DC converter. Then diagnosis method is described. Impact and requirements due to the diagnosis and fault tolerance approach are given. The constraints of the diagnosis method in order to obtain the fastest fault detection are detailed. The validity of the proposed approach is proven through HIL and experimental results. Finally, the last section gives the main conclusions of this work.

2. Switch fault tolerant boost converter

In this paper, in order to give some representative results, it is decided to focus on a specific structure: the DC-DC boost converter. Still, the same approach can be applied on any other type of non-isolated single switch DC-DC power converter. As represented in Figure 1, the fault tolerant converter has one redundant switch used in case of failure of the main one.

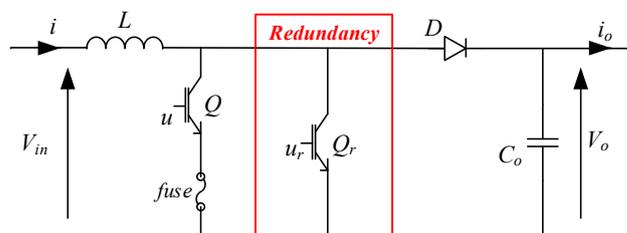


Figure 1. DC-DC boost converter with fault tolerant capability.

Tolerance against switch failure consists in three consecutive steps. First, the failure must be detected and identified as it will be detailed in section 3. In case of a converter with more than one switch, fault localization is mandatory. Since the proposed diagnosis method only focuses on single switch converter, fault location is not required. Then, the fault has to be isolated before the reconfiguration of the system. For switch failures, two configurations have to be taken into account depending on the switch failure type, OCF or SCF. In the case of an OCF, the system can immediately be reconfigured by replacing the faulty switch by the redundant one. On the other hand, in case of a SCF, the short-circuit must be cleared before using the redundant switch. For SCF tolerance, a fast fuse is used in series with the switch as proposed in (Lezana et al. , 2010; Song, Y., Wang, B. , 2013). Thus in the case of a SCF, the reconfiguration should be performed after the fuse break which will be detected by measuring a decreasing slope on the inductor current (i).

It should be noticed that even if not presented in this paper, the proposed switch fault tolerance can easily be adapted to structures consisting in several converters in parallel with a single shared redundant switch as in (Song, Y., Wang, B. , 2013) where a single redundant leg can be used indifferently if a fault occurs on DC-AC, AC-DC or DC-DC converter of a hybrid structure. In this case, for each converter in parallel another extra switch (a triac for example) will be needed as it is proposed in (Jamshidpour et al. , 2015). Also, in the literature, it is possible to find works promoting parallel redundancy for reliability purpose and fault tolerant operation such as in (Choudhary et al. , 2008). The switch fault tolerant operation proposed in this paper can easily be used in parallel structures such as in (Ribeiro et al. , 2014).

3. FPGA-based fault detection

The converter control and the Fault Detection Algorithm (FDA) are implemented on a single FPGA chip. The converter operates at fixed constant switching fre-

frequency set at $f_{sw} = 15kHz$ (corresponding switching period $T_{sw} = 1/f_{sw} = 67\mu s$). The complete FPGA-based fault tolerant scheme is depicted in Figure 2. In this figure, the converter control is also considered. As it does not interact with the purpose of this paper targeting the fault tolerant operation, the chosen control is classical, based on a two-loops PI controller acting on the mean values of the sensed variables. Still, as the control is implemented on a FPGA opening space in term of calculation time, some more complex control algorithm could be used to improve the performances of the controller. In term of implementation, the fault tolerance requires only one large bandwidth sensor and corresponding analog-to-digital converter (ADC) for the sampling of the current used for fault detection.

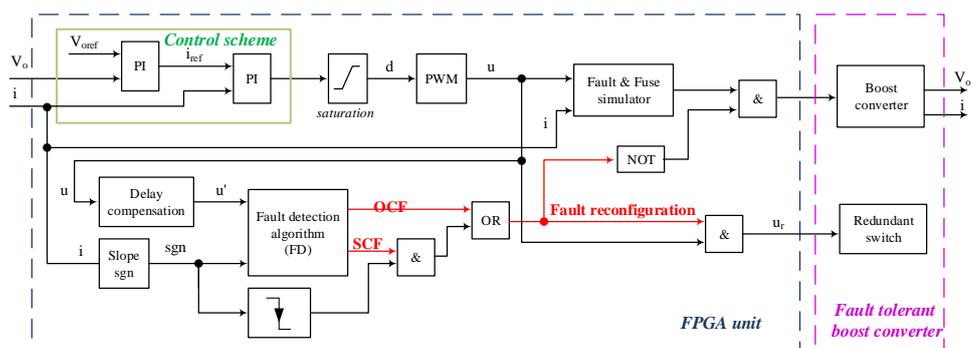


Figure 2. FPGA-based fault tolerant operating system.

3.1 Fault detection method

The switch fault detection used in this paper is based on the sign of the current slope with the possibility of distinguishing OCF from SCF. As previously mentioned, such feature is really important since OCF and SCF cannot be treated in the same way because of the fault isolation requirement.

The FDA observes if the sign of the current slope is in accordance with the imposed switch command signal. If those values differ longer than a given number (N) of sampling period, the FDA declares a failure. The FDA algorithm signals are represented in Figure 3. In this figure, the two upper signals are the switch command signal u and the sensed inductor current i . Also, the calculated sign of the current slope (sgn) is depicted in blue. As illustrated in Figure 3, the sign signal differs from the command signal for several sampling periods after a change in the state of the command signal u as represented through the error signal. A counter allows to compute how long this error lasts. In normal operation, the length of the error - and corresponding level of the counter - will only be due to natural delays of the system. Thus the time required to detect a change in the current slope sign remains limited. On the other hand, if the counter increases too much - i.e. more than a given threshold N defined later on in this section - it will traduce a fault.

This algorithm has the advantage to enable very fast detection, but it can fail if the system is working with a very large - indifferently very low - duty cycle. In (Jamshidpour et al. , 2015; Shahbazi et al. , 2013), in order to detect every possible failure, a second fault detection algorithm is used. This second algorithm also observes the sign of the current slope (sgn) changes within a switching period. If a failure occurs, depending on the failure type (OCF or SCF), the value of

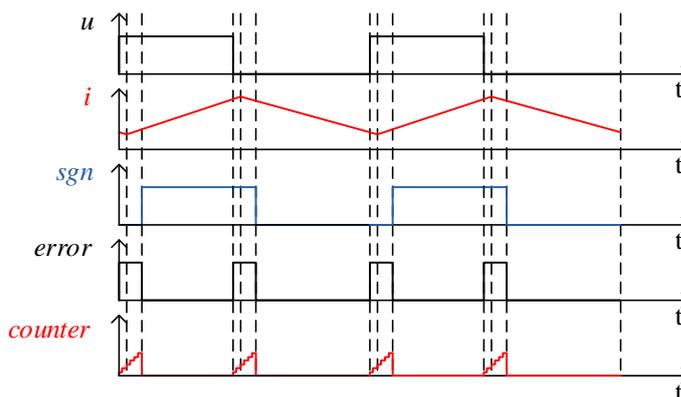


Figure 3. Fault detection algorithm signals.

sgn stays constant during the period that fault occurred in. When the switching command changes in the next switching period, the second FDA can detect the fault by comparing the signals u and sgn . Finally, for both algorithms, OCF can be distinguished from SCF depending if the fault is detected when the current is increasing (SCF) or decreasing (OCF). In this paper compared to previous works, the first FDA is improved by applying some modifications that are explained in the next section, and the second FDA is eliminated.

3.1.1 Sign of the current slope acquisition

The FDA requires the sign of the current slope. In the considered test bench, the switching frequency is $f_{sw} = 15kHz$ while the sampling frequency of the FPGA is $f_s = 1MHz$ (corresponding sampling period $T_s = 1/f_s = 1\mu s$). Then, 67 points on the current are sampled over a switching period.

In practice, the sign of the current slope is obtained by comparing the sensed value of the current with its value of 4 samples before. It has been experimentally observed that most of the time, a change of the sign of the current slope is detected within 2 or 3 samples. Still, this time can increase especially if the value of inductance increases leading to smaller slopes. Then the worst case is considered, and it can be ensured that a change on the current slope sign is detected within 4 sampling periods, corresponding to an acquisition time of $T_{sgn} = 4\mu s$. It is noticeable that the value of sgn is '1' when the current (i) increases and is '0' when i decreases or is equal to zero.

3.1.2 Time delay compensation

In practice the current slope does not change immediately with the command signal. Indeed, because of non-ideal behaviour of power switches, delays and dead times, the change of the current slope is delayed. Compared with the previous diagnosis methods, time delay compensation allows to reduce detection time. Then, it is preferable to consider this delay in the detection algorithm in order to avoid false fault declaration. Finally, the FDA will not compare the acquired sign of the current slope with the command signal u , but with the delayed command signal u' as shown in Figure 4. It results that the threshold (N) of the FDA can be reduced by several sampling periods corresponding to the delays, and then the rapidity of the fault detection is increased by the same time T_d (total delay time).

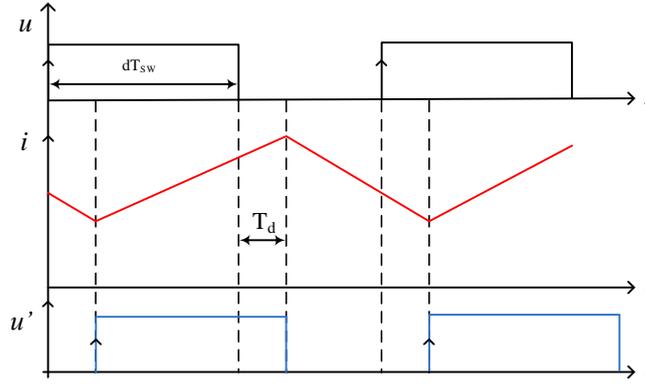


Figure 4. Natural time delays compensation.

The system delays can be theoretically determined based on the data sheets of the system components. Indeed, they include the driver propagation time, the switch commutation time, and any delays from the instrumentation chain (sensors, digital-to-analog converters DAC, ...). In this paper, the total delays of the system (calculated and verified in experimental tests) is supposed to be around $2\mu s$ ($T_d = 2\mu s$). Then the threshold N of the FDA can be reduced compared with the FDA without delays compensation. Also, it has been observed that on-delays and off-delays were about the same typical magnitude. For other components, it can be required to distinguish them for the compensation as in (Nie et al. , 2014).

3.1.3 Duty cycle limitation

A last consideration must be done while implementing the proposed switch fault tolerance scheme. Indeed, the used fault detection algorithms have been designed under the hypothesis of a constant switching frequency. The duty cycle coming from the PI regulation must then be limited in order to verify this hypothesis. Without such limitation, it will be shown that false fault detection can appear during transients.

In order to ensure those requirements, one must again consider the time required for the current slope sign acquisition T_{sgn} . The duty cycle will then be limited between a minimum and a maximum value, d_{min} and d_{max} . For the FPGA implementation, those limitations will be imposed as integer numbers of the sampling period, $n_{d_{min}}$ and $n_{d_{max}}$. Recalling notation $\lceil x \rceil$ as the smallest integer greater than x , the value of $n_{d_{min}}$ can be expressed as Eq. (1).

$$n_{d_{min}} = \left\lceil \frac{T_{sgn}}{T_s} \right\rceil = 4 \quad (1)$$

With the parameters (f_{sw} , f_s) used in practice, the limitation on the duty cycle can be calculated as follows:

$$d_{min} = \frac{n_{d_{min}}}{\frac{T_{sw}}{T_s}} = \frac{4}{67} = 0.06 \quad (2)$$

For the upper limitation of the duty cycle, the same hypothesis can be applied for cases with large duty cycles and it can be expressed as follows:

$$d_{max} = 1 - d_{min} = 1 - 0.06 = 0.94 \quad (3)$$

Then, the system is allowed to work in an interval corresponding to around 88% of the entire duty cycle. It is clear that during a transient (for example fast load variation) the system's control will try to follow the variation as fast as possible by setting the duty cycle in its maximum '100%' (or minimum '0%'). Such limitations will impact the time response of the system during transients, but they are mandatory to avoid false fault detection.

Finally, knowing the duty cycle interval, the threshold of the FDA detection algorithm (N) can be optimally determined following Eq. (4).

$$N = n_{d_{min}} + 1 = 5 \quad (4)$$

3.2 HIL verification

Hardware-In-the-Loop (HIL) approach is becoming increasingly the preferred, reliable and cost-effective alternative in a virtual scenario for tedious, time-consuming, and expensive tests on real devices. HIL for fault tolerant topologies allows evaluating the behavior of newly topologies, fault detection methods, controllers, and protective devices in an effective and economic approach, before applying them in a real system. Such testing allows the system components to be subjected to extreme conditions during fault appearance in a non-destructive environment and an expedited manner.

In this paper, the overall control and switch fault tolerant scheme have been implemented on a Stratix EP1S80B956C6 FPGA chip.

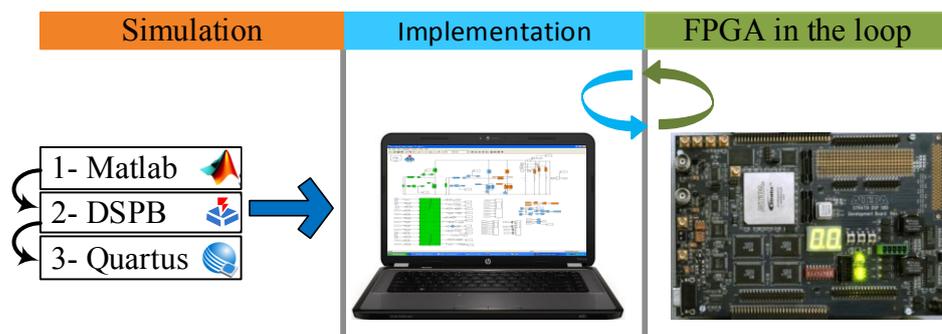


Figure 5. Hardware-In-the-Loop (HIL) synoptic.

As shown in Fig. 5, after discrete time simulations with Simulink in Matlab environment, simulation with Altera DSP Builder blocks is carried out. Using DSP Builder allows us to have visual programming and to translate it to Hardware Description Language (HDL) very easily. The VHDL design is later compiled using

Quartus software and uploaded on the Altera FPGA board via a Joint Test Action Group (JTAG) interface. In this step, the power system is simulated in the MatlabSimulink environment, while the control and diagnosis parts are both implemented on the FPGA. HIL is used for more realistic evaluation of the control and detection implementation (Karimi et al. (2008); Jovanovic et al. (2008); Karimi et al. (2009)).

In the following, HIL results are provided to verify the validity of the proposed fault tolerant approach.

3.2.1 OCF detection

The first result shown in Figure 6 gives the response of the system when an OCF occurs. For this HIL result, the system is initially working with a duty cycle around 50%.

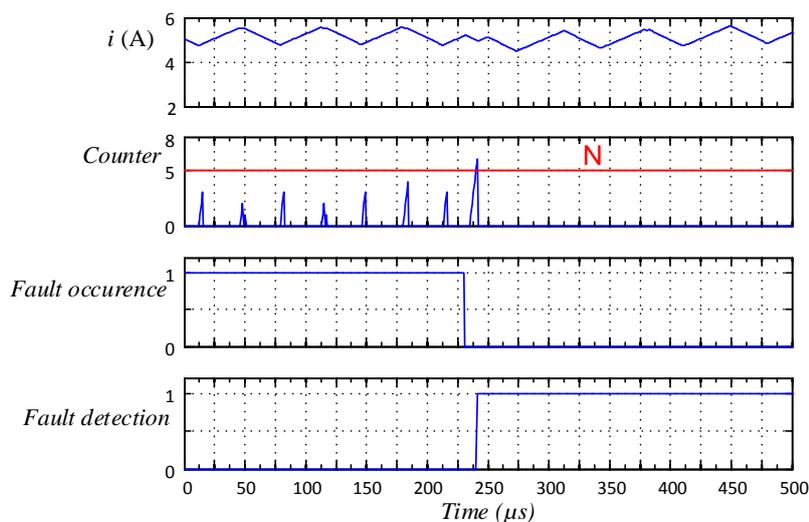


Figure 6. Detection of an OCF with a duty cycle around 50% - HIL results

As it can be seen in Figure 6, after the OCF occurs, the fault is detected through the proposed FDA algorithm in $10\mu s$ when the counter reaches the maximum value (N). Right after the detection, the system is reconfigured and the redundant switch comes into operation in replacement of the faulty one. Then the system comes back to its normal pre-fault operation.

3.2.2 SCF detection

A second HIL simulation has been realized to verify the validity of the proposed fault tolerance approach in the case of a SCF. The HIL results are given in Figure 7.

As shown in Figure 7, the SCF is detected through the FDA algorithm in $25\mu s$. Contrary to the case of the OCF, the reconfiguration is not realized directly after the fault detection. Indeed, before activating the redundant leg, the faulty switch (in short-circuit) must be removed. Then the system waits the fuse breaks before being reconfigured. This can be seen in Figure 7 on the plotted current which is rising for about $500\mu s$. Right after the fuse breaks, the current falls and the system is then reconfigured by activating the redundant switch. Because the current

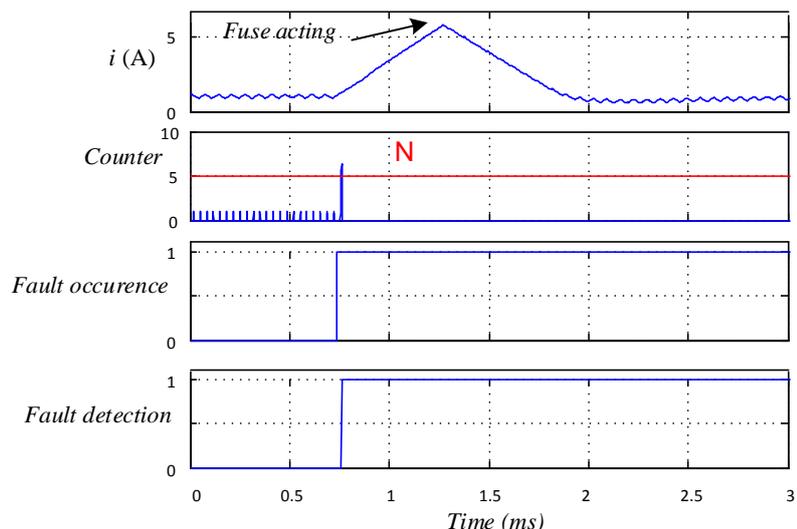


Figure 7. Detection of a SCF-HIL results

increased significantly before the fuse opened the system takes a little more than $500\mu s$ before coming back to the initial functioning point. Indeed, this time is a little higher than the rising time before the fuse breaks because the duty cycle is limited while the SCF corresponded to a duty cycle equal to one.

3.2.3 Validity of the duty cycle limitations

A last HIL result is shown in Figure 8. In this figure, we have compared the system response for a load step with and without duty cycle limitation.

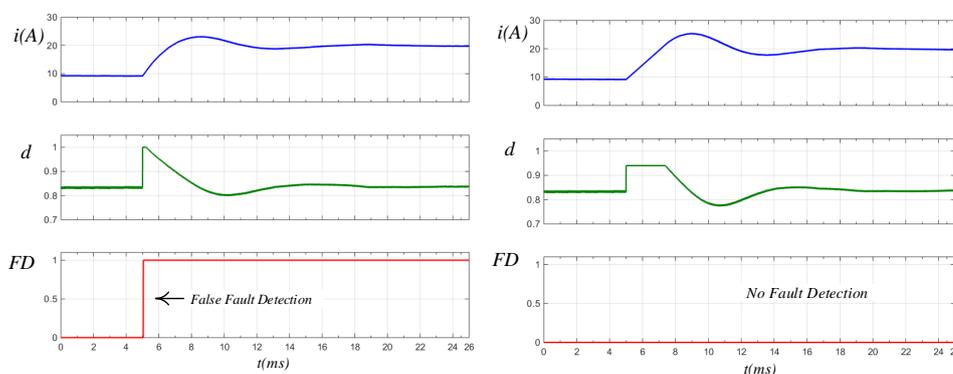


Figure 8. Fault detection validation under load variation - (left) false detection without duty cycle limitation - (right) No fault detection with duty cycle limitation.

As expected, when the duty cycle fixed by the controller is not limited, a false fault detection may occur during the transient. For this positive load step, the detection algorithm interprets the behavior of the system as a SCF. On the other hand, with duty cycle limitation, even if the system response is a little slower but the load step does not lead to any false fault detection.

4. Experimental validation

In order to validate the proposed switch fault tolerant converter, an experimental test bench has been realized in our laboratory. The parameters of the experimental set-up are listed in Table 1. The tests have been carried out through the boost converter fed by a programmable DC voltage source and loaded by a variable resistor.

Table 1. Experimental parameters

Input inductance	$L = 9mH$
Semiconductor devices	Semikron <i>SKM50GB123D</i> IGBTs
Output capacitor	$C_o = 1.1mF$

4.1 OCF detection

Figure 9 gives the results obtained when an OCF occurs; the system is initially working with a duty cycle around 50%. As for the HIL results, it can be seen in Figure 9 that the OCF is quickly detected through the FDA in less than $15\mu s$. After the OCF detection, the system is directly reconfigured and comes back to its normal operation.

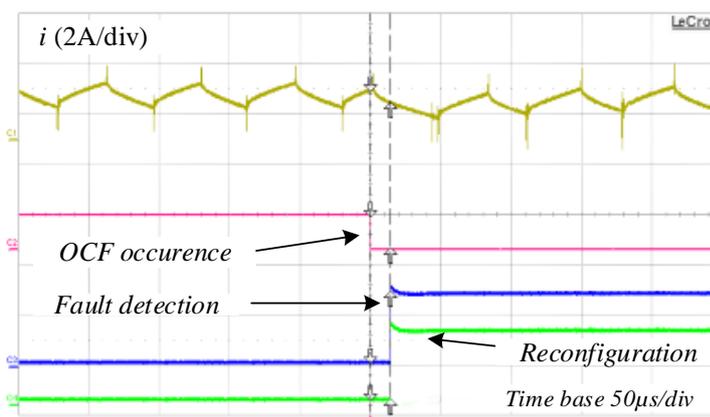


Figure 9. Detection of an OCF with duty cycle 50% - experimental results

A second experiment has been realized to verify the behavior of the system for an OCF occurrence when the system is initially working with a small duty cycle close to its lower limitation (i.e. around 11%). The results are given in Figure 10. Indeed, in this second experiment, the OCF is detected by FDA in $14\mu s$ which is close to the previous test. When the OCF is detected, the system is directly reconfigured with the redundant leg. Once again, the system quickly comes back to its pre-fault operation.

Figure 11 shows the results of an experimental test when the system works with a large duty cycle (around 86%) before OCF occurrence. As illustrated in Figure 11, the OCF is detected in $13\mu s$ and the system has been perfectly reconfigured.

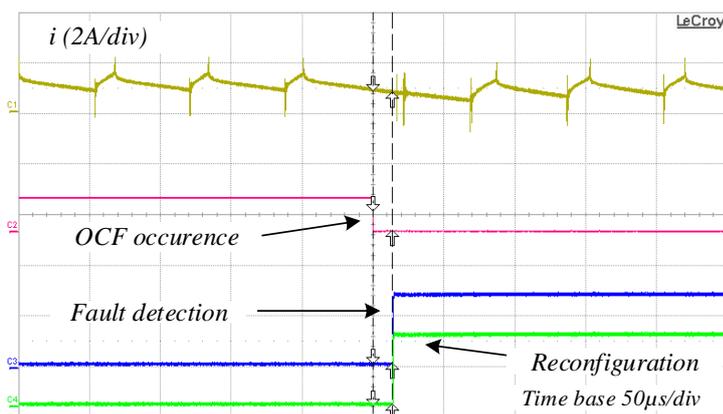


Figure 10. Detection of an OCF when the duty cycle is small - experimental results

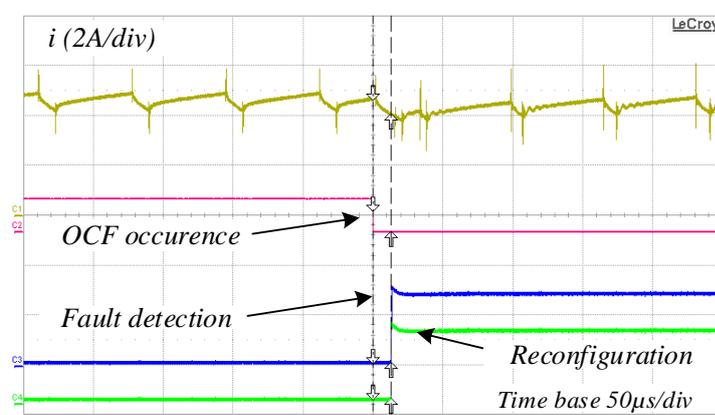


Figure 11. Detection of an OCF when the duty cycle is large - experimental results

4.2 SCF detection

A last experiment has been realized to validate the proposed method in the case of a SCF as shown in Figure 12. In the experimented scenario, the SCF is detected through the FDA in $18\mu s$.

Contrary to the case of an OCF, the system reconfiguration is not realized directly after the fault detection. As expected, the system waits the fuse breaks before being reconfigured. As it can be seen in Figure 12, the current increases, and when a fall in the current is detected the redundant leg is activated.

It should be noted that because of the used converter structure (provided by SEMIKRON), inserting a fuse in series with the main switch is impossible. Consequently, short circuit faults are generated "artificially" by means of the switch command as shown in Figure 2. To do this, the main switch is kept on by forcing the switch command generated by control loop ' u ' to '1'. Thus, the fuse is emulated by means of FPGA programming. For this, $500\mu s$ after SCF generation or when the current i passes the defined limit, the switch command u which has been

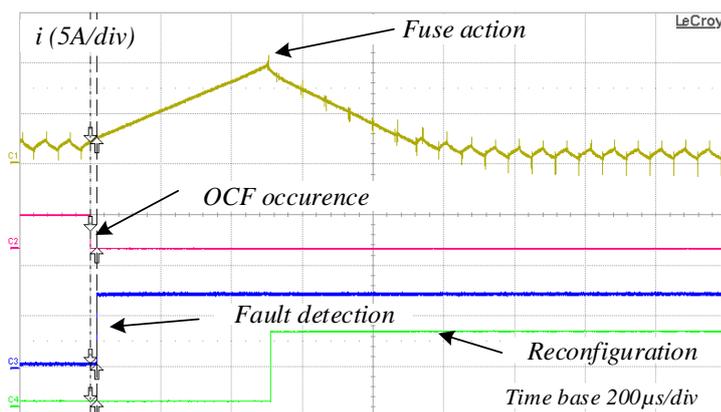


Figure 12. Detection of an SCF - experimental results

artificially set to '1' is reset to '0'. This reset to '0' imitates the fuse breaking and therefore, the end of permanent switch short circuit.

As already observed through HIL and experimental results, after the fuse breaks the system comes back to its initial operating point after some required time for the current to decrease (a little more than the $500\mu s$ because of the duty cycle limitation).

5. Conclusion

This paper deals with the study of a switch fault tolerant converter which is particularly dedicated to boost converter. Nevertheless, it can be also applied to DC-DC non-isolated single switch converter family such as buck, buck-boost, Cuk, SEPIC, and dual SEPIC converters. The proposed fault detection algorithm is based on the observation of the sign of the inductor current slope. This algorithm can detect and identify both types of switch failures: open-circuit and short-circuit faults. Thanks to FPGA implementation and efficiency of the proposed FDA, the switch faults can be detected in less than one switching period.

To improve the robustness of the FDA, some constraints have been considered:

- The dead times and delays in the system are calculated (and verified experimentally) and compensated to reduce the detection time.
- The duty cycle is limited to avoid any false fault detection during load variation and to cover the incapability of fault detection in small (or large) duty cycles.

Although, the second constraint reduces the system control response to the load variation, but it increases the robustness of the fault detection. Note that the proposed FDA does not need any additional current or voltage sensors.

Then a fault tolerant topology based on redundancy is proposed. An extra switch is considered for redundancy. Once a fault is detected, two possibilities are considered for the system reconfiguration:

- In case of an OCF, the system can be reconfigured immediately after the fault detection.

- In case of a SCF, the reconfiguration must be performed after the faulty switch isolation which requires a very fast fuse in series with the main switch.

Then, in order to confirm the validity of the proposed FDA and fault tolerant topology, a DC-DC boost converter has been built for this study. HIL and experimentation results show that the OCF is detected in $14\mu s$ and the SCF in $18\mu s$ (less than one switching period). As illustrated, system reconfiguration is performed immediately after fault detection in case of OCF. But for SCF, reconfiguration has to wait for the fuse action (around $500\mu s$). The fault-tolerant converter continue to operate, after reconfiguration, in the same condition as in healthy.

The proposed method is one of the best in term of real time fault detection in both OCF and SCF cases in comparison with other methods from the literature.

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