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Design and implementation of a new digital automatic gain control

E. Tisserand and Y. Berviller

This work describes and tests a new design method of an all-digital automatic gain control easy to implement. The discretization of the instantaneous gain provides a recursive form that merges the exponential function with the level detection. The first proposed circuit is well adapted for a software implementation. It comprises a simple control loop and two multipliers. It does neither contain digital filter nor divider and its setting only requires a loop gain parameter. Some tests were conducted on real digital audio signals with a dynamic range of 80 dB and they validate this approach. Under some conditions, the second circuit can even be simpler since it requires only one multiplier. It is well adapted to an FPGA implementation for high speed signal processing.

Introduction: Automatic Gain Control (AGC) is used in all applications that requires the processing of wide dynamic range signals (Acoustics, Imaging, Telecommunications, Digital Audio Broadcasting, Radar ...). The purpose of this function is to equalize the level of the output signal whatever the level of the input signal. An ideal AGC obeys the following equation

$$y(t) = Y_{ref} \frac{x(t)}{X_{rms}} \quad (1)$$

Where X_{rms} is the RMS value of the input signal $x(t)$ computed over a chosen duration and Y_{ref} a positive factor corresponding to the desired level for the output signal $y(t)$. In order to avoid the use of a divider that would seriously reduce the processing speed, most analog or digital methods use a Variable Gain Amplifier (VGA) controlled through a feedback loop (Fig. 1).

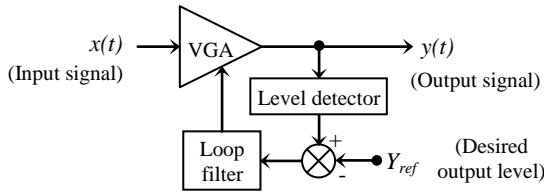


Fig. 1 Simplified block diagram of a feedback AGC

The numerous proposed solutions [1] vary according to the detection type (envelope, square law, true RMS, log), the loop transfer function or the VGA structure that is used. Since more than two decades, researchers and engineers develop digital AGC [2-3]. Kim and Im [4] propose a low cost version that requires the computation of the average output power. To overcome this diversity of solutions and to simplify the design phase, we propose a new all-digital method that needs no level detector. It implements a reduced number of parameters in a solution that is optimized for fast processing architectures.

Principle: Let $g(t) = \frac{y(t)}{x(t)}$ be the instantaneous gain of the VGA

According to (1) we can write $h(t) = \frac{1}{g(t)} = \frac{X_{rms}}{Y_{ref}}$

X_{rms}^2 is estimated by the short-term square mean of the signal so that $h^2(t)$ can be determined by the diagram given in Fig. 2.

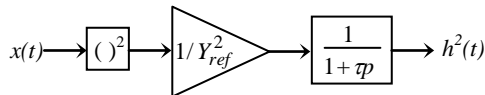


Fig. 2 Estimate of the reciprocal of the instantaneous gain

τ is the filter time constant and p is the Laplace transform variable. This diagram obeys the following differential equation

$$\tau \frac{d(h^2(t))}{dt} + h^2(t) = \frac{1}{Y_{ref}^2} x^2(t)$$

That can also be written as

$$\frac{d(h^2(t))}{h^2(t) dt} = \frac{1}{\tau} \left[\frac{1}{Y_{ref}^2} \frac{x^2(t)}{h^2(t)} - 1 \right]$$

Finally the instantaneous gain of the VGA can be expressed as

$$\frac{d(g(t))}{g(t) dt} = - \frac{d(h(t))}{h(t) dt} = - \frac{1}{2\tau Y_{ref}^2} (y^2(t) - Y_{ref}^2) \quad (2)$$

Within a constant factor, the solution of (2) is given by

$$g(t) = \exp \left[K \int_0^t (Y_{ref}^2 - y^2(t)) dt \right] \quad (3)$$

with $y(t) = g(t) \cdot x(t)$ and $K = \frac{1}{2\tau Y_{ref}^2}$

The AGC that uses this feedback loop is shown in Fig. 3.

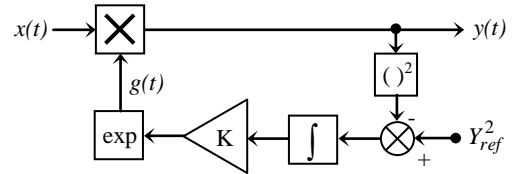


Fig. 3 Proposed analog feedback AGC

Digital version: the input signal sampled at a period $T_s = 1/F_s$ provides the samples x_k . Let y_k and g_k be the digital output signal and the instantaneous amplification factor respectively. A discrete version of (3) can be provided by

$$g_k = \exp(z_k) \text{ where } z_k = KT_S \sum_{n=0}^{k-1} (Y_{ref}^2 - y_n^2)$$

The numerical integration can be computed in a recursive way

$$z_k = z_{k-1} + KT_S (Y_{ref}^2 - y_{k-1}^2)$$

Thus we can also compute g_k according to a geometric progression

$$g_k = g_{k-1} \cdot \exp(KT_S (Y_{ref}^2 - y_{k-1}^2)) \quad (4)$$

In practice the reference level Y_{ref} is chosen to be equal to 1 and the time constant τ is much greater than T_s

In this case we have $KT_S = \frac{T_s}{2\tau} = d \ll 1$

The common ratio of g_k can thus be approximated by its first order Taylor development

$$\exp(KT_S (Y_{ref}^2 - y_{k-1}^2)) \approx 1 + d(1 - y_{k-1}^2) \quad (5)$$

With those approximations, we obtain the diagram of the digital AGC in Fig. 4.

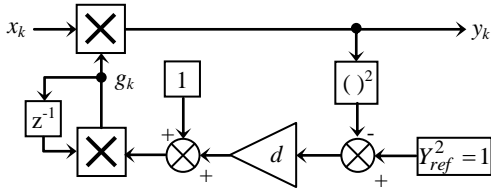


Fig. 4 Proposed digital feedback AGC

This diagram neither requires digital filter nor divider. Its setting only requires the determination of the factor d . In the case of a low level input signal, the common ratio of g_k equals $1 + d$ for each sample period which corresponds to a rising rate of about $8,68dF_s = 8,68/2\tau$ dB/s. The falling rate is much faster. Fig. 5 shows the output signal when the input is a 1 kHz unitary amplitude sinusoid with an attenuation of 60 dB in the time interval from 1 to 4 s. Here $d = 10^{-3}$ and $F_s = 44100$ Hz hence a gain variation rate of 380 dB/s.

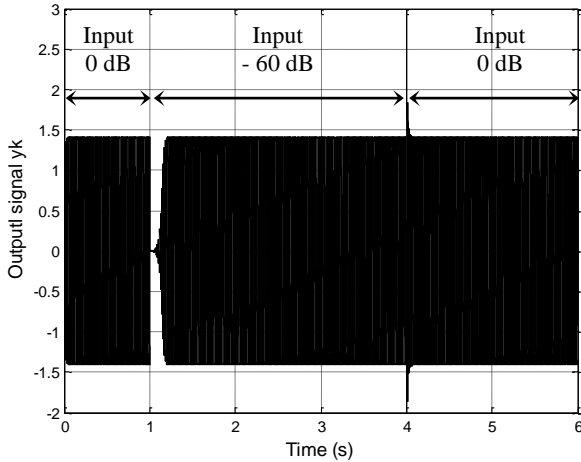


Fig. 5 AGC response to a 1 kHz signal with a 60 dB attenuation

Audio tests results: in order to validate the system with real signals we supplied it with a digital music sample (PCM 16 bits, 44100 Hz) with various attenuation factors. This signal starts with a silent phase of about 1.5 s. The parameter d is fixed at 10^{-4} ($\tau = 0.11$ s) this ensures that no audible distortion is added. The output signals corresponding to an input signal attenuated by 40 and 80 dB are plotted in Fig. 6.

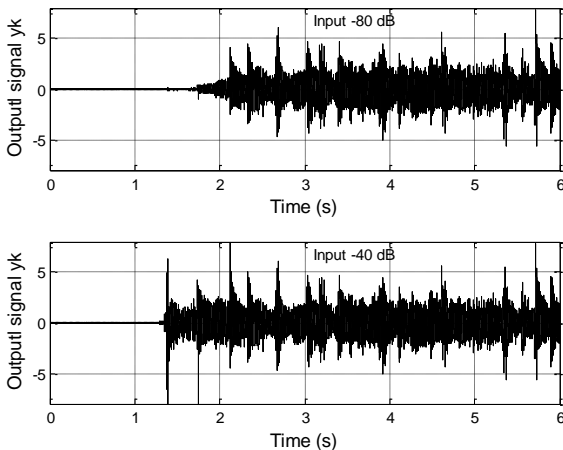


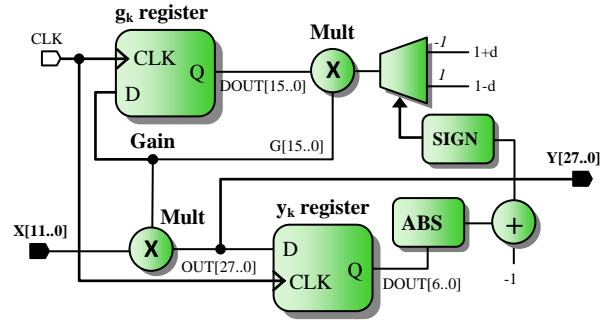
Fig. 6 AGC output signals for -40 dB and -80 dB input signals

With the chosen value of τ , the gain rising rate is about 39 dB/s.

FPGA Architecture implementation: with the aim of an FPGA implementation, a simpler alternative is proposed by substituting (4) with

$$g_k = g_{k-1} \cdot (1 + d \cdot \text{sign}[\text{abs}(y_{k-1}) - 1]) \quad (\text{corrected equation})$$

The whole system can then be synthesized by means of the digital architecture depicted in Fig. 7.



(corrected and improved figure)

Fig. 7 Digital architecture of our AGC

This scheme shares some similarities with the one published by Kim [4]. Since the level detector of the signal is no more needed, our system is both simpler and faster. For comparison purposes, we made two implementations (ours and Kim's one) on a low-cost FPGA (Altera Cyclone V 5CEBA2F17A7). The results are given in Table 1. In the particular cases where d is chosen as a negative integer power of two, one of the two multipliers becomes a right shift operator that requires no FPGA resources (only routing) combined with an adder-subtractor.

Table 1: Performances comparison of two digital AGC

	Logic cells (ALM)	Flip-Flops	DSP blocks	Max clock (MHz)
Our AGC	15	16	2	91
Kim's AGC	43	67	2	60
Difference (%)	-65	-76	0	+52

Conclusion: the instantaneous gain of an ideal AGC can be expressed as a single differential equation whose general solution requires an exponential function and the square of the output signal. The discretization of this gain introduces a recursive expression that can be simplified in order to merge the exponential function and the output signal level detector. The first proposed diagram is well adapted to a fast software implementation. It needs neither digital filters nor dividers. Its setting requires only choosing the loop gain that also impacts the response time of the system. Tests provided with a digital sound that has a dynamic range of 0 to -80 dB show a low distortion in steady state and an inaudible quick transient. Finally we propose a second version that is optimized for a fast and small hardware implementation.

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