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# FPGA Implementation of UWB-IR impulse generator and its corresponding decoder based on discrete wavelet packet

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## Abstract

In this paper, we propose an IR-UWB pulse generator and its corresponding decoder using respectively inverse discrete wavelet packet transform (IDWPT) and the discrete wavelet packet transform (DWPT) with various wavelets (Haar, Db2, Db4, Coif2, rbio1.5). These architectures being based on FIR filters, polyphase structure were chosen to easily suit in FPGA because of their parallel structures. The interpolator and decimator filter has been optimized using multiplexers to improve the delay, further the N-tap filter is divided into N/2-tap filters in parallel. The result comparisons in terms of BER has been shown for all wavelets through a Gaussian channel transmission. The results confirm the same transmission quality due to the perfect reconstruction property between the proposed IDWPT and DWPT implementation whatever the wavelet types that can be associated with sensors. We designed architectures of receiver and transmitter based on studied wavelets and we implemented them in FPGA to visualize generated pulses by experiences. The proposed FPGA implementations of IDWPT and DWPT architectures for Haar wavelet only require 3888 LUT/740 FF and 5359 LUT/996 FF, respectively, while providing low power consumption. The hardware and timing comparisons with existing techniques prove that our architectures are better. Our proposal permits a low complexity and good performance. Indeed, in transmitter part, one block can simultaneously generate pulses and modulate them. In receiver part, we replace a correlator used in a traditional IR-UWB system and generally complicated by our simple architecture.

**Keywords:** wavelet, FPGA, IR-UWB

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## 1. BACKGROUND

Ultra wideband impulse radio (UWB-IR) communication, included in the IEEE 802.15.6 norm, allows the robustness for Wireless Sensor Networks and offers lots of advantages like high data rate, less path-loss, better immunity to multipath propagation and low power spectral density considering the intrinsic characteristic of very short impulse transmission [1] - [4]. However, it presents also some drawbacks such as pulses synchronization and/or recognition at the reception part, interference coming from multiple access and the high system complexity.

Methods to generate an impulse found in the literatures are straightforward but the design of receiver's architecture is problematic. There exist two kinds of receivers, coherent and non-coherent [3]. Among coherent receivers, the UWB-IR Rake receiver provides good performance though

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requiring accurate channel estimation [4]. Consequently, this increases the system complexity even though it allows good performance [5].

Furthermore, non-coherent receivers do not need channel estimation [6] permitting low complexity and low power consumption, nevertheless they offers low performance compared to Rake receivers [7].

Actually, most of receivers' architectures are based on correlator and energy detection functions designed on ASIC technologies [8]. Some works studying the wavelet packet transform for communication as [10] or [11] give all applications for wavelets. The DWPT and/or IDWPT are mainly used for Wavelet Packet Modulation (WPM) to do multiple access with different packets and replace OFDM system [12], [13], [14], for Wavelet Division Multiple Access (WDMA) [15], or to substitute sine and cosine carriers in BPSK modulation [18]. We also find them in cognitive radio for dynamical spectrum allocation [16], [17], or to replace FFT blocks in OFDM [19].

In this paper, we propose a new architecture of pulses' generators based on IDWPT and its symmetric architecture, DWPT, to decode these pulses. More precisely, our embedded communication system performs DWPT/IDWPT for carrier-less communication and offer a modern ultra-wideband impulse radio communication suitable for wireless sensors network.

Nowadays, few works propose an implementation of DWPT/IDWPT targeted for the FPGA technology [9]. That is why we propose a complete study of our proposed original transmitter and receiver architectures, tailored to FPGA technology. The symmetric and regular structure allow us to modify the wavelet by the configuration of the sensor number. Compared to previous work, our approach permits to get a higher data rate, consuming less power and utilizing less logical resources while maintaining higher flexibility.

The paper is organized as follows. The next section briefly introduces the communication medium based on wavelets and the section 3 details our proposal RTL (Register Transfer Level) transmitter and receiver architectures. Section 4 presents wavelet packet transmissions simulations and MATLAB Simulink results for 5 common wavelets. The section 5 gives the FPGA synthesis results and experimentations. Finally, conclusion and future works are given in section 6.

## 2. WAVELET AS A DATA CARRIER

Previous works [5] - [19] allow either good performance with a high complexity or low performance with a low complexity.

We propose to design and implement on FPGA an IR-UWB system based on IDWPT and its corresponding decoder based on DWPT permitting a low complexity while maintaining good performance. The figure 1 gives an overview of the proposed IR-UWB system based on simple hardware entails low cost and low power consumption while reducing complexity in transmitter and receiver part traditionally based on pulse generator+modulator and correlator .

More accurately, the synthesis filter bank of Mallat's algorithm [20] transmit pulses and the analysis filter bank receive them. A brief introduction describing our approach can be found in [21] where the feasibility of the IR-UWB transmission based on behavioral simulations with the Db 4 wavelet is presented. This paper gives the optimized implementation and experimental results of the IR-UWB system based on polyphase structure filters chosen to easily suit in FPGA technology allowing the integration of parallel structures for several configurable wavelets (Haar, Db2, Db4, Coif2 and Rbio1.5). Our method provides multiple advantages. Architectures are simple because they are only based on FIR (Finite Impulse Response) filters. Basically, most of the wavelet based hardware filters are based on FIR filter but the architectures of IR-UWB transmitter's are commonly more complicated considering the required coherent receiver with correlator. However, our method provides multiple advantages considering the proposed architectures are low complexity and only

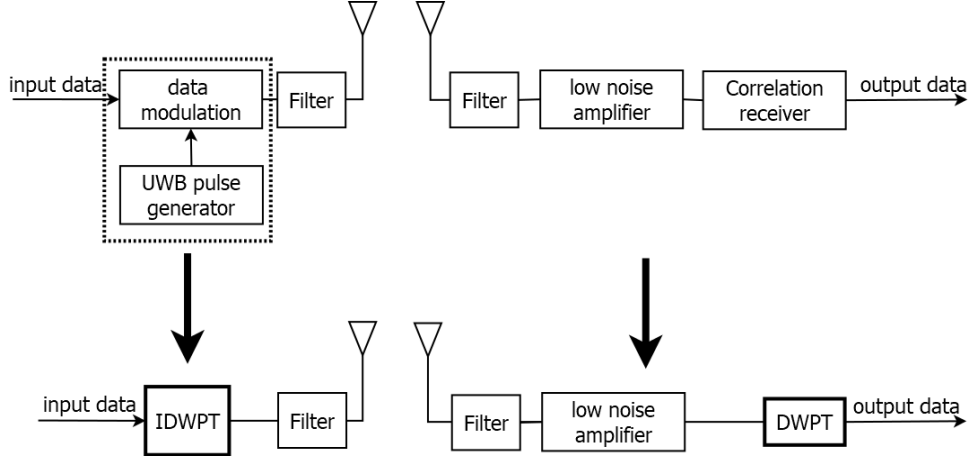


Figure 1: Traditional IR-UWB system and the proposed digital IR-UWB transmitter and receiver systems.

based on FIR filters to perform IR-UWB transmitter and receiver. Each input of the Mallat's filter bank generates its own wavelet packet, orthogonal to each others, hence allowing to identify the transmitter (i.e. the input) depending on the wavelet's shape. We also define two functioning modes [21]. In the "parallel mode", the architecture of the transmitter is the entire synthesis filter bank and every input is a data. In the "serial mode", one transmitter is composed by one branch of the entire architecture (a binary tree of filters). Consequently, in this mode, we can create a WSN formed by  $2^N$  transmitters (N being the depth of the filter bank, denoted level of resolution) and one receiver, all architectures being based on one wavelet (for the equivalency between transmitters and receiver). The architecture is based on one type of wavelet (allowing correspondence between transmitters and receiver). Therefore, only one type of wavelet is used but different packets are associated to this wavelet while wavelet packets are orthogonal and can be decoded with a single receiver. More precisely, there is one FIR filter and one up-sampler by level of resolution as illustrated in Fig. 2. For instance, in the Fig. 2, the sensor 1 and 8 transmit data with just three interpolated low pass and high pass filters, respectively.?

This approach of communication method, based on IDWPT and DWPT will be implemented on FPGA. By considering this targeted technology, a low power and reconfigurable architecture will be designed for a scalable solution. The following section presents the feasibility of this new communication method, the considered approach for the design and the implementation of DWPT and IDWPT architectures.

### 3. METHOD AND DESIGN APPROACH

Although the proposed study is mainly focused on transmissions' architectures, the wavelet selection while the channel is changed it is a very important and difficult tasks for sensors even though the channel can be common. However, the study of the signal at the DWPT part allows to measure the channel properties and to choose the wavelet accordingly. Basically, by knowing the transmission channel in advance, the type of wavelets can be selected in order to offer the best communication performance. We carried out simulations and experiences to validate the concept of the proposed communication method as follows:

- a functional simulation with MATLAB Simulink tool of the whole architecture (parallel mode) in order to get the BER vs  $E_b/N_0$  (energy per bit to noise power spectral density ratio) and to

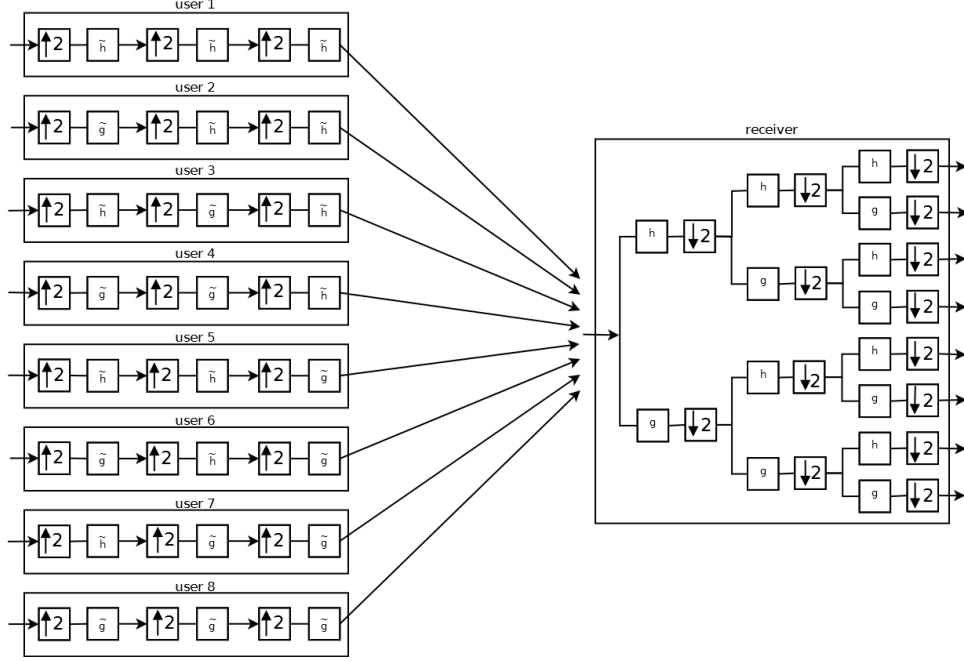


Figure 2: Architecture of transmitters and receiver with 3 levels of resolution for a WSN.

conclude about the impact of the wavelet packet used on the quality of transmission through an additive white Gaussian noise channel.

- the second one is a hardware behavioral simulation with Vivado tool to obtain synthesis results and to visualize wavelet packets for different levels of resolution;
- and a hardware implementation on Arty-7 FPGA board to test the data transmission and to validate the method. This experimentation bench includes an ADC (Analog to Digital Converter) and a DAC (Digital to Analog Converter), by using the XADC wizard to implement an ADC and a 16-bit DAC [28].

For a given wavelet, there are two couples of FIR filters with same length: one couple of filters for the transmission and another one for the reception. Every coefficients of these filters are already predefined [20] because we operate with common orthogonal wavelets.

As mentioned, the design of transmitter and receiver are exclusively based on FIR filters. Consequently, the structure of the filter influences directly the characteristics of our transmitter and receiver. We prefer the transposed form filter to the direct form filter. Indeed, the transposed form gives a response after one clock cycle whereas the direct form gives a response after  $N$  clock cycles (for a  $N$ -tap filter). Moreover, by using the polyphase structure of a filter, we can adapt the structure of the filter suitable for an FPGA implementation [22]. The process of simplification for a polyphase filter to fit in FPGA is started as follows:

$H$  is a causal FIR filter and its Z-transform is:

$$H(z) = \sum_{k=0}^{\infty} h(k)z^{-k} \quad (1)$$

By separating the even and odd parts in (1), we get:

$$H(z) = \sum_{k=0}^{\infty} h(2k)z^{-2k} + \sum_{k=0}^{\infty} h(2k+1)z^{-2k-1} \quad (2)$$

$$H(z) = \sum_{k=0}^{\infty} h_0(k)(z^{-k})^2 + z^{-1} \cdot \sum_{k=0}^{\infty} h_1(k)(z^{-k})^2 \quad (3)$$

$$H(z) = H_0(z^2) + z^{-1} \cdot H_1(z^2) \quad (4)$$

(4) is the equation of a polyphase filter with 2 branches. By knowing that our architecture is composed of interpolator filter (for transmitter) and decimator filter (for the receiver), there is an equivalency depicted in Fig. 3.

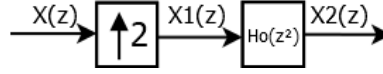


Figure 3: The first branch of interpolator filter.

$$x_1(n) = \begin{cases} x(\frac{n}{2}) & \text{if } n \text{ even} \\ 0 & \text{otherwise} \end{cases}$$

Another writing is:

$$x_1(n) = \frac{1 + (-1)^n}{2} x(\frac{n}{2}) \quad (5)$$

The Z-transform of expression (5) gives:

$$X_1(z) = \frac{1-z}{2} X(z^2) \quad (6)$$

Thus, we get:

$$X_2(z) = \frac{1-z}{2} H_0(z^2) X(z^2) \quad (7)$$

The equation 7 is illustrated by the Fig. 4:

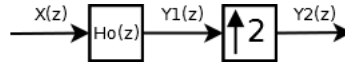


Figure 4: The first branch of the simplified interpolator filter.

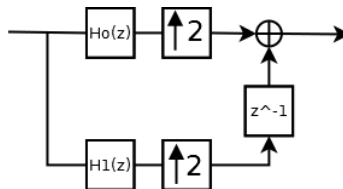


Figure 5: 4<sup>th</sup> step of simplification process.

In both branches of the Fig. 5, there are upsamplings, one sample from two is zero (in both branches). The second branch's samples are shifted by one beside the first branch. Consequently, the addition block takes sum with one zero sample alternately in two branches. Finally, we can

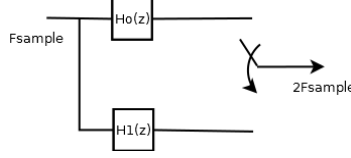


Figure 6: Last step of simplification process.

substitute two upsamplers and one adder by only one multiplexer as described in the Fig. 6. A similar simplification has been considered for the decimation filter. The Fig. 7 represents the proposed simplification for interpolator filters (a) and decimator filters (b) allowing an optimized FPGA implementation.

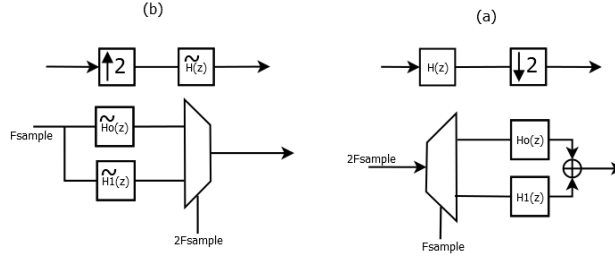


Figure 7: The proposed optimized architecture for interpolator filter (a) and decimator filter (b).

These optimization transform the architectures of the transmitters as presented in Fig. 8.

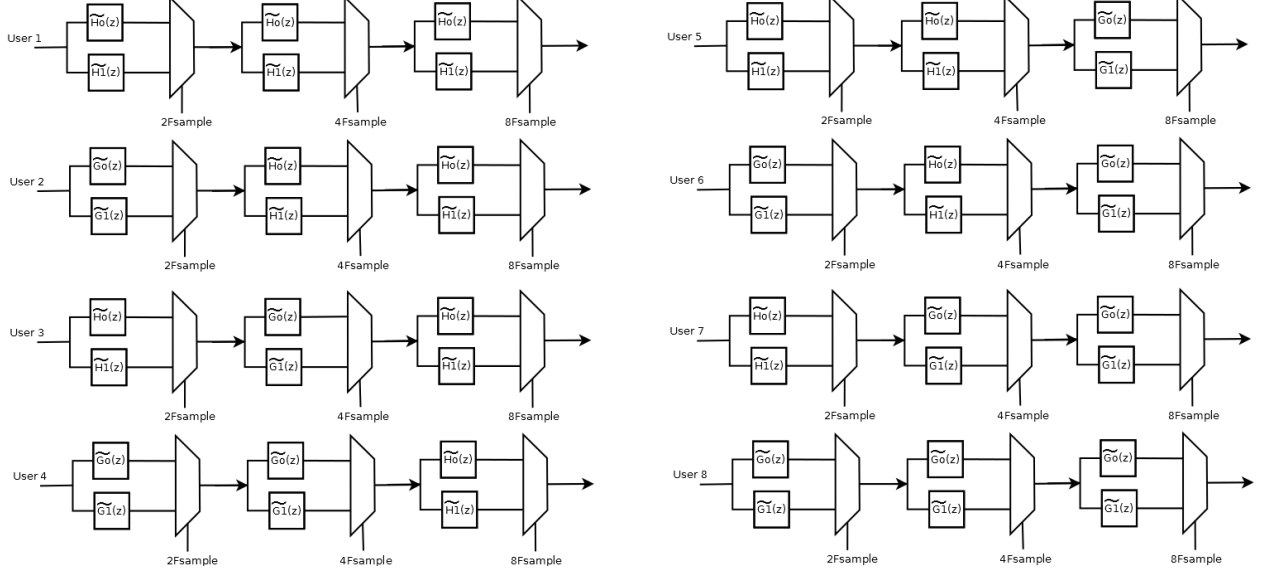


Figure 8: Architectures of transmitters for 3 levels of resolution with the proposed optimization.

These simplification allow us to get two  $\frac{N}{2}$ -tap filters in parallel instead of 1  $N$ -tap filter as in the scheme depicted in Fig. 9. Thereby, Fig. 9.(a) describes the low pass filter for the transmitter part (low pass reconstruction filter) while the Fig. 9.(b) details the low pass filter for the receiver part (low pass decomposition filter). Therefore, the proposed schemes for transmitter and receiver are symmetric.

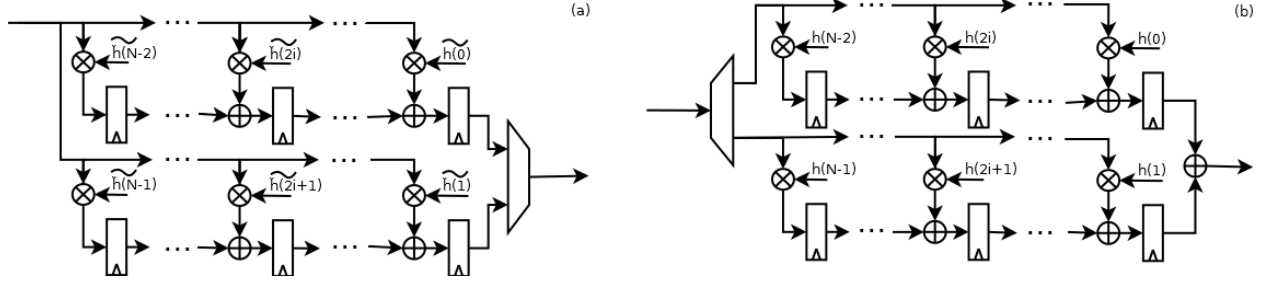


Figure 9: Schemes of N-tap filters for transmission (a) and reception (b).

#### 4. MATLAB Simulink simulations and results

This section analyses the communication performance of wavelets. For this purpose, simulations of the transmitter's and receiver's architectures through an Additive White Gaussian Noise (AWGN) channel for many wavelets (Haar, Db2, Db4, rbio1.5, coif2) are performed. An AWGN channel adds white Gaussian noise that affects the transmitted signal when it passes through the channel. This channel model contains a uniform continuous frequency spectrum over a particular frequency band [25]. The simulations are achieved under the MATLAB Simulink environment providing an AWGN model to determine the Binary Error Rate (BER) versus  $E_b/N_0$  [26]. Simulations' results are given and allow to define which wavelet is the most appropriate for an AWGN channel. The simulation with MATLAB Simulink using scheme depicted in Fig. 11 allows to view the BER according to  $E_b/N_0$  for a system with 3 levels of resolution and for different wavelets cited above. The sampling frequency is 1 GHz, coefficients and intern data are in fixed-point with 14 bits for decimal part considering in the real situation, FPGA technology can perform fixed-point data format and working with a high clock frequency even at 1GHz [33]. Simulations were carried out for WSN applications with Gaussian channel. In Fig. 11, the block "data emitted" is constituted of 8 different Bernoulli binary generators and the block "thresholding" contains 8 converters to binary data. All sensors generate a discrete wavelet packet associated to the used wavelet. Thresholds are set to 0.5 because this value is the mean value for the energy of signal. The block "BER calculator" calculates the binary error rate for 512 bits.

We firstly did simulations without the AWGN channel to obtain the reception delay in order to correctly calculate the BER. There is one Simulink model for each studied wavelet (Haar, Db2, Db4, Coif2, Rbio1.5). For each of them, the different reception delays are 1 clock cycle for Haar, 2 for Db2, 4 for Db4, 6 for Coif2 and 5 clock cycles for rbio1.5 wavelet. These values are due to the upsamplers at each level of resolution. With MATLAB Simulink, we determined the BER according to  $E_b/N_0$  for eight random binary data. The Figure 10 illustrates the BER for data1 (i.e. through 3 low pass filters), data2, data3, data4, data5, data6, data7 and data8 (i.e. through 3 high pass filters).



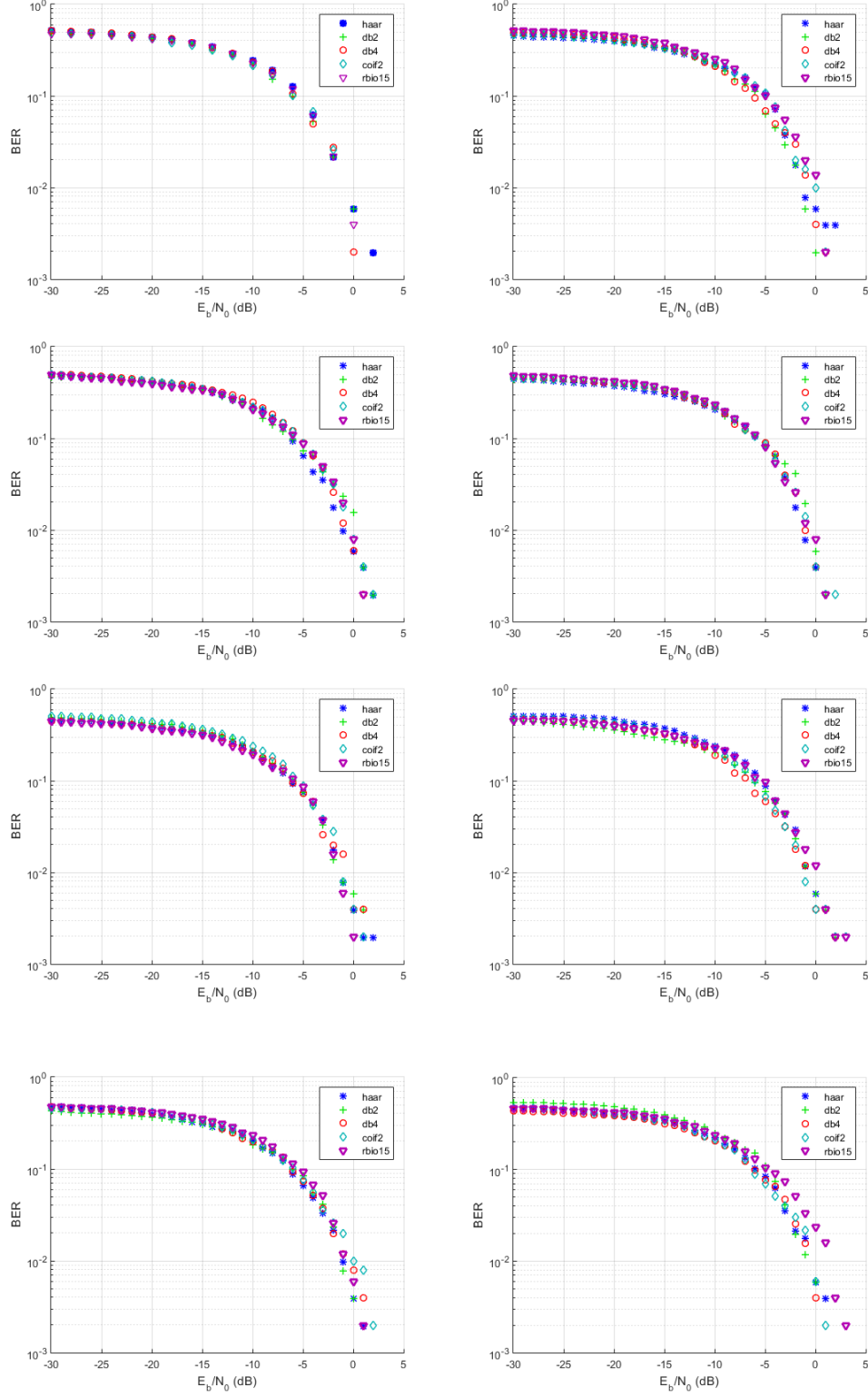


Figure 10: The BER vs  $E_b/N_0$  for data1 (top left), data2 (top right), data3, data4 , data5, data6, data7 (bottom left) and data8 (bottom right).

Considering the modeling and simulations results, we note that all BER versus  $E_b/N_0$  are very

close for eight sensors as well as five wavelets (Haar, Db2, Db4, Rbio1.5, Coif2). In other words, we got almost the same transmission quality for every wavelet used through an AWGN channel. The same BER results for each frequency band can be explained by the channel used, because the AWGN channel is non-selective on frequency and its spectrum is constant inside the bandwidth. Consequently, to get a good transmission quality, the choice of wavelet does not matter, when considering an AWGN channel. Hence we selected the simplest wavelet which is Haar wavelet. The synthesis results are given for every studied wavelet and implementations results are given for the Haar wavelet (the simplest) and Db4 wavelet (in order to give a prove of good working architecture even with another wavelet). That is why we focus on Haar and Db4 wavelets for the behavioral simulation and experimentations. Further, simulations have to be carried out for different channel's models, but we focus here on an implementation model suited for any wavelet, hence the nature of the transmission channel and the wavelet used do not constitute a key issue in the present work.

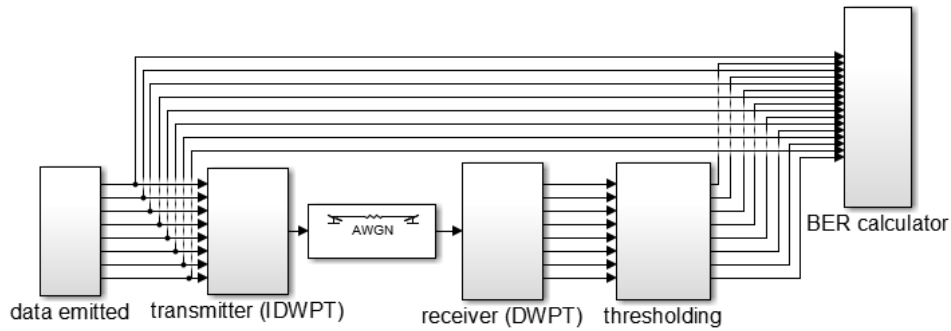


Figure 11: Simulated Simulink model.

## 5. Hardware implementations and results

The considered simplified structure of the decimation and interpolation filters are described in VHDL language (RTL structural descriptions). We have chosen to code the coefficients with 16 bits in fixed-point, 7 bits being reserved for the decimal part. The proposed architectures are flexible, allowing easy changes of the number of sensors (or the number of data inputs) by changing the level of resolution, the number of bits reserved to the fractional part and the wavelet by changing filters' coefficients.

The Table 1 gives the coefficients of low-pass and high-pass reconstruction filters corresponding to the studied wavelets.

To obtain coded coefficients, we transform the operation  $\tilde{h}(n) \times 2^7$  in hexadecimal coded on 16 bits,  $\tilde{h}(n)$  being real coefficients. To get simulations and implementations' results, we used a FPGA Arty-7 XC7A35T included in Arty board [23] under the Vivado 2015.2 software environment [24]. The considered clock frequency is 100 MHz. The following section presents synthesis results.

### 5.1. Synthesis results

RTL structural architectures of the transmitter and the receiver are given in the Fig. 12. In the Fig. 12 (a), "entree[i].resizing" permit us to convert input data from one bit to 16 bits for the good processing and to save inputs up while "clock" block generates and distributes clocks signals in each level of resolution. In the Fig. 12 (b), the two last stages allow to threshold outputs. It gives us the correct binary output data on the receiver.

Coeffs	Haar	Db2	Db4	rbio1.5	coif2	Coeffs	Haar	Db2	Db4	rbio1.5	coif2
$\widetilde{h}_0$	005B	003E	001D	0002	0002	$\widetilde{g}_0$	005B	FFEF	FFFF	0000	FFFE
$\widetilde{h}_1$	005B	006B	005C	FFFE	FFFB	$\widetilde{g}_1$	FFA5	FFE3	FFFC	0000	FFFB
$\widetilde{h}_2$		001D	0051	FFF0	FFF7	$\widetilde{g}_2$		006B	0004	0000	0009
$\widetilde{h}_3$		FFEF	FFFC	0010	0031	$\widetilde{g}_3$		FFC2	0018	0000	0031
$\widetilde{h}_4$			FFE8	005B	0068	$\widetilde{g}_4$			FFFC	005B	FF98
$\widetilde{h}_5$			0004	005B	0035	$\widetilde{g}_5$			FFAF	FFA5	0035
$\widetilde{h}_6$			0004	0010	FFF6	$\widetilde{g}_6$			005C	0000	000A
$\widetilde{h}_7$			FFFF	FFF0	FFF8	$\widetilde{g}_7$			FFE3	0000	FFF8
$\widetilde{h}_8$				FFFE	0003	$\widetilde{g}_8$				0000	FFFD
$\widetilde{h}_9$				0002	0001	$\widetilde{g}_9$				0000	0001
$\widetilde{h}_{10}$					0000	$\widetilde{g}_{10}$					0000
$\widetilde{h}_{11}$					0000	$\widetilde{g}_{11}$					0000

Table 1: Reconstruction low-pass and high-pass filters coefficients for Haar, Db2, Db4, rbio1.5 and coif2 wavelets.

Table 3 summarizes the synthesis results of the implemented transmitter and receiver according to the logic area requirement and to the power consumption for Daubechies level 4 wavelet and for different resolution levels. The FPGA implementation of IDWPT and DWPT architectures based on 3 levels of resolution only requires 1735 Flip-Flops/8177 Look-Up Tables and 1827 Flip-Flops/9361 Look-Up Tables, respectively. Furthermore, the power consumption are 294 mW and 330 mW, respectively. Thus, we get promising results about the interest of the proposed transmitter and receiver architectures which can be designed and integrated in embedded devices/sensors for wireless sensor networks.

We also obtained synthesis results for the purpose of getting area utilization, maximal clock frequency and power consumption for different wavelets and different resolution levels. All of these synthesis results are summarized in tables 2, 3 and 4. We note, when the resolution level increases, the power consumption and the area utilization increase while the clock frequency stays nearly constant. Actually, each added level of resolution increase the surface occupied almost twice because of added filters. More precisely, with N level there are  $2 \cdot (2^N - 1)$  filters while with one more level there are  $2^{N+1}$  additional filters. As we can expect, the Haar wavelet is less area-utilizing, faster and less power-consuming than other wavelets designed. Some of these synthesis results are not directly valid for IR-UWB networks considering the signal frequency is not in norms of this communication type. Nevertheless, by using a frequency shifting or a high clock frequency, the results prove that the proposed RTL architectures are applicable for IR-UWB networks. Furthermore, the area utilization and power consumption are suitable for IR-UWB networks by exploiting the proposed approach of transmitting data with discrete wavelet packets.

To conclude, with an AWGN channel, we only consider the Haar's wavelet. The MATLAB Simulink results indicate that we get the same BER results with AWGN channel for any wavelet used. Therefore, we choose the Haar wavelet. Nevertheless, we will also implement the Db4 wavelet for the reasons mentioned before.

## 5.2. Hardware simulations results

Fig. 13 details the transmission tests for the Db4 wavelet with 2 levels of resolution. It represents transmitted wavelet packets by each sensor in accordance with the established theory which is the proof of proper functioning of our architecture.

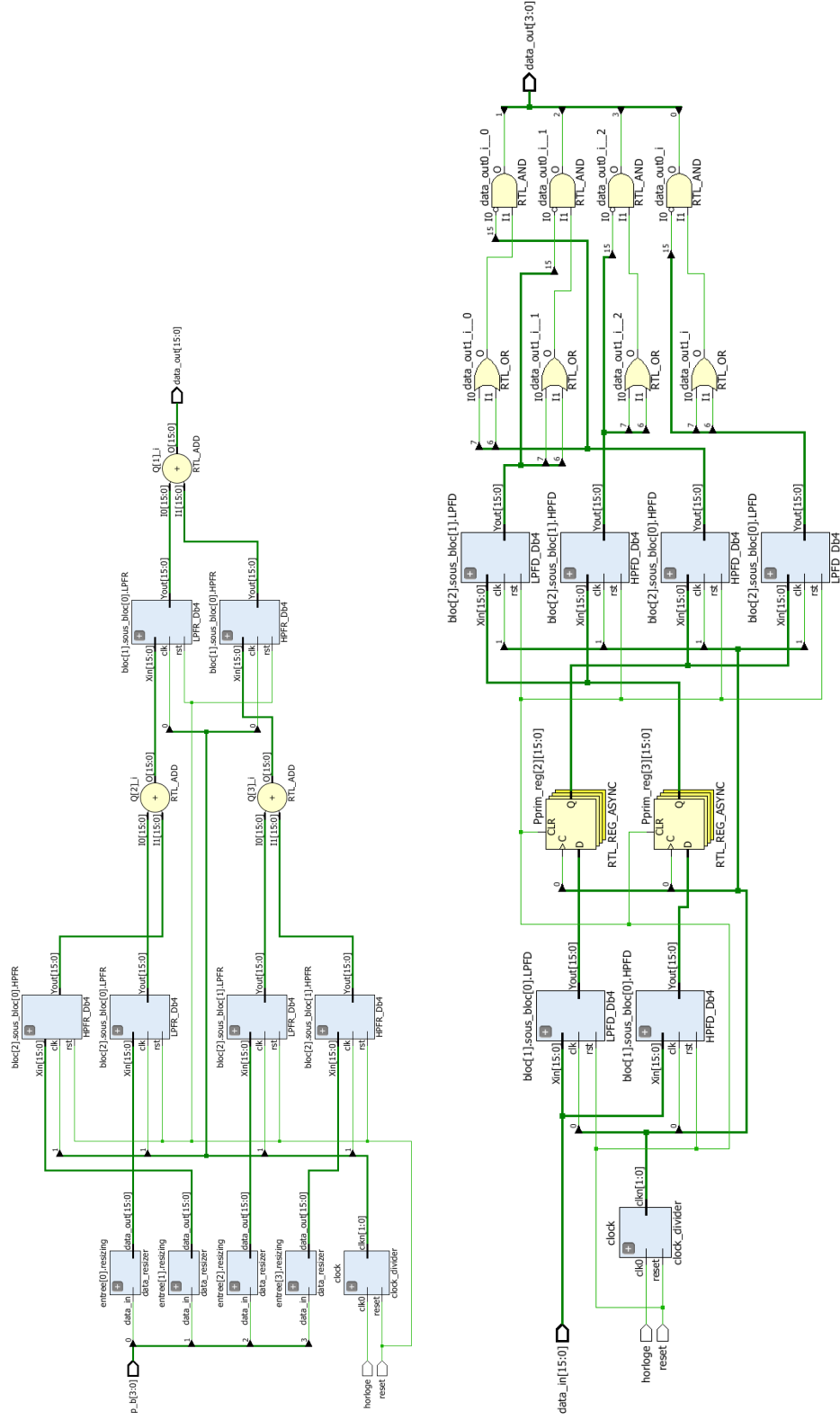


Figure 12: RTL structure of transmitter (a) and receiver (b) for 2 levels of resolution.

	Haar transmitter				Db2 transmitter			
Resolution level	1	2	3	4	1	2	3	4
FF	65	162	355	740	129	386	899	1924
LUT	260	779	1815	3888	653	1958	4566	9783
Power (mW)	147	159	179	218	152	179	233	342
Maximum clock frequency (MHz)	325	326	371	264	332	342	308	323
	Haar receiver				Db2 receiver			
Resolution level	1	2	3	4	1	2	3	4
FF	71	226	483	996	135	418	931	1956
LUT	359	1074	2502	5359	703	2106	4910	10519
Power (mW)	142	166	213	309	152	198	291	473
Maximum clock frequency (MHz)	373	388	372	388	272	344	353	376

Table 2: Ressource utilization and power consumption for transmitter and receiver based on Haar and Db2 wavelets.

	Db4 transmitter				Coif2 transmitter			
Resolution level	1	2	3	4	1	2	3	4
FF	242	740	1735	3724	337	1026	2403	5156
LUT	1057	3431	8177	17678	1161	4103	9985	21750
Power (mW)	155	201	294	478	158	213	323	546
Maximum clock frequency (MHz)	322	338	314	298	298	338	334	321
	Db4 receiver				Coif2 receiver			
Resolution level	1	2	3	4	1	2	3	4
FF	263	802	1827	3876	359	1090	2499	5316
LUT	1339	4014	9361	20059	1822	5462	12880	57597
Power (mW)	153	212	330	571	163	257	433	773
Maximum clock frequency (MHz)	420	359	372	388	256	273	172	163

Table 3: Ressource utilization and power consumption for transmitter and receiver based on Db4 and Coif2 wavelets.

rbio1.5 transmitter				
Resolution level	1	2	3	4
FF	239	734	1723	3700
LUT	460	1580	3818	8295
Power (mW)	151	175	220	310
Maximum clock frequency (MHz)	301	372	351	349
rbio1.5 receiver				
Resolution level	1	2	3	4
FF	263	802	1827	3876
LUT	1042	3122	7285	15603
Power (mW)	150	201	296	481
Maximum clock frequency (MHz)	280	345	229	174

Table 4: Ressource utilization and power consumption for transmitter and receiver based on rbio1.5 wavelet.

Figure 14 gives the Vivado behavioral simulation for Haar wavelet with 3 levels of resolution. We can see the inputs and output data at the transmitter's side and the output data at the receiver's

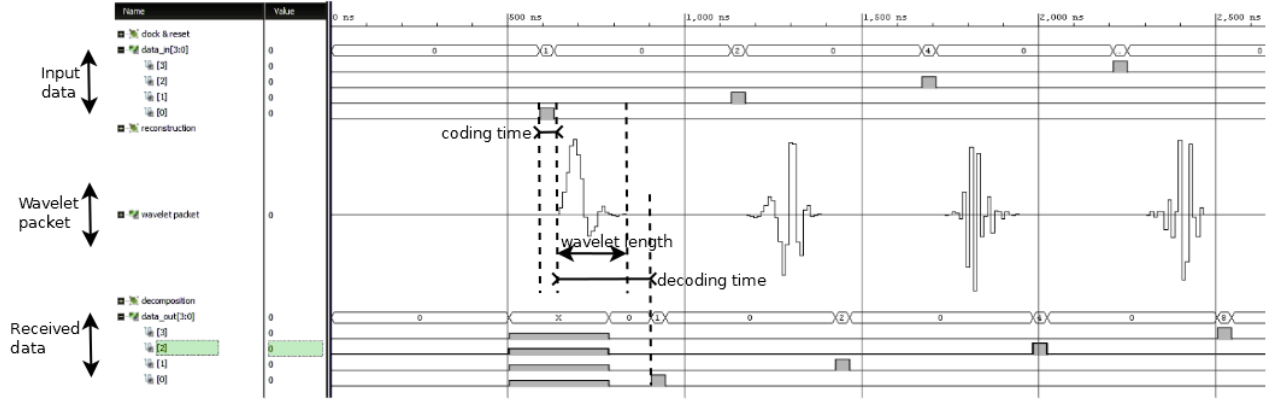


Figure 13: Simulation results for transmission of discrete wavelet packets associated to Db4 with 2 levels of resolution.

side. The wavelet packets visualized in the Fig. 14 has a width depending on wavelet, level of resolution and clock frequency. The used clock frequency is 100 MHz providing only wideband signals. By considering greater FPGA clock frequency, our scheme can provide IR-UWB signals. In that case, the architecture of transmitter based on IDWPT is an impulse generator that signals has the shape of wavelet packets. Indeed, the UWB-IR architectures transmit and receive efficiently discrete wavelet packets where received data correspond to transmitted data from the IDWPT.

Input data correspond to output data and wavelet packets obtain exactly the expected shape which is the proof of proper functioning of our architecture.

In the figure 14, we observe “primitive” Haar wavelet packets and a combination (at the the end of the transmission) transmitted (labeled P[1][31:0]) between transmitter and receiver with 3 levels of resolution’s architectures. For each data, there is 60 ns between the first time of detection and the start time of the wavelet packet. This time corresponds to “coding time”. In the same way, there are 180 ns between the time of detection of wavelet packet and the start time of decoded data. This time corresponds to “decoding time”. The reason of these values is the length of the datapath. Actually, there is one clock for each level of resolution and the frequency of each clock is divided by 2 between two successive levels.

The Table 5 summarizes the distribution of the clock in architectures. For the transmitter and the receiver, the level 1 is the level with less filters than others. Consequently, the level 1 is the last level for transmitter and the first level for receiver.

resolution level	1	2	3
name of clock	clockdiv(0)	clockdiv(1)	clockdiv(2)
clock period (ns)	20	40	80

Table 5: The clock distribution in the architectures for each level of resolution.

At the transmitter:

$$coding\ time = \frac{clockdiv(2)}{2} + \frac{clockdiv(1)}{2}$$

At the receiver:

$$decoding\ time = clockdiv(0) + 2 * clockdiv(1) + clockdiv(2)$$

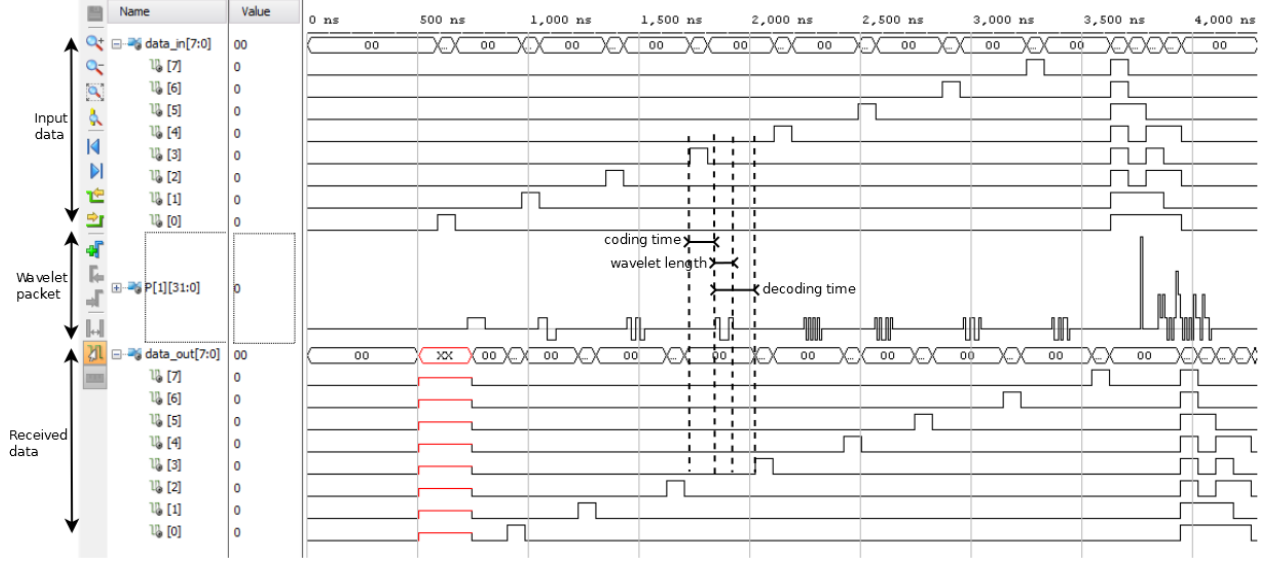


Figure 14: Visualization in Vivado simulator of transmitted data (datain), transmitted wavelet packet (P[1]) and received data (dataout).

An important point is the signal's frequency. For Haar wavelet and 3 levels of resolution, the frequency of the signal is 12.5 MHz. For Db4 wavelet and 2 levels of resolution, the frequency of signal is 4.5 MHz. All these values are valid for a 100 MHz initial clock frequency. We note that these values of signal frequency can only use IR-Wideband (IR-UWB) applications considering the low performance of the hardware setup used (arty 7 FPGA technology). Thus, these values of signal frequency is not directly valid for an IR-UWB signal because usually the signal frequency should be between 3,1-10,6 GHz. Nevertheless, Higher sampling rates and frequency transposition by considering a higher clock FPGA frequency can provide a higher signal frequency performing the UWB-compliant timings and frequencies. More generally, if clock period is  $k$  ns and  $N_S$  is the number of samples in the wavelet packets then:

- the coding time =  $\frac{4k}{2} + \frac{8k}{2} = 6k$  ns
- the decoding time =  $2k + 2 * 4k + 8k = 18k$  ns
- the signal frequency =  $\frac{1}{N_S * k}$

Nevertheless,  $N_S$  depends on the level of resolution ( $N_{lvl}$ ) and on the number of coefficients in the filter corresponding to the wavelet ( $N_{coeff}$ ). We want to express  $N_S$  according to  $N_{lvl}$  and  $N_{coeff}$  in order to generalize the signal's frequency. During simulations, we observed and measured the number of samples for several wavelets (Db2, Db4, Haar, etc.) and for different levels of resolution (from 1 to 4). These observations are saved in the table 6.

$N_{lvl}$	$N_S$
1	$N_{coeff}$
2	$N_S + 2(N_{coeff} - 1)$
3	$N_S + 2(N_S + 2(N_{coeff} - 1) - 1)$

Table 6: The number of samples measured according to the level of resolution for several wavelets.

From these observations, we conclude that there is a valid mathematical sequence to calculate the number of samples for each wavelet at each level. More accurately, we can set  $N_{lvl} - 1 = n$  and  $N_S = U_n$ . Thus, we get the following mathematical sequence:

$$\begin{cases} U_0 &= N_{\text{coeff}} \\ U_{n+1} &= N_{\text{coeff}} + 2(U_n - 1) \end{cases}$$

After some operations, we get the following expression that allows us to know the number of samples for a given wavelet packet at each level of resolution:

$$N_S = (2^{N_{lvl}} - 1)(N_{\text{coeff}} - 1) + 1 \quad (8)$$

We conclude that, for a given level of resolution, the Haar wavelet packets are smaller than the other wavelet packets and consequently, it gives us the fastest response and the highest signal's frequency. Moreover, we can note that all Haar wavelet packets begin by a positive high value (Fig. 14) whereas all other wavelets packets do not always begin by a positive value (Fig. 13 for Db4 wavelet packet). If we replace a high value by 1 and a low value by -1, packets transmitted could be written as in the table 7.

datain	packet transmitted
only 0 active	1 1 1 1 1 1 1
only 1 active	1 1 1 1-1-1-1-1
only 2 active	1 1-1-1 1 1-1-1
only 3 active	1 1-1-1-1-1 1 1
only 4 active	1-1 1-1 1-1 1-1
only 5 active	1-1 1-1-1 1-1 1
only 6 active	1-1-1 1 1-1-1 1
all active	8 0 0 0 0 0 0
0, 1 and 5 active	3 1 3 1-1 1-1 1
0, 1, 2, 3 and 4 active	5 3 1-1 1-1 1-1
0, 2 and 4 active	3 1 1-1 3 1 1-1
only 7 active	1-1-1 1-1 1 1-1

Table 7: Sampled Haar wavelet packets transmitted according to each data as illustrated in figure 14.

The last fact permits us to detect easily the Haar packet because it always begins with a high value (between 1 and 8). Furthermore, the sum of all samples of any Haar packet is 0 or 8 for 3 levels of resolution, more generally, 0 or  $2^{N_{lvl}}$ .

*Proof.* Any transmitted Haar packet is a unitary linear combination of “primitive” packet and is written:

$$S = \sum_{j=0}^{2^{N_{lvl}}-1} \sum_{i=0}^{2^{N_{lvl}}-1} a_i \cdot p_{ij}$$

with:  $\forall i \in \llbracket 0, 2^{N_{lvl}} - 1 \rrbracket$ ,  $a_i = 0$  or  $1$ ,  
 $\forall (i, j) \in \llbracket 0, 2^{N_{lvl}} - 1 \rrbracket^2$ ,  $p_{ij} = 1$  or  $-1$  (see table 7).



$$S = \sum_{i=0}^{2^{N_{lvl}}-1} \sum_{j=0}^{2^{N_{lvl}}-1} a_i \cdot p_{ij} \quad (9)$$

$$= \sum_{i=0}^{2^{N_{lvl}}-1} a_i \sum_{j=0}^{2^{N_{lvl}}-1} p_{ij} \quad (10)$$

$$\sum_{j=0}^{2^{N_{lvl}}-1} p_{ij} = \begin{cases} 2^{N_{lvl}} & \text{if } i = 0 \\ 0 & \text{otherwise} \end{cases}$$

$S = 2^{N_{lvl}} \cdot a_0$  but  $a_0 = 0$  or  $1$ ,  
 $S = 0$  or  $2^{N_{lvl}}$ . □

With this simple operation of summing of samples, we can quickly check if the packet received is correct or not and also verify if the packet 1 is included or not in the received packet (if packet 1 is included the checksum is always equal to  $2^N$ ).

### 5.3. Experimentation results

The architecture of the IDWPT for wavelets with 2 levels of resolution is implemented in the Arty board [23]. A 16-bit DAC [27] plugged in pmod connector permits us to convert the output wavelet packets into an analog signal. This analog signal is captured by an oscilloscope with a sampling frequency value of 1 GSa/s. The pmod DA3 utilizes Analog Devices AD5541A to provide analog output with 16-bits resolution [28]. This experimentation allows a visualization of wavelet packets on the IDWPT output architecture (as we can see in Fig. 18). If we compare the wavelet packets presented in Fig.15, 16 and 17 and the corresponding packets in the literature, we can see the proper functioning of our architecture. However, the 16-bit DAC has a maximum clock signal of 50 MHz. Consequently, our implementations provide us a 400 kHz signal frequency and are only to prove the feasibility of our proposal. We can consider this like a frequency shifting from 3,1 - 10,6 GHz to 400 kHz in order to use properly the DAC and visualize wavelet packets.

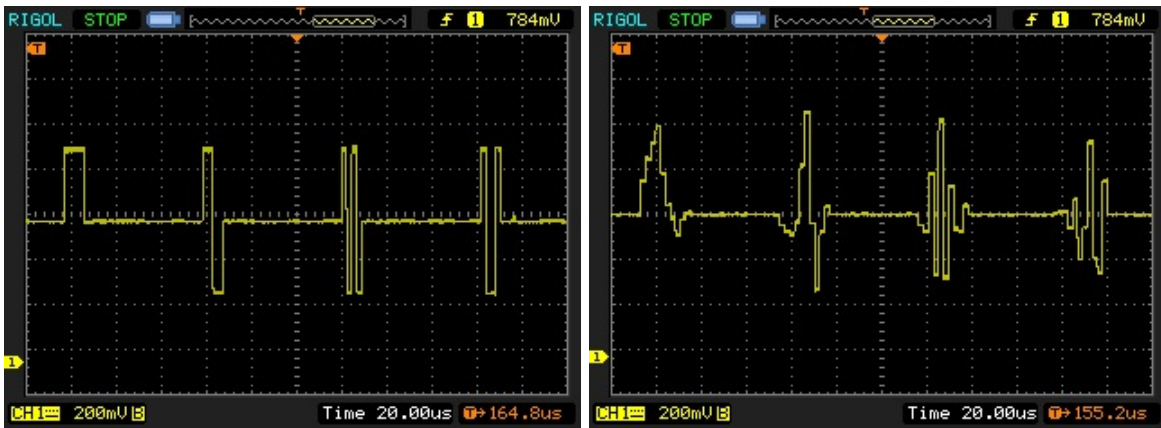


Figure 15: The visualization of transmitted packets by the IDWPT architectures on a FPGA Arty board (Haar wavelet at the left and Db2 wavelet at the right) and 2 levels of resolution.

The results for tested wavelet are presented in Fig. 16. We count the number of samples in each packet to compare it with the formula given in the previous subsection. There are 15 samples



Figure 16: The visualization of transmitted packets by the IDWPT architectures on a FPGA Arty board (Db4 wavelet at the left and Coif2 wavelet at the right) and 2 levels of resolution.

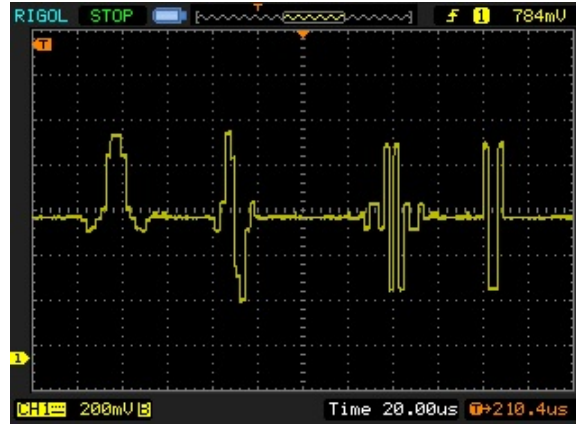


Figure 17: The visualization of transmitted packets by the IDWPT architectures with FPGA Arty board (rbio1.5 wavelet and 2 levels of resolution).

for the wavelet packets 1 and 4, and 16 samples for the others whereas with the formula we get 22 samples (as we can see in the behavioral simulation). This difference between theoretical and experimental results comes from the approximation of computing method. Actually, the fixed point method gives us a 0 value for some samples at the beginning or the end of pulse, that is why we cannot see all samples in scope.

#### 5.4. Discussions about the implementation

The Table 8 presents a comparison between existing implementations of Mallat's algorithm for discrete or continue wavelet transform. Since [9] dating back to 2002, there is no work about the implementation of the DWPT/IDWPT. We propose, an update with actual technology and a more accurate implementation report including resource utilization, maximum frequency and power estimation. We can find more implementations but we will limit the comparison to 4 studies. The topic in [30] is about the optimization of the implementation using a residue number system, while [31] use his implementation for image denoising. We should note that in the study [32], the fixed-point is 18 bits while we have 7 bits for fixed-point. We can conclude that we presented a more accurate implementation of a flexible DWPT and IDWPT for 5 most studied wavelets.

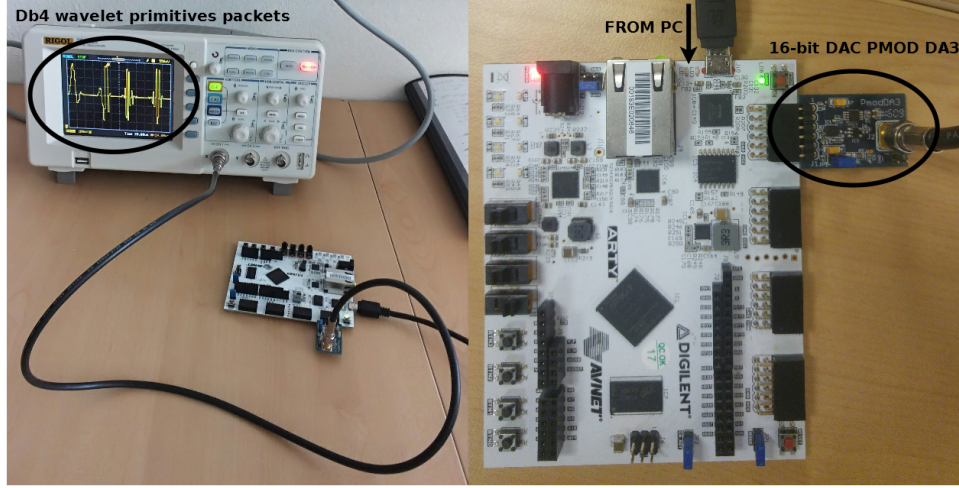


Figure 18: The experimentation with FPGA Arty board of the IDWPT architecture for Db4 wavelet and 2 level of resolutions.

	this work	[9]	[30]	[31]	[32]	
wavelet	Haar, Db2, Db4, Coif2, rbio1.5	8-tap and 4-tap filter	Db2	Haar	Db20	Db30
type	discrete	discrete	continue	continue	discrete	
level	1 - 4	3 - 10	2	5	1	
LUT	260 - 21750	200k - 950k gates	1261	586	35208	49165
FF	65 - 5156	1100 - 9500 slices	1643	1156	38655	57219
max freq. (MHz)	264 - 371	-	318,8	295,6	-	
power (mW)	147 - 546	-	127	-	-	
technology	artix-7	virtex-E	ZC706	cyclone V	artix-7	

Table 8: Comparison between other works in the literature.

In terms of the wide band impulsion, our IR-UWB system allows to provide narrower impulsions compared to previous works. For instance, considering one level of resolution wavelets, our architecture generates Db4 wavelet pulses of 37.2 ns.

## 6. Conclusion and future works

In this paper, we described a communication approach for wireless sensor networks based on impulse radio generated by an IDWPT and decoded by a DWPT scheme. Our architectures allow us to easily change parameters such as:

- the number of sensors depending on the resolution level (only in the serial mode) i.e. the number of inputs of the IDWPT block;
- and also the wavelet shaping packets for transmission and reception.

Actually, the regular and symmetric structure is a form of binary tree. Therefore, it is about only one parameter to characterize this regularity implying the facility to change the architecture (or network) size.

In summary, we proposed an optimized IR-UWB system based on IDWPT and DWPT with various wavelets and permitting a low complexity and good performance. Indeed, the proposed IR-UWB system based on logic hardware has been implemented in FPGA technology. In transmitter part, one block can simultaneously generate pulses and modulate them. In receiver part, we replace a correlator used in a traditional IR-UWB system by our simple architecture. Our embedded architecture is suitable for WSN where the reduction of transmitter's/receiver's size and the power consumption are the most important challenges.

As like in [22], we chose filters with polyphase structure to easily suit in FPGA because their structures are parallel. Moreover, this characteristic enhances the timing performance and reduces the area utilization by optimizing the filter's structure. We obtain good results for an AWGN channel. The AWGN channel has been considered to validate the architectures of pulses' emitter and receiver only, in order to ensure clean bases for further development. That's why this work only focuses on the architecture and its implementation on FPGA. Actually, WSNs introduce two main issues: 1) channel propagation and 2) power consumption. WSN common channels and how wavelet can help to facilitate gathering the multipath components are still under study. Power consumption of WSN is highly impacted by routing algorithms and medium access control layer (overlistening, overhead, etc.). This latter can be highly improved with our architecture which reduces the size of the packets and the wake up time (implicit addressing of sensors, parallel communications). In future work, we will study the data transmission when emitted pulses are mixed and through a multipath channel such as Rayleigh and Rician fading channels and Saleh-Valenzuela model. Thus, the implementation of the transmitter and receiver in the same FPGA and both in separate FPGA will allow to observe the influence of the clock synchronization between FPGAs. Nevertheless, radio resources allocations will become dynamic. About this dynamical resources management, we could choose a software management (dynamical allocation) or a hardware management (hardware reconfigurability). In this paper, we presented two processing modes, parallel and serial. To get a dynamical allocation of resources by proposing a possible solution, the hybrid mode (parallel and serial depending on the requirement of user) can be also studied. Moreover, we will study our architectures through others specific channel models.

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