Open-Switch and Open-Clamping Diode Fault Diagnosis for Single-phase Five-Level Neutral-Point-Clamped Inverters

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***Abstract*— In this paper, a fast and efficient open-circuit switch and clamping diode fault diagnosis for Neutral-Point-Clamped inverters is proposed. Multilevel converters employed in safety-critical applications should include fault tolerant capability, where fault diagnosis plays a vital role. The proposed fault diagnosis algorithm is based on failure mode analysis, which is a logic based approach. The required signals and measurements are available in the healthy control system. Furthermore, component modeling, load parameters and complicated calculations are not required. The fault detection and identification of the faulty switch or clamping diode are carried out based on the available data such as switching pattern and terminal voltage. Although switches are more fragile than clamping diodes, clamping diodes are also subjected to breakdown. Hence, it is also crucial to achieve a clamping diode fault diagnosis strategy. Moreover, for fault detection procedure, a voltage quantifier is proposed to avoid any misdiagnosis arising from measurement errors and voltage drop in the circuit. The simulation and experimental results are presented to validate the effectiveness of the proposed approach.**

***Index Terms*— Fault diagnosis, open-switch failure, open clamping diode failure, neutral-point-clamped inverter.**

I. Introduction

Multilevel converters have been increasingly used for decades in industry. Thanks to the key advantages such as less switching losses, less total harmonic distortion, limited voltage transients dv/dt, small size of filter elements and reduced common-mode voltage, multilevel inverters have become an appropriate substitute for two-level conventional ones [1], [2]. Since three-level neutral-point-clamped (NPC) inverters do not employ flying capacitors and isolating transformers, they are widely applied in industry. However, in high voltage applications, in a classical NPC inverter, several components and capacitors have to be cascaded which are supplied only by a single DC power source. In this case, due to different characteristics of the components (even with the same rating values fabricated by the same manufacturer), non equal voltage sharing would arise across the components while in NPC/H-bridge inverters, the single phase NPC modules are cascaded in each phase. In this case, each module has its own DC power supply. Thus, the voltage sharing would be improved. [3]. In order to tackle the mentioned problems of NPC inverters, NPC/H-bridge topology is proposed rather than NPC inverter. In a cascaded H-bridge inverter, some single phase modules are cascaded to achieve a certain number of voltage levels. Thus, compared with NPC, the voltage sharing is improved in a cascaded H-bridge inverter but higher number of DC power sources is required. Thus, for high voltage applications, an NPC/H-Bridge converter overcomes two main shortcomings of the classical NPC and cascaded H-bridge converters together. Compared with classical NPC inverters, the dynamic and static voltage sharing problems would be tackled and compared with cascaded H-Bridge inverters, it includes less DC power sources.

Compared with conventional two-level inverters, the NPC/H-bridge inverter, like other multilevel inverter topologies, is constituted of higher number of power semiconductor components which based on the field experiences are vulnerable to failures [4]. This matter may cause an increase in probability of occurrence of switch or clamping diode fault. Furthermore, for some applications such as aviation, automobile, offshore and ship propulsion, a timely fault diagnosis is of great concern to ensure the reliability of the power electronic converter [5]. For these reasons, identification of a faulty switch or clamping diode in an NPC/H-Bridge inverter is of considerable importance. Faults in power semiconductors are classified into short-circuit and open-circuit. Although the short-circuit fault has a more destructive effect, it can be canceled immediately by the protective circuits and elements as implemented in [6] and [7]. In contrast to short-circuit faults, open-switch faults subsist in the system without detection. Secondarily, open-switch fault leads to current distortion which has significant impacts such as induced torque ripples and vibrations in electrical motors

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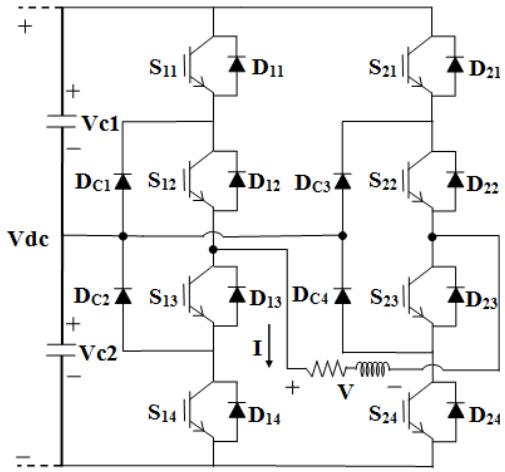

Fig. 1. Scheme of a single phase NPC/H-bridge inverter.

[8]. On the other hand, once the short circuit fault is eliminated by the protective devices such as fuses, the short circuit fault is transformed to an open circuit fault. Hence, this paper deals with open-circuit fault diagnosis. In addition to power switches, it should be noted that in the NPC/H-bridge inverter, the clamping diodes also play a vital role to make some terminal voltage levels. Moreover, the clamping diodes are subjected to the open-circuit fault and are not immune to the fault occurrence. Consequently, open-circuit fault diagnosis in clamping diodes should be taken into consideration as well, which is often overlooked in many studies.

In [9], the authors propose a fault diagnosis method for a T-Type inverter. Based on the average of the phase currents the faulty half-leg is identified; afterwards, by analyzing the voltages of the DC link capacitors, the faulty switch is pinpointed. The research work presented in [10] deals with the fault localization in a flying capacitor inverter. The proposed localization is carried out by monitoring the state of charge the flying capacitors and knowing the switching states generated by the modulator. In [11], the authors propose a localization method for a T-Type inverter. In this method, the current injected to the neutral point and the three pole voltages are measured. The fault localization is accomplished within some tens of ms. Based on the measured currents and the switching state generated by the modulator, the fault diagnosis is accomplished. The switching states are determined based on the three pole voltages. In [12], using neural networks, a faulty switch is identified in a single phase NPC inverter. This research work assumes that the clamping diodes are unbreakable. The fault localization is carried out within some tens of ms. The authors in [13] propose a voltage reference residual based fault diagnosis approach for three-level NPC inverters. To realize this strategy, the voltage across each DC link capacitor and AC side currents should be measured. Furthermore, the resistance and capacitance of the DC link capacitors are required. Reference [14] concerns a current based fault diagnosis approach for three-level NPC inverters. This approach is realized by analyzing the slope of the phase current trajectory. This strategy does not investigate fault event in clamping diodes. The authors in [15] propose a diagnosis method for an NPC inverter. By using the three-phase normalized current residual variables, the faulty switch is identified. In this research work, the clamping diodes are assumed unbreakable. In [16], a combined model-based and data processing fault localization strategy for a grid-connected NPC inverter has been proposed. To accomplish the proposed fault diagnosis, measurement of the line currents and gird voltage is necessary. Furthermore, the presented modeling of the inverter relies on the resistance and inductance values of the ac-side filter. Fault event in clamping diodes is not examined in this research work. The authors in [17] propose a fast fault diagnosis method based on failure mode analysis. However, in case of fault event in a clamping diode, this strategy is no longer valid. Indeed, in the current research work, the authors have developed the research presented in [17] by considering the fact that the clamping diodes are also subjected to fault occurrence. In [18], based on the Average Current Park's Vector, the phase and the switch pair including the faulty switch are identified in a three-phase three-level NPC inverter. This method cannot identify the defected switch in the faulty switch pair as well as a faulty clamping diode. The research work presented in [19] detects an open circuit fault event by examining the magnitude of the Average Current Park Vector (ACPV). Then, it identifies a faulty pair (faulty half-leg) by examining the angle of ACPV. Afterwards, by defining the threshold values corresponding to the positive and negative half cycles, it pinpoints the defected switch. In case of fault event in a clamping diode, the angle of ACPV has not been studied. Furthermore, defining the new threshold values is necessary. Hence, the authors of this research work have not investigated and demonstrated that their strategy is able to identify a faulty clamping diode. In [20], according to the possible current patterns, caused by an open-switch fault occurrence in a back-to-back three-phase three-level NPC inverter and zero current duration time, a defected switch can be pinpointed. However, the presented method is not able to detect a faulty clamping diode. Moreover, an estimation of the generator parameters is required. The diagnosis approach presented in [21] solely identifies the faulty phase in a three-phase three-level NPC inverter. Furthermore, external circuits are required to measure pole voltages. Open-switch fault diagnosis presented in [22] for three-phase three-level NPC rectifier is based on the pole voltage measurement. In this regard, the pole voltages are estimated from two line-line voltages (Vab and Vbc) which requires the line parameters to estimate the voltage values. Furthermore, the proposed strategy cannot identify the faulty clamping diode. In [23], faulty switch is localized based on the radius of the Concordia current pattern for three-level grid connected NPC inverters. The proposed method is not able to identify the defected clamping diode. Based on pole voltage measurements in [24], the faulty component is identified in a three-level NPC inverter. This strategy necessitates measuring the three pole voltages. In [25], six Rogowski coils are positioned in current paths of clamping diodes. By analyzing the currents measured by the coils, the defected switch is

TABLE I
CONDUCTING COMPONENTS CORRESPONDING TO EACH SWITCHING STATE FOR POSITIVE AND NEGATIVE OUTPUT CURRENTS DURING HEALTHY OPERATION

State	Terminal voltage	Conducting components (I>0)	Conducting components (I<0)
1	+Vdc	S11, S12, S23, S24	D11, D12, D23, D24
2	+Vdc/2	S11, S12, S23, DC4	D11, D12, S22, DC3
3	+Vdc/2	DC1, S12, S23, S24	DC2, S13, D23, D24
4	0	S11, S12, D22, D21	D11, D12, S21, S22
5	0	DC1, S12, S23, DC4	DC2, S13, S22, DC3
6	0	D14, D13, S23, S24	S13, S14, D24, D23
7	-Vdc/2	DC1, S12, D22, D21	DC2, S13, S22, S21
8	-Vdc/2	D14, D13, S23, DC4	S13, S14, DC3, S22
9	-Vdc	D14, D13, D22, D21	S13, S14, S22, S21

TABLE II
SWITCHING PATTERNS CORRESPONDING TO EACH VOLTAGE LEVEL

State	Terminal voltage	S11	S12	S13	S14	S21	S22	S23	S24	Decimal number
1	+Vdc	1	1	0	0	0	0	1	1	195
2	+Vdc/2	1	1	0	0	0	1	1	0	198
3	+Vdc/2	0	1	1	0	0	0	1	1	99
4	0	1	1	0	0	1	1	0	0	204
5	0	0	1	1	0	0	1	1	0	102
6	0	0	0	1	1	0	0	1	1	51
7	-Vdc/2	0	1	1	0	1	1	0	0	108
8	-Vdc/2	0	0	1	1	0	1	1	0	54
9	-Vdc	0	0	1	1	1	1	0	0	60

located. This method is not cost effective. In spite of observing the current flowing through the clamping diodes, the faulty clamping diode is not identified by this strategy. In the research presented in [26], by analyzing the characteristic of distorted current in case of open-circuit fault occurrence in three-level NPC converter, the faulty phase and switch group is identified. Afterwards, by injection of under excited current, the defected component is localized. By presenting mixed logical dynamic modeling of the single-phase grid-connected NPC/H-bridge converter in [27], the grid current is estimated. Thereafter, in case of all different open-switch faults, the generated residual values are analyzed to achieve the fault diagnosis. In the proposed approach, the grid parameters such as the equivalent inductor and resistance of the traction transformer are needed. In [28]-[30], the applied switch fault detection procedures have been surveyed and based on the performed investigation, an efficient fault detection method is proposed. However, choosing improper parameter values in the detection algorithm may result in wrong fault detection, due to system imperfections.

In this paper, a fast and efficient open-circuit fault detection and localization approach based on the failure mode analysis for a single-phase five-level NPC inverter is presented. In contrast to the current based methods ([18]-[20], [23], [25], [26], [27]), the proposed approach is remarkably fast since it is based on the failure mode analysis, which is a logic based method and does not require significant calculations. Furthermore, the presented strategy is able to localize any faulty switch as well as any defected clamping diode while the strategies proposed in ([12], [14]-[23], [25]) are not able to identify a faulty clamping diode. Moreover, complicated calculations and modeling presented in [25], are avoided here. It should also be noted that the proposed approach does not depend on the ac side parameters required in ([16], [22], [27]). Moreover, a voltage quantifier is devised for fault detection procedure to get rid of choosing a threshold value as presented in ([28]-[30]), which in turn prevents any wrong fault detection. Therefore, the mentioned drawbacks and vulnerable spots regarding fault localization in NPC inverter are tackled in this paper and also an efficient strategy to pinpoint a faulty clamping diode is presented.

The rest of this paper is organized as follows: In the second section, failure mode analysis of the single-phase NPC/H-bridge inverter under open-switch fault condition is presented. In section III, the proposed fault diagnosis method including fault detection and fault localization strategies, is detailed. In section IV, some selected simulation results are provided and discussed. In section V, the experimental results are reported. Finally, in section VI, conclusions are drawn regarding the proposed fault diagnosis method.

II. OPEN-CIRCUIT FAILURE MODE ANALYSIS OF THE SINGLE-PHASE NPC/H-BRIDGE INVERTER

The schema of a single phase NPC/H-bridge inverter is illustrated in Fig. 1. In accordance with Table I which is established for healthy mode operation, the five achievable voltage levels and the corresponding conducting components are presented. Table II depicts the switching patterns related to each switching state, regardless of the output current sign. For the sake of simplicity and also to better represent the switching patterns, decimal numbers are attributed to each switching state by considering the switching pattern as an 8-bit word. In Table III and Table IV (the three left columns), post-fault operation of the inverter is demonstrated for each switching state as well as the corresponding terminal voltages and conducting components. The cases involving clamping diodes are highlighted in yellow. Table III and Table IV are established for the positive and negative terminal currents, respectively. In order to clarify the approach employed to establish Table III and Table IV, some cases are detailed in the following.

For positive terminal current, when switching state 2 is applied in normal operation, current passes through S11, S12, S23 and DC4 (Table I). After the open-circuit fault occurrence in S11, the terminal current flows through DC1 rather than S11 (Table III). Consequently, the terminal voltage attains 0 V rather than +Vdc/2 in healthy mode. In case of open-circuit fault in S23 or DC4 in switching state 2 for positive terminal current, freewheeling diodes D21 and D22 conduct instead of

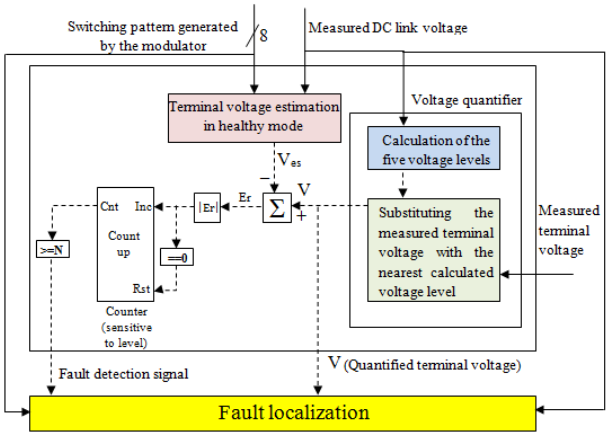

Fig. 2. Proposed fault detection principle.

TABLE III
IDENTIFICATION OF THE DEFECTED COMPONENT FOR POSITIVE CURRENT

State	Faulty switch or diode	Conducting components (terminal voltage)	Second step	Conducting components (terminal voltage)
1	S11	DC1, S12, S23, S24 (Vdc/2)	S24 is switched off	DC1, S12, S23, DC4 (0)
1	S24	S11, S12, S23, DC4 (Vdc/2)		S11, S12, S23, DC4 (Vdc/2)
1	S12	D14, D13, S23, S24 (0)	S23 is switched off	D14, D13, D22, D21 (-Vdc)
1	S23	S11, S12, D22, D21 (0)		S11, S12, D22, D21 (0)
2	S12	D14, D13, S23, DC4 (-Vdc/2)	S12 is identified in the first step.	
2	S11	DC1, S12, S23, DC4 (0)	S24 is switched on	DC1, S12, S23, S24 (Vdc/2)
2	S23	S11, S12, D22, D21 (0)		S11, S12, D22, D21 (0)
2	DC4	S11, S12, D22, D21 (0)		S11, S12, S23, S24 (Vdc)
3	S23	DC1, S12, D22, D21 (-Vdc/2)	S23 is identified in the first step.	
3	S12	D14, D13, S23, S24 (0)	S11 is switched on	D14, D13, S23, S24 (0)
3	DC1	D14, D13, S23, S24 (0)		S11, S12, S23, S24 (Vdc)
3	S24	DC1, S12, S23, DC4 (0)		S11, S12, S23, DC4 (Vdc/2)
5	S12	D14, D13, S23, DC4 (-Vdc/2)	S11 is switched on	D14, D13, S23, DC4 (-Vdc/2)
5	DC1	D14, D13, S23, DC4 (-Vdc/2)		S11, S12, S23, DC4 (Vdc/2)
5	S23	DC1, S12, D22, D21 (-Vdc/2)		S11, S12, D22, D21 (0) (see Table V for third step)
5	DC4	DC1, S12, D22, D21 (-Vdc/2)		S11, S12, D22, D21 (0) (see Table V for third step)
7	S12	D14, D13, D22, D21 (-Vdc)	S11 is switched on	D14, D13, D22, D21 (-Vdc)
7	DC1	D14, D13, D22, D21 (-Vdc)		S11, S12, D22, D21 (0)
8	S23	D14, D13, D22, D21 (-Vdc)	S24 is switched on	D14, D13, D22, D21 (-Vdc)
8	DC4	D14, D13, D22, D21 (-Vdc)		D14, D13, S23, S24 (0)

TABLE IV
IDENTIFICATION OF THE DEFECTED COMPONENT FOR NEGATIVE CURRENT

State	Faulty switch or diode	Conducting components (terminal voltage)	Second step	Conducting components (terminal voltage)
2	S22	D11, D12, D23, D24 (Vdc)	S21 is switched on	D11, D12, D23, D24 (Vdc)
2	DC3	D11, D12, D23, D24 (Vdc)		D11, D12, S21, S22 (0)
3	S13	D11, D12, D23, D24 (Vdc)	S14 is switched on	D11, D12, D23, D24 (Vdc)
3	DC2	D11, D12, D23, D24 (Vdc)		S13, S14, D23, D24 (0)
5	S13	D11, D12, S22, DC3 (Vdc/2)	S14 is switched on	D11, D12, S22, DC3 (Vdc/2)
5	DC2	D11, D12, S22, DC3 (Vdc/2)		S13, S14, S22, DC3 (-Vdc/2)
5	S22	DC2, S13, D23, D24 (Vdc/2)		S13, S14, D23, D24 (0) (see Table V for third step)
5	DC3	DC2, S13, D23, D24 (Vdc/2)		S13, S14, D23, D24 (0) (see Table V for third step)
7	S22	DC2, S13, D23, D24 (Vdc/2)	S22 is identified in the first step.	
7	S13	D11, D12, S21, S22 (0)	S14 is switched on	D11, D12, S21, S22 (0)
7	DC2	D11, D12, S21, S22 (0)		S13, S14, S21, S22 (-Vdc)
7	S21	DC2, S13, DC3, S22 (0)		S14, S13, DC3, S22 (-Vdc/2)
8	S13	D11, D12, DC3, S22 (Vdc/2)	S13 is identified in the first step.	
8	S14	DC2, S13, DC3, S22 (0)	S21 is switched on	DC2, S13, S21, S22 (-Vdc/2)
8	S22	S13, S14, D23, D24 (0)		S13, S14, D23, D24 (0)
8	DC3	S13, S14, D23, D24 (0)		S13, S14, S22, S21 (-Vdc)
9	S13	D11, D12, S22, S21 (0)	S13 is switched off	D11, D12, S22, S21 (0)
9	S14	DC2, S13, S22, S21 (-Vdc/2)		D11, D12, S22, S21 (0)
9	S22	S13, S14, D23, D24 (0)		D11, D12, D23, D24 (Vdc)
9	S21	S13, S14, DC3, S22 (-Vdc/2)		D11, D12, DC3, S22 (Vdc/2)

TABLE V
IDENTIFICATION OF THE DEFECTED COMPONENT IN THIRD STEP

State	Faulty switch or diode	Third step	Conducting components (terminal voltage)
5, (I>0)	S23	S24 is switched on	S11, S12, D22, D21 (0)
5, (I>0)	DC4		S11, S12, S23, S24 (Vdc)
5, (I<0)	S22	S21 is switched on	S13, S14, D23, D24 (0)
5, (I<0)	DC3		S13, S14, S21, S22 (-Vdc)

S23 and DC4. Therefore, the terminal voltage drops to 0 V. Likewise, the presented analysis is applicable to obtain the new current paths and new terminal voltages in all cases of open-switch fault occurrence in the other half-legs and

negative terminal currents. By observing the results given in Table III and Table IV, it can be concluded that when open-circuit fault occures in the internal switches (S12, S13, S22, and S23) or clamping diodes, the two freewheeling diodes situated in the opposing half-leg conduct rather than the defected switch. Moreover, in case of open-circuit fault occurrence in the external switches (S11, S14, S21, and S24), the terminal current flows through the clamping diode connected to the same half-leg. It should be noted that the failure mode analysis results are used for fault localization step, subsequent to fault detection. By comparing the terminal voltage corresponding to each switching state in Table I (healthy operation) with those in Table III and Table IV (post-fault operation), it is deduced that in case of open-circuit fault occurrence, magnitude of the error value is always greater than or equal to Vdc/2. Thus, the fault detection could be realized for all cases.

III. Principles of the Proposed Fault Diagnosis Approach

A. *Fault detection strategy*

In a fault diagnosis approach, the fault detection is an essential step to be performed prior to the fault localization procedure. The proposed fault detection procedure is based on comparing the measured terminal voltage with the predicted terminal voltage. Knowing the switching pattern applied to the power switches as well as the DC link voltage value, the estimation of the terminal voltage is realized. Therefore, the control signals already available in the control system fulfill the fault detection requirements. Although the terminal voltage measurement is not universally used in all the inverters, it is not merely used for fault diagnosis. It could be used for control and monitoring in grid-connected applications and some electric motor drives. Likewise, DC link voltage measurement could be indispensable for protection and also control of the output of the rectifiers or choppers which supply DC link. In the fault detection strategy proposed in this paper, certain performance constraints are fulfilled as discussed hereafter. Even in healthy mode operation, at any instant, there is difference between the measured terminal voltage and its estimated value, due to voltage drop in the components, commutation effect, response time of the sensors and measurement errors. As depicted in Fig. 2, a voltage quantifier is devised to compensate the voltage measurement error and also to compensate the voltage drop. In normal operation, the measured terminal voltage is around one of the five voltage levels in terms of DC link voltage presented previously (terminal voltages in Table I). Therefore, the voltage quantifier assigns the nearest terminal voltage, based on DC link voltage measurement, to the measured terminal voltage. Thus, thanks to the voltage quantification employed, a safe margin is employed. This safe margin prevents any false fault detection due to the voltage drop in the components and measurement errors. Since the quantified measured voltage is also applied in fault localization phase, all of the mentioned benefits obtained thanks to the voltage quantification are applied in the fault localization. Even in normal operation, once the switching pattern changes, due to the existing delay

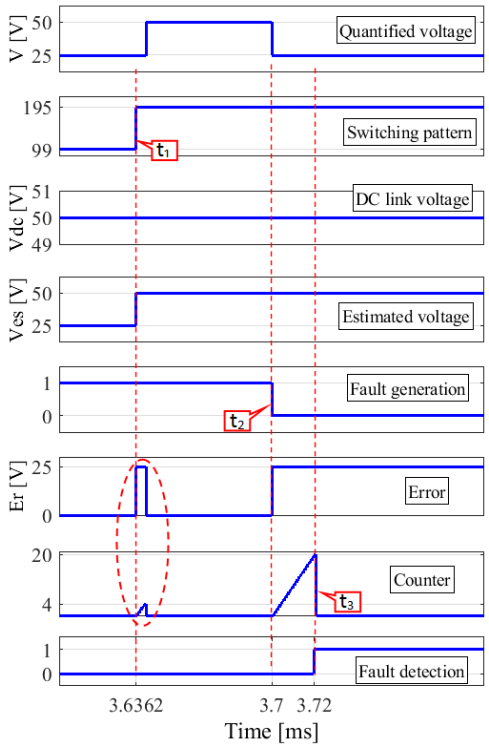

Fig. 3. Fault detection procedure in case of open-circuit fault occurrence in S11.

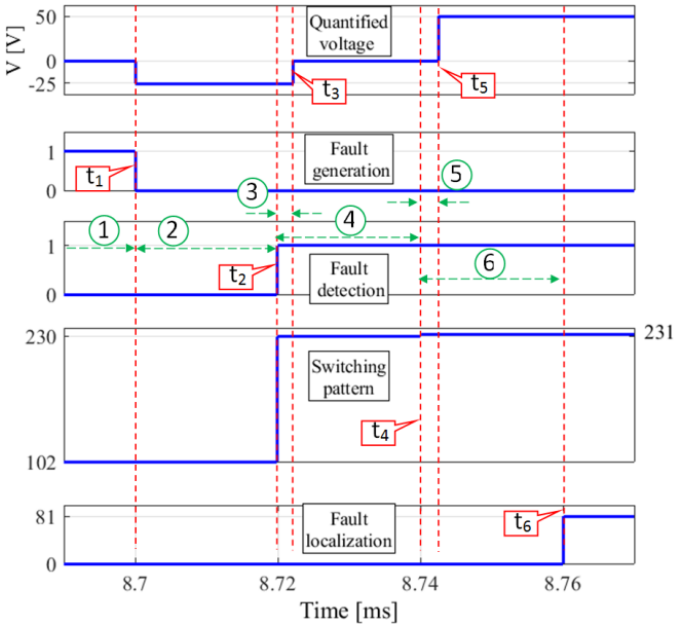

Fig. 4. Simulation results for localization of faulty clamping diode DC4 in the third step.

times, the last measured terminal voltage does not immediately correspond to the new switching pattern. In order to solve this problem, as depicted in Fig. 2, a counter is employed. If the voltage error subsists beyond the up limit value, it means that this voltage error is due to a real open-switch fault and consequently the fault declaration signal is generated. Otherwise, the voltage error arises from the commutations and the sensor response time. The up limit value of the counter is determined based on the overall delay

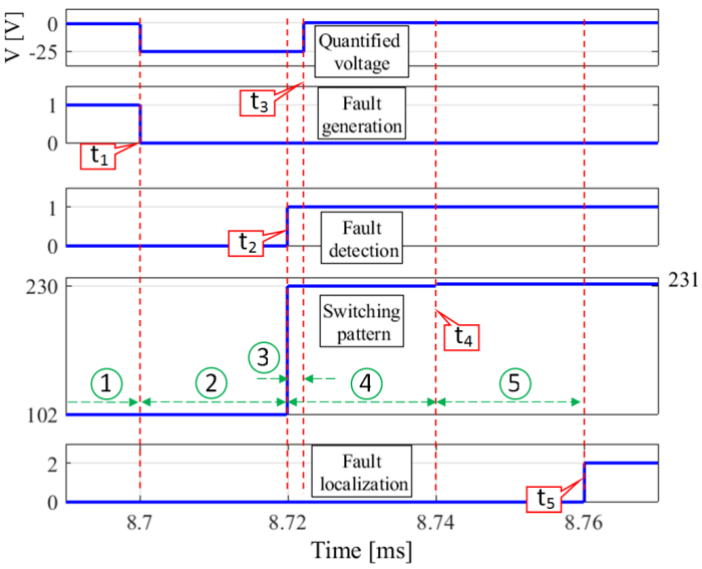

Fig. 5. Simulation results for localization of faulty component S23 in the third step.

time which is due to the response time of the sensors and turn off and turn on delay times of the power switches. This overall delay time does not surpass 4 µs. In order to consider a safe margin to avoid any wrong fault detection, the up limit value is set at 20 µs.

B. *Fault localization strategy*

Subsequent to the detection of the open-circuit fault occurrence, the fault localization strategy is initiated. It is based on the failure mode analysis. If DC link voltage measurement is required for control and protection of the converter, one can state that for fault localization, no extra sensor is employed. Otherwise the DC link voltage sensor is treated as an additional hardware. In Table III, Table IV, and Table V, for all the possible switching states with positive and negative load currents, the post-fault analysis is summarized. As shown in Table III, in case of open-circuit fault occurrence in external switches S11, S14, S21 and S24, the faulty switch necessarily is identified after performing a switching pattern modification (second step) while in case of the open-circuit fault in internal switches S12, S13, S22, and S23, the defected switch is located directly or after a second step depending on the applied switching state. In order to locate a faulty clamping diode, according to Table III, Table IV, and Table V the second step or the third step should be performed. Knowing the last applied switching state (just before fault detection) and the load current sign, the fault localization algorithm locates the relevant subsection in Table III or Table IV (state number with current sign). Afterwards, the measured terminal voltage which has been quantified in the fault detection step is compared with the expected voltages estimated by assuming the open-circuit fault occurrence in each power switch or clamping diode. In this regard, an example accompanying the simulation results is given in the next sections to clarify the employed fault localization algorithm.

IV. Simulation Results

The simulation results consist of two sections. In the first one, only the fault detection strategy is presented. The second one deals with simulation results concerning the fault localization. It should be noted that in all sections the load resistance, the load inductance, the switching frequency, the fundamental frequency, the DC link capacitors, the DC link voltage and modulation index are set at 27.7 Ω, 9 mH, 1 kHz, 50 Hz, 2.2 mF, 50 V and 0.8, respectively. Since the converter topology is symmetric, the simulation results are solely presented for the positive load current. The simulations have been carried out in MATLAB/Simulink environment.

A. *Fault detection strategy*

Since principles of the proposed fault detection strategy are similar for all switches and clamping diodes, S11 is arbitrarily chosen as a case study. As shown in Fig. 3, at instant t_1 (healthy condition), the switching pattern changes from 99 (state 3) to 195 (state 1) which according to Table II corresponds to terminal voltage change from +Vdc/2 to Vdc. Although this variation occurs in healthy mode, the error due to the delay times indicates the discrepancy between the quantified and the estimated voltage values during the short transient time. Since the error value does not subsist noticeably, the counter output (Fig. 3) does not reach the maximum limit (here N=20). Thus, any fault detection is not declared. At instant t_2 (state 2), an open-circuit fault occurs in S11. In compliance with Table III, the quantified terminal voltage drops to +Vdc/2 while the estimated voltage which depends on the switching pattern, remains in +Vdc (Table II, state 1). Therefore, the error signal reaches +Vdc/2 and remains in this value. Once the counter reaches the upper limit N at instant t_3, the fault detection signal is generated.

B. *Fault localization strategy*

As discussed previously, according to the last applied switching pattern in healthy mode, the defected switch is located in the first, second or third step (Tables III, IV and V) while the faulty clamping diode is identified in the second or third step. In order to avoid verbosity, the longest procedure or in another words, the most comprehensive case study is elaborated. The chosen case study includes identifying the faulty switch and clamping diode in the third step.

Fig. 4 and Fig. 5 represent the fault localization procedure for clamping diode DC4 and switch S23, respectively. It should be noted that for better representing the faulty switch in the simulations, specific numbers are assigned to the power switches and clamping diodes. The numbers 128, 64, 32, 16, 8, 4, 2, 1, 3, 9, 27 and 81 are assigned to S11, S12, S13, S14, S21, S22, S23, S24, DC1, DC2, DC3 and DC4, respectively. As shown in Fig. 4, before instant t_1 (interval 1), the inverter operates in healthy mode during which the terminal voltage and switching state are equal to 0 V and 102 (switching state 5). Therefore, just before the fault generation in DC4 at instant t_1, current flows through DC1, S12, S23 and DC4. Once the open-circuit fault is generated in DC4 at instant t_1, the quantified voltage drops to –Vdc/2 which is justified by Table III. Hence, at instant t_2 the fault detection is declared.

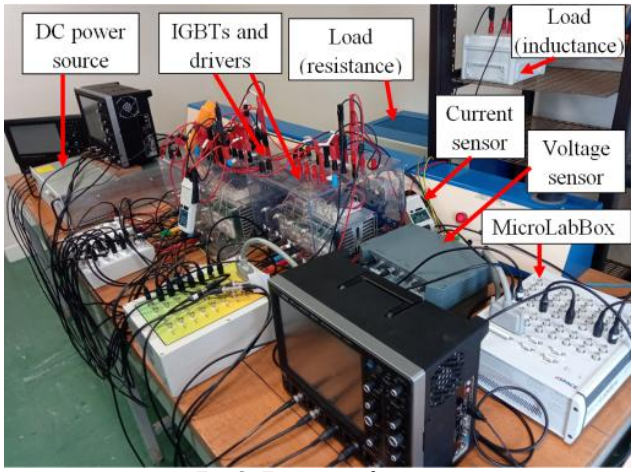

Fig. 6. Experimental setup.

However, the faulty component identification is still not possible because by referring to Table III, an open-circuit fault occurrence in S12, DC1, S23 or DC4 leads to the same quantified voltage –Vdc/2 at the first step. Inevitably, the second step has to be performed in which the gate signal of S11 is switched on once the fault detection is declared at instant t_2 as observed in Fig. 4. Once S11 conducts, the current path according to Table III is formed of S11, S12, D22, D11. Consequently, the quantified voltage reaches 0 at instant t_3 due to the delay times (interval 3). By referring to the corresponding subsection in Table III, after the second step (applying the first modification of the switching pattern), the measured quantified terminal voltages resulted by open-circuit fault occurrence in S23 and DC4 are the same and equal to 0 V. Consequently, by performing two steps, the faulty component between S23 and DC4 is not distinguished which necessitates to perform the third step. For this purpose, at instant t_4 in accordance with Fig. 4, the third step is carried out by closing S24. After passing interval 5 (similar to interval 3 caused by delay times), the quantified terminal voltage attains +Vdc at instant t_5. By comparing the obtained results with the corresponding failure-mode analysis tabulated in Table V, the defective component DC4 is declared at instant t_6. It should be noted that comparison of the quantified terminal voltage with estimated voltage values following to each switching pattern modification (at instant t_2 and t_4) is performed after interval 3 and 5 (chosen in accordance with N value for fault detection procedure) to prevent wrong fault localization due to the existing delays. Likewise, a similar analysis is employed to justify the fault localization procedure represented in Fig. 5 for faulty switch S23. In case of the fault occurrence in S23, the quantified voltage after closing S24 in the third step remains equal to zero.

Likewise, fault localization strategy employed to identify any defected component has been validated by simulation.

It should be noted that the purpose of the fault diagnosis is applying the appropriate actions to ensure the fault tolerant operation of the inverter, irrespective of whether the fault is occurred in a power switch or in a driver. Indeed, from this view point, the open circuit fault event in a switch or in the corresponding driver has the same impact.

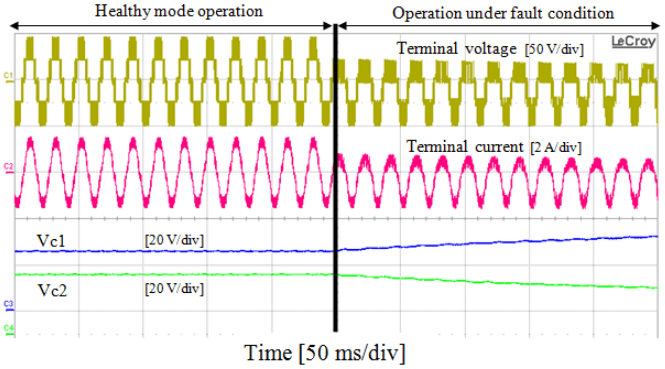

Fig. 7. Experimental results of the inverter operation under fault event in S11 without fault diagnosis.

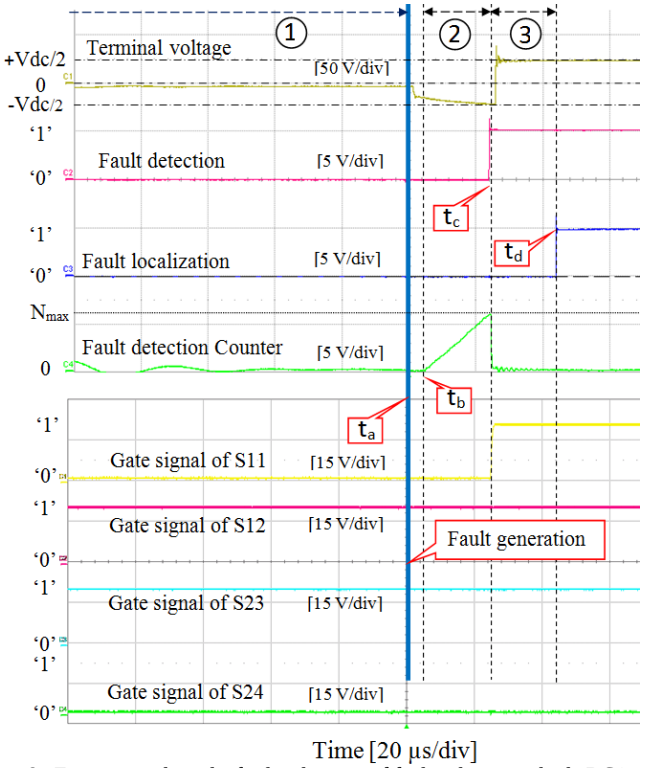

Fig. 8. Experimental results for localization of faulty clamping diode DC1 in the second step.

In this research work, the fault diagnosis for the anti-parallel diodes is not investigated which can be an interesting proposition for the future studies if the redundant anti-parallel diodes are not incorporated in the fault tolerant structure.

V. Experimental Results

For the implementation of the modulator and the fault diagnosis parts (fault detection and fault localization), a MicroLabBox (one of the dSPACE platforms) containing a processor and an FPGA chip (Xilinx® Kintex®-7 XC7K325T) is used. The modulation and the diagnosis parts are implemented separately in such a way that the modulator is implemented on the processor module of MicroLabBox (dSPACE platform) and the diagnosis part is implemented on the Xilinx FPGA chip of MicroLabBox. Since the fault

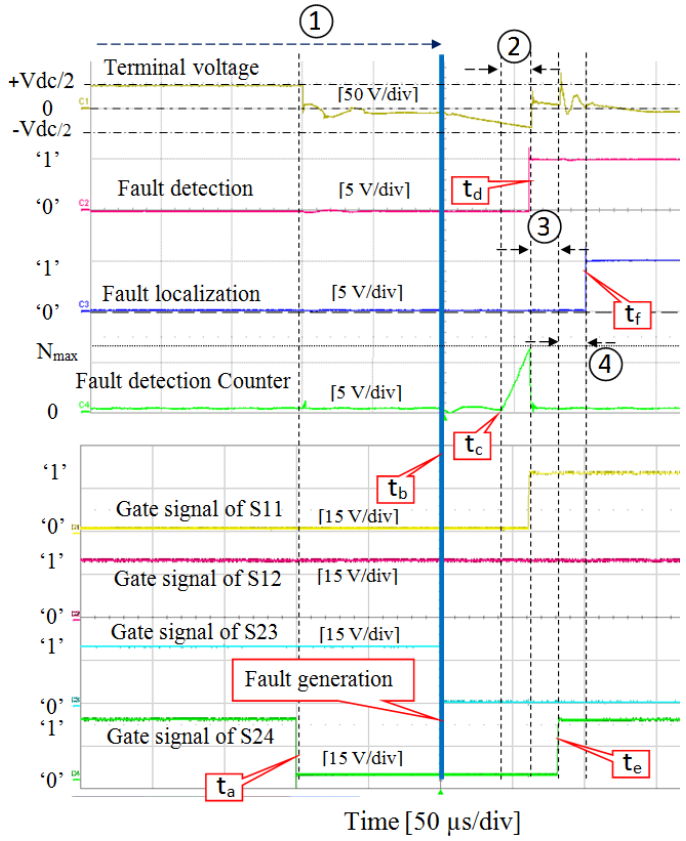

Fig. 9. Experimental results for localization of faulty switch S23 in the third step.

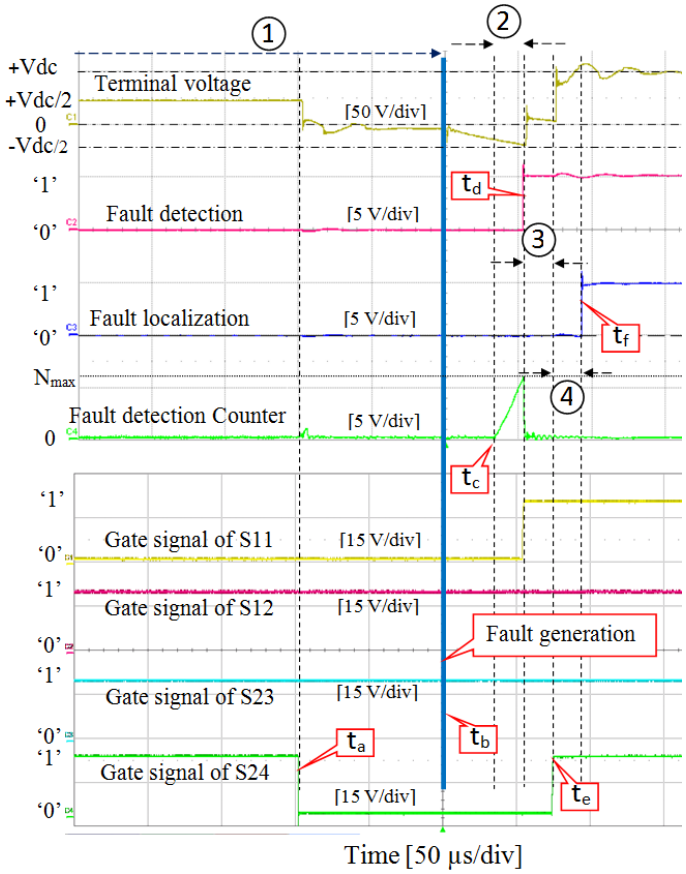

Fig. 10. Experimental results for localization of faulty clamping diode DC4 in the third step.

detection and localization procedures must be carried out quickly, the fault diagnosis part is realized by the FPGA-based module of the MicroLabBox. The inverter is constituted of the IGBTs SKM50GB123D of SEMIKRON, commanded by SKHI22A drivers. The experimental setup is shown in Fig. 6. For the experimental setup, all parameters are the same as those reported in the simulation section. In order to generate an open circuit fault in an IGBT, the gate signal of the concerned IGBT is interrupted. In order to generate an open circuit fault in a clamping diode, an IGBT is connected in series with the concerned clamping diode. Throughout the healthy operation, a high level signal (‘1’) is applied to the gate of the IGBT connected in series with the clamping diode. To generate the open circuit fault, the gate drive of the IGBT connected in series with the concerned clamping diode is set at low level (‘0’). Hence, the branch including the clamping diode cannot carry any current which is treated as an open circuit fault event in the clamping diode. In the experimental results, switching pattern is illustrated by four selected IGBTs gate signals. Based on these four IGBTs gate signals, the switching state can be determined according to Table II because the command signals corresponding to the other four IGBTs are complementary. Moreover, similar to the simulation section, the results are only represented for fault occurrence in case of a positive current to avoid the verbosity. In this section, the most complicated case study is presented in which, depending on the faulty component, two steps or three steps should be performed.

As can be seen in Fig. 7 (without applying fault diagnosis), in case of open circuit fault occurrence in S11, the voltage level +Vdc is no longer achievable at the terminal voltage leading to increase in harmonic content of the terminal voltage and current. Above all, once the fault occurs, the DC link capacitors’ voltages diverge from their rated value. Hence, one of them would be subject to overvoltage. Therefore, considering a fault diagnosis method is of a great importance to stop operating quickly or to take the appropriate actions for ensuring fault tolerant operation of the converter. As can be seen in the following, since the fault diagnosis is accomplished within some tens of µs, failure of DC link capacitors does not occur.

According to Fig. 8, before the fault event, the inverter operates in healthy mode during interval 1 where the applied switching state and the terminal voltage are S5 and 0 V, respectively (see Table II). Subsequent to the fault event in DC1 at the instant t_a, (switching state S5), the terminal voltage drops to –Vdc/2 (see Table III) and the counter starts to count at the instant t_b. At the end of interval 2, the counter reaches to the predefined value (N_{max}) and consequently the fault occurrence is declared at the instant t_c. However, the faulty component is still not identified among the components S12, DC1, S23 and DC4 (see Table III). Therefore, performing the second step is necessary (closing the S11 in accordance with Table III). To this end, once the fault occurrence is detected, the gate signal of S11 is established. Subsequent to the performing the second step, the terminal voltage reaches +Vdc/2 and at the instant t_d, the DC1 is identified as the faulty component. As mentioned previously, interval 3 (chosen in accordance with N_{max} value for fault detection procedure) prevents wrong fault localization due to the existing delays.

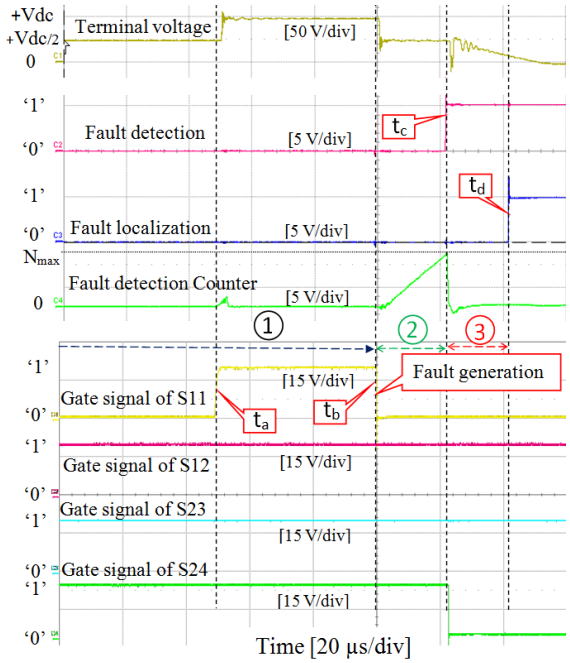

Fig. 11. Experimental results for localization of faulty external switch S11 in the second step.

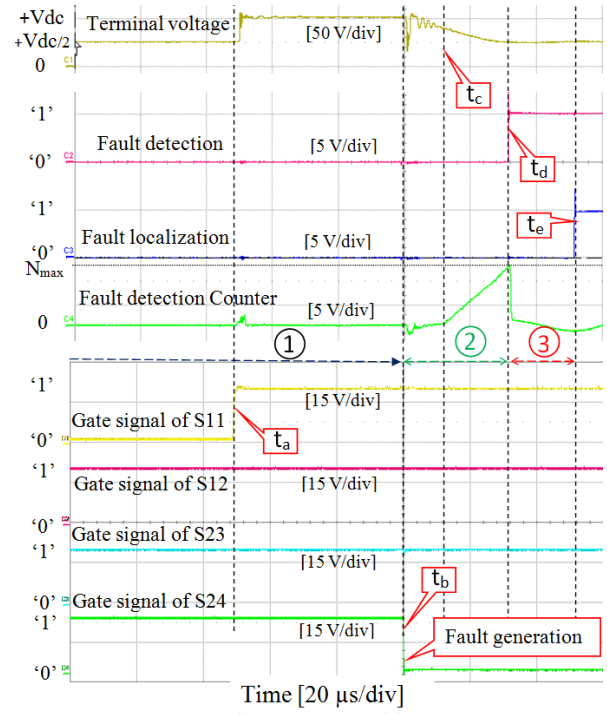

Fig. 12. Experimental results for localization of faulty external switch S24 in the second step.

In Fig. 9, prior to the fault event in the S23, the inverter operates in healthy mode during interval 1. Before the instant t_a, the applied switching state and the terminal voltage are S2 and +Vdc/2 (according to Table II) and after the instant t_a, the applied switching state is S5 and 0 V is obtained at the terminal (see Table II). The open-circuit fault is generated in the S23 at the instant t_b and subsequent to the fault event, the terminal voltage reaches –Vdc/2 (see Table III). At the instant t_c, the counter starts to count and at the end of interval 2 it reaches the maximum limit. The fault occurrence is detected at the instant t_d but it is still not possible to pinpoint the defective component among the components S12, DC1, S23 and DC4 (see Table III). Therefore, performing the second step is necessary (switching on the S11 in accordance with Table III). After switching on S11 at the instant t_d, the terminal voltage attains 0 V. However, after performing the second step, the faulty component is still not distinguished between the components S23 and DC4. Hence, performing the third step is mandatory. For this purpose, at the instant t_e the S24 is switched on and the terminal voltage remains at 0 and thus, at the instant t_f (see Table V), the component S23 is identified as faulty component. It should be noted that the interval 3 and interval 4 (chosen in accordance with N_{max} value for fault detection procedure) are considered to prevent any wrong fault identification due to the existing delays and transition times. The same procedure could be applied to identify the faulty component DC4 in the third step presented in Fig. 10. The only difference is that after applying the third step in case of fault event in DC4, the terminal voltage reaches +Vdc instead of 0 (see Table V). As can be seen in Fig. 9 and Fig. 10, despite of voltage transients during healthy operation (during interval [t_a , t_b]), wrong fault detection is avoided which is due to the voltage quantifier. Furthermore, after fault detection, despite of the voltage transients, the fault component is identified correctly.

As demonstrated in Fig. 11, during interval 1, the inverter operates in healthy mode. According to the presented gate signals and Table II, right before the open-circuit fault event at instant tb, switching state 1 is applied (corresponding to the terminal voltage +Vdc). Once the open-circuit fault is generated in S11 at instant t_b, the terminal voltage attains +Vdc/2 (which complies with Table III). Due to the mismatch between the measured terminal voltage (+Vdc/2) and the terminal voltage corresponding to switching state 1 (+Vdc according to Table II), the counter starts to count. At the end of the interval 2, the counter reaches the up-limit value. Therefore, the fault detection signal is generated at instant t_c and the localization step is triggered. In accordance with Table III, it is not still possible to distinguish the faulty component between S11 and S24. Thus, once the fault event is declared, the gate signal of S24 is set to zero (complying with Table III for the fault localization). Hence, the terminal voltage reaches 0 V and at instant t_d, the defected switch is located. As addressed in the analysis of the simulation results, interval 3 (chosen in accordance with Nmax value for fault detection procedure) prevents wrong fault localization due to the delay times. Likewise, a similar analysis is applied to justify the fault localization step presented in Fig. 12 for faulty switch S24. In case of the fault event in S24, after interrupting the gate signal of S24 in the second step, the terminal voltage remains equal to +Vdc/2. In order to prevent any system damage following to the fault diagnosis, all the IGBTs should be switched off once the faulty component is identified.

VI. Conclusion

The presented strategy not only detects the open-switch and open-clamping diode fault occurrence but also identify quickly the defected component in any case. The required signals and

measurements such as the DC link voltage, the terminal voltage, the switching pattern and the current sign are available in the control system. In this strategy, compared with the literature, some measurements which are merely used for fault diagnosis are avoided for example, measuring the pole voltages, measuring the voltages across each DC link capacitor, measuring the current of the clamping diodes, measuring the neutral point voltage and measuring the current injected to the neutral point are avoided. However, for realizing the proposed fault diagnosis method, a sensor for DC link voltage measurement is required. In applications where DC link voltage is neither used for control nor for protection, the employed sensor is considered as an extra component. Furthermore, complicated calculations, component modeling and load parameters are not required in the proposed strategy. In addition, for the fault detection procedure, an efficient method using a voltage quantifier has been presented with which wrong fault detection due to the components voltage drop and measurement errors are avoided. Moreover, an efficient and new strategy is proposed to diagnose a faulty clamping diode which is rarely seen in the previous studies. The represented simulation results confirm the effectiveness and fastness of the presented fault diagnosis strategy. The experimental results validate the effectiveness and merits of the proposed approach. The investigated approach could be applied and generalized for other multilevel topologies as a fast, effective, simple and economic strategy. Failure mode analysis employed for fault localization procedure is logic based and does not require any calculation allowing to employ FPGA for fast fault detection and fault localization in parallel with control system which leads to high time performance. The only parameters restricting the time performance of the presented approach are intrinsic characteristics and imperfection of the components which are not avoidable. For instance, the fault detection is infeasible when the largest pulse width corresponding to the switching state involving the faulty component is lower than 20 µs. This pulse width corresponds to a high switching frequency (at least 50 kHz) which is rarely used for multilevel converters.

Although multiple fault events are very unlikely, the proposed approach cannot diagnosis multiple faults. Furthermore, employing an FPGA chip can complicate the implementation of the proposed strategy because it should be inserted between the modulator and the drivers of the power switches.

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