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A Real Time Fault Diagnosis for Neutral-Point-Clamped Inverters based on failure mode algorithm

Sajjad Ahmadi, Philippe Poure, *Member, IEEE*, Shahrokh Saadate, Davood Arab Khaburi

***Abstract*—Fault diagnosis in multilevel converters is of great importance since they are comprised of more solid-state switches, compared to the conventional two-level converters. This paper proposes a fast and efficient real time fault detection and faulty component identification for open-switch fault diagnosis, based on failure mode algorithm for a single-phase five-level neutral-point-clamped inverter. Component modeling, complicated calculations and load parameters are not required for realizing the proposed approach. Furthermore, the proposed strategy does not require any extra sensor. The signals already available in the control system such as the applied switching pattern and terminal voltage fulfill the fault diagnosis. Thanks to the proposed fault detection strategy, any misdiagnosis arising from noise existence, response time of the sensors, turn on and turn off delay times of the power switches and measurement errors are avoided. The simulations and experiments are carried out to confirm the performance and effectiveness of the presented strategy.**

***Index Terms*— Failure mode algorithm, fault diagnosis, open-switch fault, failure mode analysis, multilevel inverter.**

I. Introduction

NOWADAYS, numerous researches are being conducted on multilevel inverters due to their advantages over conventional two-level inverters such as reduced total harmonic distortion of the generated voltage and current, higher voltage level, reduced voltage stress, less switching losses, limitation of the voltage transients dv/dt, smaller size of the required filter elements and reduced common-mode voltages [1], [2]. The neutral-point-clamped (NPC) inverter as a kind of multilevel inverter is the most widely used topology in the industry because this topology does not require flying capacitors and isolation transformers and comprises less active switches compared to active NPC (ANPC) inverters. Moreover, NPC inverters compared to T-type inverters can withstand against the higher voltage levels. However, for high voltage applications, the number of switches per each leg increases inevitably leading to static and dynamic voltage sharing problems [3]. In order to eliminate the mentioned weak points, NPC inverters based on a single-phase five-level module (Fig. 1) are used. Thus, each module has its own DC link capacitors in contrast with the three-level NPC inverters in which the DC link capacitors are shared by the three phases. However, this inverter, like other multilevel converters in comparison to two-level conventional inverters, has a higher number of switches. Hence, the switch fault occurrence is more likely in NPC inverter. Fault diagnosis step is prerequisite for realizing fault tolerant operation which is of great importance for safety-critical applications [4]. Furthermore, fault diagnosis is critical in applications where the reliability of the maintenance techniques for electric derives is a crucial factor [5]. Thus, fault diagnosis strategies for power switches have attracted attentions.

In case of short circuit fault occurrence, a huge current flows through the components. However, it should be noted that the short circuit faults can be suppressed and canceled by means of the protection circuits and fuses while in case of open-circuit fault event the fuses do not blow. Thus, the open circuit fault can remain in the system. Open-switch fault can lead to increase in harmonic content of the terminal voltage or current which in long term has destructive impact on the equipment supplied by the inverter such as transformers or electric motors. Furthermore, in case of open-switch fault event, the DC link capacitors' voltages can diverge from their rated value in such a way that one of them would be subject to overvoltage and eventually breakdown. Therefore, the system should be equipped with a fast open-circuit fault diagnosis capability to prevent the consequences arising from the open-switch fault occurrence.

The open-switch fault diagnosis methods are mainly divided into current and voltage based algorithms. The voltage based methods are faster than the current based approaches but generally require extra sensors and circuits. In recent years, numerous open-switch fault diagnosis methods applied in two-level conventional converters have been presented [6]-[15]. Papers [6] and [7] present a literature review of fault diagnosis

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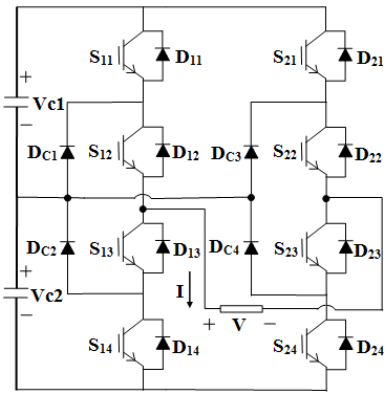

Fig. 1. Scheme of a single-phase five-level NPC inverter module.

in power inverters. In [8], a diagnosis method for two level voltage source inverters (2L-VSI) based on average absolute value of current is proposed. The diagnosis method presented in [9] for a 2L-VSI requires the measured motor phase currents and the corresponding reference signals. In [10] by employing model reference adaptive system technique, a fault diagnosis method is presented for a 2L-VSI. The research work presented in [11] proposes a current based method for fault diagnosis in a 2L-VSI. In [12], fault diagnosis for a 2L-VSI is carried on based on residual vector. In [13], analytical model of a 2L-VSI is employed to present a fault diagnosis approach. The research effort presented in [14] investigates the use of fuzzy logic for fault diagnosis in a 2L-VSI. In [15], by using external circuits and switching function model of 2L-VSI, a fault diagnosis strategy is proposed. The summarized description and remarkable points of the research works presented in [8]-[16] are tabulated in Table I.

In addition, several research studies have been devoted to fault diagnosis strategies in multilevel converters. To this end, in [16], the average current Park's Vector strategy is applied to diagnose the faulty upper or lower half-leg of a three-level NPC inverter. However, the proposed strategy is not able to identify the faulty switch in the defected half-leg. In [17], by applying the average current Park's Vector, the defected switch can be located in a three-level NPC inverter. For the same topology, the fault diagnosis strategy proposed in [18] is based on the analysis of the different current waveforms. The proposed approach solely identifies the faulty half-leg in the grid-side inverter and cannot identify the faulty component. In [19], additional circuits are used to detect an open-switch fault in a defected phase of a three-level NPC inverter. This approach cannot identify the faulty switch. Moreover, this strategy is based on the pole voltage measurement, which requires extra sensors. The diagnosis strategy presented in [20] is based on pole voltage estimation. The pole voltage estimation requires accurate knowledge of the line parameters. In [21], the fault diagnosis is based on the radius of the Concordia current pattern for three-level NPC inverter system. In [22], the faulty switch in H-bridge multilevel converters is located using neural network algorithm. The realization of the proposed algorithm requires long calculations and reduces the temporal performance. In [23], six Rogowski coils are positioned in the current paths to diagnose the fault in three-level NPC converters. This method cannot be considered as a cost-effective approach. In [24], by analyzing the current in case of an open-switch fault occurrence, the defected

TABLE I
SUMMARY OF THE RESEARCH WORKS ADDRESSED IN THIS PAPER DEALING WITH FAULT DIAGNOSTIC METHODS FOR TWO-LEVEL CONVENTIONAL INVERTERS

Ref	Description of the method	State of the art versus the proposed approach
[8]	Based on average absolute value of current	- Current based method
[9]	Based on measurement of the phase currents and the corresponding reference signal	- Current based method
[10]	Employs the model reference adaptive system technique	- Relies on the electrical model of the motor supplied by the converter
[11]	Based on the analysis of the inverter symmetric topology by introducing allelic points	- Complicated method requiring to set five threshold values - Current based method
[12]	Based on current residual vector method	-Requires the resistance and inductances of the motor supplied by the converter - Current based method
[13]	Based on voltage measurement	-Employs extra sensors
[14]	Based on fuzzy logic	- Current based method
[15]	Based on switching function model of the converter	- Requires external circuits

TABLE II
SUMMARY OF THE RESEARCH WORKS ADDRESSED IN THIS PAPER DEALING WITH FAULT DIAGNOSTIC METHODS NPC INVERTERS

Ref	Description of the method	State of the art versus the proposed approach
[16]	Uses average current Park's strategy	- Solely detects faulty half-leg - Current based method
[17]	Uses average current Park's strategy	- Current based method
[18]	Analyses the current waveforms	- Solely identifies a defected half-leg - Current based method
[19]	Measures the pole voltages	- Uses extra sensors and additional circuits - Only detects the faulty phase - Relies on the modulation technique
[20]	Based on the pole voltage estimation from the grid voltages	- Requires accurate knowledge of the line parameters
[21]	Uses Concordia current pattern method	- Current based method
[22]	Uses neural network algorithm	- Requires long calculations
[23]	Uses Rogowski coils to measure the currents	- Uses additional sensors - Current based method
[24]	Analyses the current waveforms	- Only applicable for grid-connected converters - Current based method
[25]	Uses the mixed logical dynamic modeling of the converter	- Depends on the equivalent inductance and resistance values of the traction transformer - Current based method
[26]	Analyses the electromagnetic emissions of the DC bus	- Requires external filters and antennas

component is pinpointed in a three-level NPC converter. This method is solely applicable for grid-connected three-level NPC converters. By using the mixed logical dynamic modeling of the single-phase grid-connected NPC/H-bridge converter in [25], the faulty component is identified. The proposed approach depends on the grid parameters such as the equivalent inductor and resistance of the traction transformer. In [26], the faulty component in the three-level NPC inverter is identified by analyzing the electromagnetic emissions of the DC bus, which requires the external filters and antennas. The summarized description and remarkable points of the research works presented in [16]-[26] are tabulated in Table II (second column).

In this paper, a real time fast and efficient fault diagnosis approach under open-circuit fault event in power switches in a single-phase five-level NPC inverter is presented.

The single-phase NPC inverter module (see Fig. 1) is considered in this paper. Unlike the previously mentioned approaches, which rely on current measurement and analysis ([16]-[18], [21]-[23]), the proposed approach is based on failure mode algorithm. The proposed algorithm consists of a preliminary analysis for all open-switch fault cases. In the proposed approach, any additional sensors and circuits are not required. Compared to the previously proposed method in [25], the modeling of the converter is not required and it does not rely on the AC side parameters. Our strategy is performed by means of the electrical signals available in the control system such as switching patterns, load voltage, and DC link voltage. Although the load voltage measurement is mostly used for monitoring and control in some applications such as grid-connected inverters and motor drives, it should be mentioned that it is not universally required. Furthermore, by devising a voltage quantifier, the shortcomings regarding the fault detection methods in [27]-[28] are overcome, as detailed in the later sections. To conclude this section, the major advantages offered by this research work compared to the state of the art (the information given in Table I and Table II, third column) can be summarized as follows: fast fault diagnosis is carried out thanks to employing a logic based failure mode algorithm, there is no requirement for load and feeding line parameters' values, the complicated calculations are not required and any external circuit is not employed.

The structure of this paper is organized as follows: In the second section, the operation of the NPC inverter under open-switch fault condition is presented. In section III the proposed fault diagnosis method, including the fault detection and fault localization strategies, is explained. In section IV, some selected simulation results are presented and discussed. In section V, the simulation results are validated by experimental ones. Finally, in section VI, conclusions are drawn regarding the proposed fault diagnosis method.

II. Open-switch failure mode analysis of the single phase NPC/H-bridge inverter

The proposed failure mode analysis is a design method applied to systematically analyze power switch failures and identify the resultant effects on system operation. Successful development of a failure mode analysis requires that the analysis includes all failure modes for each contributing power switch in the system. In this section, the topology of a single-phase five-level NPC inverter and the corresponding available terminal voltage levels are demonstrated. Afterwards, in case of open-circuit switch faults, the variations of terminal voltages are indicated according to the terminal current sign. In order to analyze the open-switch fault, the switches are classified into two groups, namely external and internal switches. The components S11, S14, S21 and S24 are treated as external switches, while the components S12, S13, S22 and S23 are considered as internal switches. The scheme of a single-phase five-level NPC inverter is illustrated in Fig. 1. In accordance with Table III which is established for healthy condition, the five voltage levels that can be reached and the corresponding conducting components are presented. Table IV describes the switching patterns associated with each switching state regardless of the current sign. For the sake of simplicity and also to better represent the switching patterns, decimal numbers are assigned to each switching state by considering the switching patterns as an 8-bit word.

Table V and Table VI (the three left-hand columns) show the post-fault operation of the inverter for each switching state, as well as the corresponding terminal voltages and

TABLE III
CONDUCTING COMPONENTS CORRESPONDING TO EACH SWITCHING STATE FOR POSITIVE AND NEGATIVE CURRENTS IN HEALTHY OPERATION

State	Terminal voltage	Conducting components (I>0)	Conducting components (I<0)
1	+Vdc	S11, S12, S23, S24	D11, D12, D23, D24
2	+Vdc/2	S11, S12, S23, DC4	D11, D12, S22, DC3
3	+Vdc/2	DC1, S12, S23, S24	DC2, S13, D23, D24
4	0	S11, S12, D22, D21	D11, D12, S21, S22
5	0	DC1, S12, S23, DC4	DC2, S13, S22, DC3
6	0	D14, D13, S23, S24	S13, S14, D24, D23
7	-Vdc/2	DC1, S12, D22, D21	DC2, S13, S22, S21
8	-Vdc/2	D14, D13, S23, DC4	S13, S14, DC3, S22
9	-Vdc	D14, D13, D22, D21	S13, S14, S22, S21

TABLE IV
SWITCHING PATTERNS CORRESPONDING TO EACH VOLTAGE LEVEL

State	Terminal voltage	S11	S12	S13	S14	S21	S22	S23	S24	Decimal number
1	+Vdc	1	1	0	0	0	0	1	1	195
2	+Vdc/2	1	1	0	0	0	1	1	0	198
3	+Vdc/2	0	1	1	0	0	0	1	1	99
4	0	1	1	0	0	1	1	0	0	204
5	0	0	1	1	0	0	1	1	0	102
6	0	0	0	1	1	0	0	1	1	51
7	-Vdc/2	0	1	1	0	1	1	0	0	108
8	-Vdc/2	0	0	1	1	0	1	1	0	54
9	-Vdc	0	0	1	1	1	1	0	0	60

TABLE V
IDENTIFICATION OF THE DEFECTED POWER SWITCH FOR POSITIVE CURRENT I

State	Faulty switch	Conducting components (terminal voltage)	Second step	Conducting components (terminal voltage)
1	S11	DC1, S12, S23, S24 (Vdc/2)	S24 is switched off	DC1, S12, S23, DC4 (0)
1	S24	S11, S12, S23, DC4 (Vdc/2)		S11, S12, S23, DC4 (Vdc/2)
1	S12	D14, D13, S23, S24 (0)	S23 is switched off	D14, D13, D22, D21 (-Vdc)
1	S23	S11, S12, D22, D21 (0)		S11, S12, D22, D21 (0)
2	S11	DC1, S12, S23, DC4 (0)	S11 is switched off	DC1, S12, S23, DC4 (0)
2	S23	S11, S12, D22, D21 (0)		DC1, S12, D22, D21 (-Vdc/2)
2	S12	D14, D13, S23, DC4 (-Vdc/2)		
3	S12	D14, D13, S23, S24 (0)	S12 is switched off	D14, D13, S23, S24 (0)
3	S24	DC1, S12, S23, DC4 (0)		D13, D14, S23, DC4 (-Vdc/2)
3	S23	DC1, S12, D22, D21 (-Vdc/2)		
4	S11	DC1, S12, D22, D21 (-Vdc/2)		
4	S12	D14, D13, D22, D21 (-Vdc)		
5	S12	D14, D13, S23, DC4 (-Vdc/2)	S12 is switched off	D14, D13, S23, DC4 (-Vdc/2)
5	S23	DC1, S12, D22, D21 (-Vdc/2)		D13, D14, D22, D21 (-Vdc)
6	S23	D14, D13, S23, S24 (-Vdc)		
6	S24	D14, D13, S23, DC4 (-Vdc/2)		
7	S12	D14, D13, D22, D21 (-Vdc)		
8	S23	D14, D13, D22, D21 (-Vdc)		

TABLE VI
IDENTIFICATION OF THE DEFECTED POWER SWITCH FOR NEGATIVE CURRENT I

State	Faulty switch	Conducting components (terminal voltage)	Second step	Conducting components (terminal voltage)
2	S22	D11, D12, D23, D24 (Vdc)		
3	S13	D11, D12, D23, D24 (Vdc)		
4	S21	D11, D12, DC3, S22 (Vdc/2)		
4	S22	D11, D12, D23, D24 (Vdc)		
5	S13	D11, D12, S22, DC3 (Vdc/2)	S13 is switched off	D11,D12,S22,DC3 (-Vdc/2)
5	S22	DC2, S13, D23,D24 (Vdc/2)		D11, D12,D23,D24 (-Vdc)
6	S13	D11, D12, D23, D24 (Vdc)		
6	S14	DC2, S13, D23, D24 (Vdc/2)		
7	S13	D11, D12, S21, S22 (0)	S13 is switched off	D11, D12, S21,S22 (0)
7	S21	DC2, S13, DC3, S22 (0)		D11, D12, DC3,S22 (Vdc/2)
7	S22	DC2, S13, D23, D24 (Vdc/2)		
8	S14	DC2, S13, DC3, S22 (0)	S14 is switched off	DC2, S13, DC3,S22 (0)
8	S22	S13, S14, D23, D24 (0)		DC2, S13, D23,D24 (Vdc/2)
8	S13	D11, D12, DC3, S22 (Vdc/2)		
9	S13	D11, D12, S22, S21 (0)	S13 is switched off	D11, D12, S22, S21 (0)
9	S14	DC2, S13, S22, S21 (-Vdc/2)		D11, D12, S22, S21 (0)
9	S22	S13, S14, D23, D24 (0)		D11, D12, D23,D24 (Vdc)
9	S21	S13, S14, DC3, S22 (-Vdc/2)		D11, D12, DC3,S22 (Vdc/2)

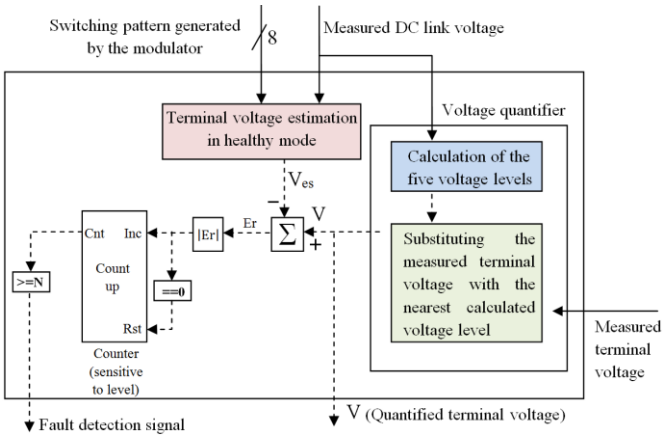

Fig. 2. Proposed fault detection principle.

conducting components. In each switching state, all possible failure modes are considered and the post-fault operation corresponding to these failure modes are studied and analyzed. These analysis and studies are summarized in form of the look up tables (Table V and Table VI). If a real fault occurs, the results obtained are analyzed by means of a so-called failure mode algorithm. This algorithm interprets the look up tables in the form of a flowchart. Table V and Table VI are established for the positive and negative terminal currents, respectively. In order to clarify the approach used to establish Table V and Table VI, some cases are detailed in the following. For the positive terminal current I when the switching state 1 is applied in normal operation, the current flows through S11, S12, S23 and S24 (Table III). After the open-circuit fault occurrence in S11, the terminal current flows through DC1 rather than S11 (Table V). Therefore, the terminal voltage reaches +Vdc/2 rather than +Vdc in healthy mode. In case of an open-circuit fault in S12 at switching state 1 for positive terminal current, freewheeling diodes D13 and D14 conduct instead of S11 and S12. As a result, the terminal voltage drops to zero. Likewise, the presented analysis is applicable to obtain the new current paths and new terminal voltages in case of open-switch fault occurrence in the other half-legs and with negative terminal currents. By observing the results given in Table V and Table VI, it can be concluded that whenever an open-circuit fault occurs in the internal switches, the defected internal switch is replaced by the two freewheeling diodes located in the opposite half-leg. Moreover, in case of an open-circuit fault occurrence in the external switches, the terminal current flows through the clamping diode connected to the same half-leg. It should be

noted that the failure mode analysis results are used for fault localization step after fault detection. By comparing the terminal voltage corresponding to each switching state in Table III (healthy operation) with those of Table V and Table V (post-fault operation), it is deduced that in case of open-switch fault occurrence, magnitude of error value is always greater than or equal to Vdc/2. Thus, the fault detection could be performed for all cases.

III. Principles of the Proposed Fault Diagnosis Approach

A. Fault detection strategy

In a fault diagnosis approach, the fault detection is an indispensable step to be taken prior to the fault localization procedure to detect the open-circuit switch. The proposed fault detection procedure is based on comparing the measured terminal voltage with the predicted terminal voltage, based on a voltage quantifier which is an improved form of the approach presented in [27]-[28]. From the practical point of view, one of the motives for using multilevel inverters instead of conventional inverters is reducing the switching frequency. Thus, the majority of the commonly used industrial voltage sensors can fulfill the required bandwidth. The estimation of the terminal voltage is realized by considering the switching pattern applied to the power switches and the DC link voltage value. In fact, the control signals already available in the control system meet the fault detection requirements. Hence, additional sensors are not needed. In the applied fault detection strategy, some constraints may be problematic. Even in the healthy mode operation, at any instant of the operation, there is discrepancy between the measured terminal voltage and its estimated value, mainly due to voltage drop in the components, turn off and turn on delay times of the power switches, response time of the sensors and measurement errors. As depicted in Fig. 2, a voltage quantifier which differentiates the proposed fault detection strategy from the aforementioned works is devised to compensate the voltage measurement error and also to compensate the voltage drop. In normal operation, the measured terminal voltage is close to one of the five voltage levels in terms of DC link voltage presented above (terminal voltages in Table III). Therefore, the voltage quantifier assigns the nearest terminal voltage level, based on DC link voltage measurement to the measured terminal voltage. Thus, the measured terminal voltage value is replaced by the quantified voltage value, calculated from the same DC link voltage value (see Fig. 2) which is also used for terminal voltage estimation. Since the quantified measured voltage is also applied in fault localization procedure, all of the mentioned benefits obtained thanks to the voltage quantification are applied in the fault localization procedure. Due to the delay and dead time between the measured and estimated terminal voltage, even in normal operation, the present switching pattern does not correspond to the measured voltage. In other words, the present measured terminal voltage corresponds to the previous switching pattern. In order to get rid of this problem, as depicted in Fig. 2, a counter is employed. If the voltage error subsists beyond the up limit value, it means that this voltage error is resulted from an open-switch fault and consequently the fault declaration signal is generated. Otherwise, the error value is originated from the transitional conditions (the commutations), the system imperfections, sensor response time and delays. The up limit value of the counter is determined based on the overall delay due to the sensors, drivers, controllers and switches presented by the manufacturers.

B. Fault localization strategy

After detection of the open-switch fault occurrence, the fault localization strategy is initiated, which is based on the failure mode analysis. Similar to the fault detection procedure, it does not require any external circuits and sensors. In Table V and Table VI, for all of the possible switching states with positive and negative load current I, the post-fault analysis is summarized. As shown in Table V and Table VI, in case of open-circuit fault occurrence in external switches S11, S14, S21 and S24, the faulty switch necessarily is identified after performing a switching pattern modification (second step) while in case of the open-circuit fault in internal switches S12, S13, S22, and S23, the defected switch is located directly or after a second step, which depends on the applied switching state. Knowing the last applied switching state (just before fault detection) and the load current sign, the fault localization algorithm locates the relevant subsection in Table V or Table VI (state number with current sign). Afterwards, the measured terminal voltage which has been quantified in the fault detection procedure is compared with the expected terminal voltages, which are estimated by assuming the open-circuit fault occurrence in each power switch forming the current path. In this regard, giving an example in the following would be helpful to clarify the employed fault localization algorithm. To this end, it is supposed that S11 is the faulty switch and the open-switch fault is detected when the switching state 1 is applied while the load current is positive. As depicted in Table III, in switching state 1 for positive load current, the switches S11, S12, S23, and S24 form the load current path in healthy mode operation. Hence, in the subsection established in Table V corresponding to state 1 with positive current, the new conducting components and subsequently the new attained terminal voltages in case of the open-circuit fault in S11, S12, S23 or S24 are represented. As S11 is supposed to be the faulty switch, the quantified terminal voltage equals to Vdc/2. By comparing this value with the estimated post-fault values (here, Vdc/2 or 0), it could be concluded that S11 or S24 is defected but the faulty switch cannot be determined distinctly. To overcome this issue, a second step is to be taken. In the presented example and as demonstrated in Table V, in the second step, we remove the gate signal of S24. In this case, according to the new current paths, two different terminal voltages could be obtained. Thus, the updated quantified value equals to 0. Consequently, by comparing the quantified value with the estimated values in the second step, it is deduced that S11 is the defected switch. The situations in which performing the second step is mandatory to distinguish the faulty switch

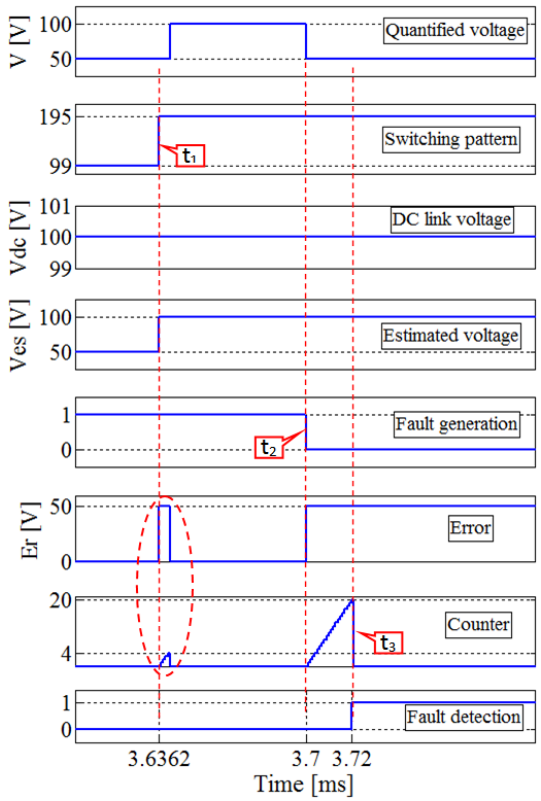

Fig. 3. Fault detection procedure in case of open-circuit fault occurrence in S11.

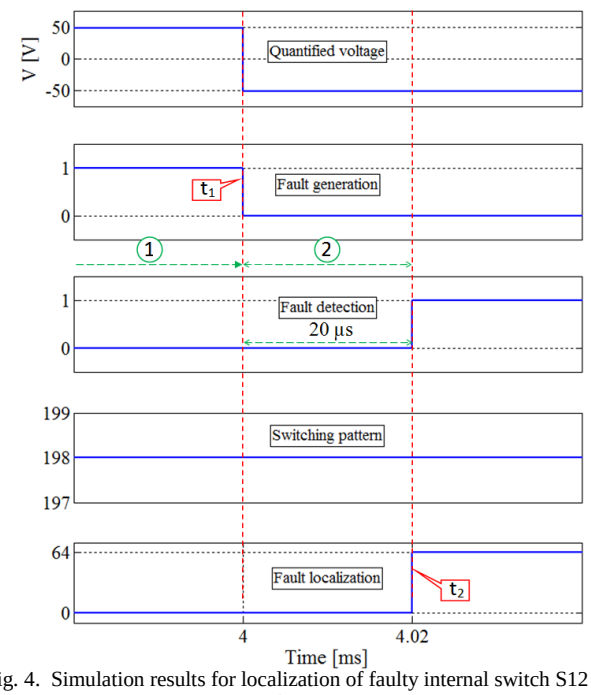

Fig. 4. Simulation results for localization of faulty internal switch S12 in the first step.

distinctly, are represented in Table V and Table VI for the positive and negative load currents, respectively. It should be noted that once the fault detection is declared, the switching states generated by the modulator are no longer applied to the power switches. Subsequent to the fault detection, the fault identification module takes action to identify the faulty component. As mentioned earlier, it can directly identify the faulty component (identification in the first step) or it switches off a certain switch (identification in the second step).

IV. Simulation Results

The simulation results are classified into two sections. In the first one, solely the fault detection strategy is demonstrated. The second one presents the simulation results regarding the fault localization. It should be noted that in all sections the load resistance, the load inductance, the switching frequency, the fundamental frequency, the DC link capacitors, the DC link voltage and modulation index are 27.7 Ω, 9 mH, 1 kHz, 50 Hz, 2.2 mF, 100 V and 0.8, respectively. Since the converter topology is symmetric, the simulation results are solely presented for the positive load current. Sine-PWM modulation has been used to generate the switching patterns. It should be noted that the proposed fault diagnosis strategy is independent from the type of modulation technique.

A. *Fault detection strategy*

Since principles of the proposed fault detection strategy are similar for all of the switches, S11 is arbitrarily chosen as a case study. As shown in Fig. 3, at instant t_1 (healthy condition), the switching pattern changes from 99 (state 3) to 195 (state 1) which according to Table IV corresponds to terminal voltage change from +Vdc/2 to Vdc. Although this variation occurs in healthy mode, the error due to the dead times and delays indicates the discrepancy between the quantified and the estimated voltage values during the short transient time. Since the error value does not subsist noticeably, the counter output (Fig. 3) does not reach the maximum limit (here N=20, Fig. 2). Thus, any fault detection is not declared. At instant t_2 (state 2), an open-circuit fault occurs in S11. In compliance with Table V, the quantified terminal voltage drops to +Vdc/2 while the estimated voltage which depends on the switching pattern, remains in +Vdc (Table IV, state 1). Therefore, the error signal reaches +Vdc/2 and remains in this value. Once the counter reaches the upper limit N at instant t_3, the fault detection signal is generated.

B. *Fault localization strategy*

In order to locate the defected internal switch, depending on the last applied switching pattern in healthy operation, one or two steps should be taken while for identifying a faulty external switch, two steps must always be carried out. Thus, there are two distinct situations in which the corresponding simulation results are discussed in the following.

As to demonstrate the fault localization procedure for the internal switches in the first step, the case depicted in Fig. 4 corresponds to the fault localization approach for S12. In Fig. 4, just before the fault generation at instant t_1, the quantified voltage and switching pattern are equal to +Vdc/2 and 198 (switching state 2), respectively. Thus, by referring to Table V, it is observed that S11, S12, S23 and DC4 form the current path just before the fault generation in S12. Once the fault occurs in S12, the quantified voltage drops to –Vdc/2 which conforms to the failure mode analysis presented in Table V. In accordance with Fig. 4, the faulty switch S12 is immediately

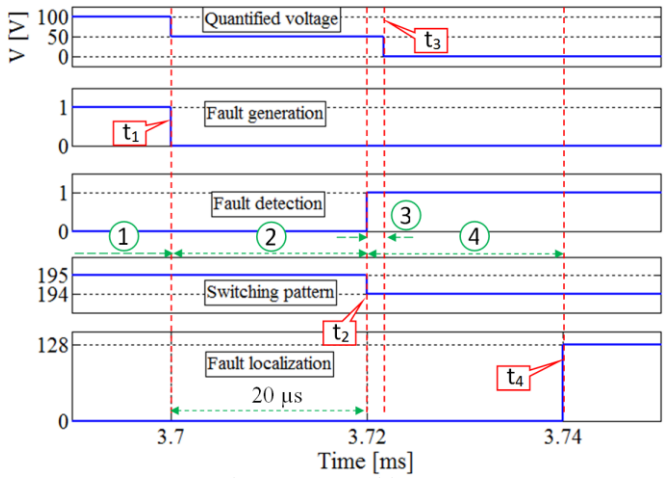

Fig. 5. Simulation results for localization of faulty external switch S11 in the second step.

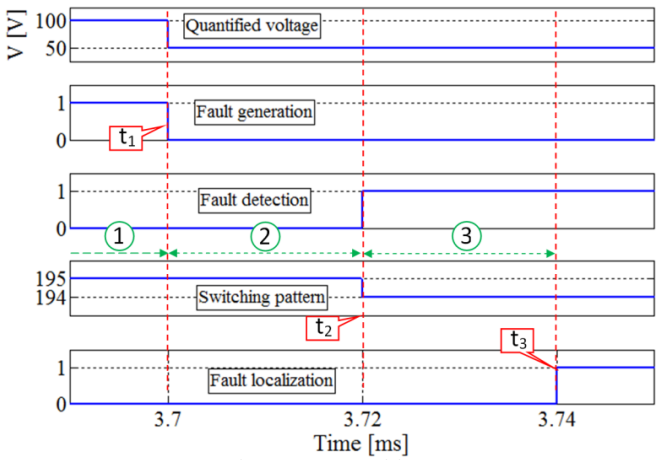

Fig. 6. Simulation results for localization of faulty external switch S24 in the second step.

identified at instant t_2 once the fault detection is declared because in this case only a single step should be taken. It should be noted that for better representing the faulty switch in the simulations, specific numbers are assigned to the power switches. The numbers 128, 64, 32, 16, 8, 4, 2, and 1 are assigned to S11, S12, S13, S14, S21, S22, S23, and S24 respectively. Likewise, the single step fault localization procedure could be realized for the other cases. Hereafter, the two step fault localization procedure for external switches S11 and S24 is discussed. The simulation results regarding the fault localization approach in external switches S11 and S24 in the second step are represented in Fig. 5 and Fig. 6, respectively. As shown in Fig. 5, before instant t_1 (interval 1), the inverter operates in healthy mode during which the terminal voltage and switching state are equal to +Vdc and 195 (switching state 1). Therefore, just before the fault generation in S11 at instant t_1, current flows through S11, S12, S23 and S24. Once the open-circuit fault is generated in S11 at instant t_1, the quantified voltage drops to +Vdc/2 which is justified by Table V. Hence, at instant t_2 (at the end of interval 2) the fault is declared. However, the faulty switch identification is not still possible because by referring to Table V, an open-circuit fault occurrence in S11 or S24 leads to the

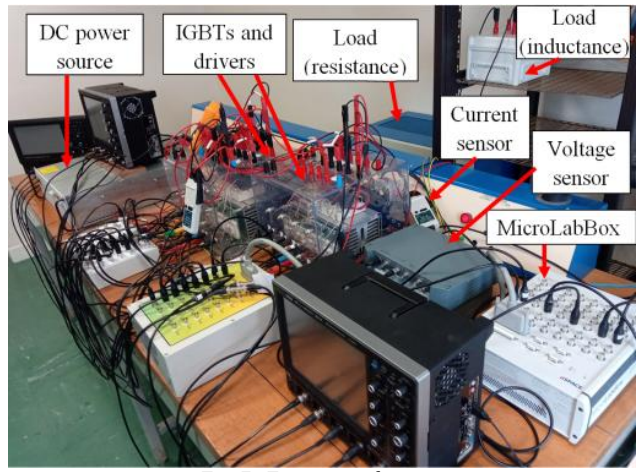

Fig. 7. Experimental setup.

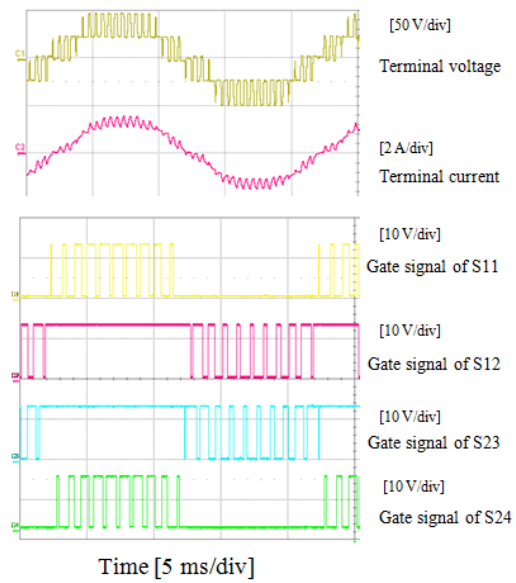

Fig. 8. Experimental results for inverter operation during healthy condition.

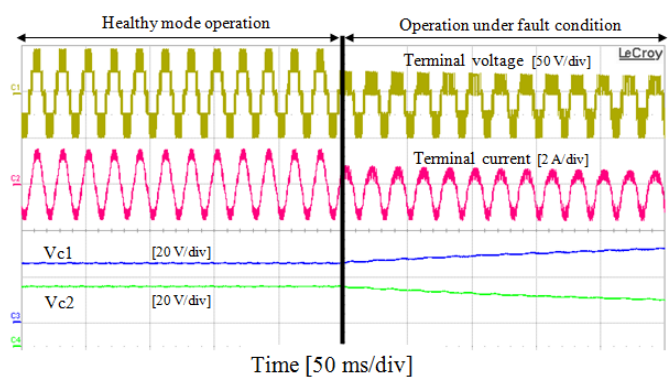

Fig. 9. Experimental results of the inverter operation under fault event in S11 without fault diagnosis.

same quantified voltage +Vdc/2 at the first step. Inevitably, the second step is to be taken in which the gate signal of S24 is removed once the fault detection is declared at instant t_2 as observed in Fig. 5. By opening S24, the current path according to Table V is formed of DC1, S12, S23 and DC4. Consequently, the quantified voltage reaches 0 at instant t_3 due

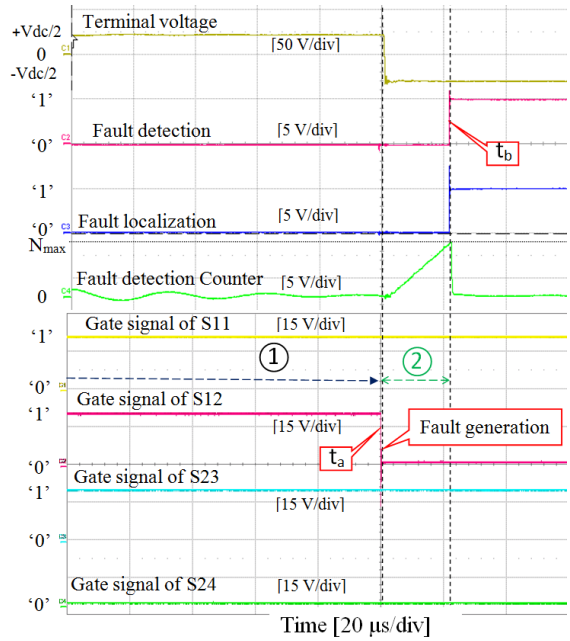

Fig. 10. Experimental results for localization of faulty internal switch S12 in the first step.

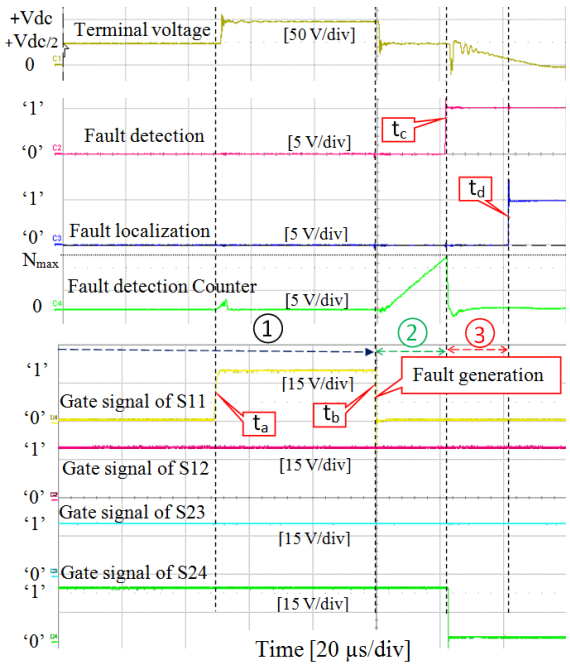

Fig. 11. Experimental results for localization of faulty external switch S11 in the second step.

to the delay time arising from commutation (interval 3). In accordance with Table V, the faulty switch S11 is identified, which is indicated by the simulation results demonstrated in Fig. 5 at instant t_4. It should be mentioned that in this case study, the fault localization is declared at the end of time interval 4 (chosen in accordance with N value for fault detection procedure) to prevent wrong fault localization due to the existing dead times and delays. Likewise, a similar analysis is employed to justify the fault localization procedure represented in Fig. 6 for faulty switch S24. In case of the fault occurrence in S24, the quantified voltage after removing the gate signal of S24 in the second step remains equal to +Vdc/2.

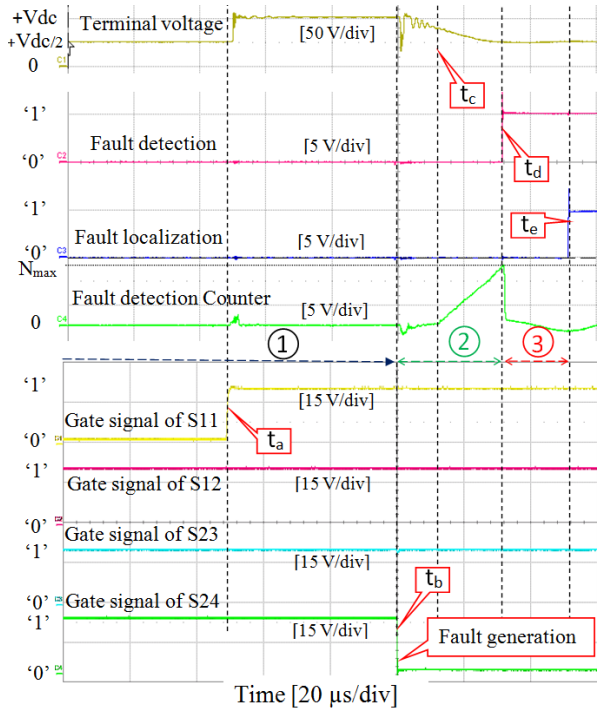

Fig. 12. Experimental results for localization of faulty external switch S24 in the second step.

Likewise, fault localization strategy employed to identify any defected switch has been validated by simulation.

As mentioned previously, each phase of a three-phase five-level NPC/H-bridge inverter is comprised of a single-phase five-level NPC module. Since each module in a three-phase five-level NPC/H-bridge topology operates independently of the other modules located in the other phases, the fault diagnosis for each phase (each module) can be carried out independently. Moreover, the presented strategy can be applied to a cascaded NPC/H-bridge inverter. In this case, each NPC module requires independent fault diagnosis equipment. The proposed strategy is applicable to T-Type and Active-NPC (A-NPC) topologies. The proposed algorithm solely takes into consideration the switching states generated by the modulator irrespective of the modulation technique. However, for the other topologies (T-Type or Active-NPC), the look up tables should be adapted but the principle of establishing the look up tables would be the same. It should be noted that the diagnostic strategy is designed in such a way that after fault identification, the system operation is stopped and any signal is no longer applied to the power switches. Hence, after faulty component identification, the occurrence of the second fault is not to be considered because the system operation is stopped. On the other hand, in accordance with the presented results in the paper, the fault identification is carried out quickly (in range of some tens of μs). In other words, the time interval between a fault event and the corresponding fault identification is very short. Hence, the second fault occurrence in this interval is very unlikely. However, if the second fault happens during this short interval, the proposed strategy is not able to identify the second fault event.

V. Experimental results

For the implementation of the modulator and the fault diagnosis parts (the fault detection and fault localization), a MicroLabBox (one of the dSPACE platforms) containing a processor and an FPGA chip (Xilinx® Kintex®-7 XC7K325T) is used. Since the diagnosis part is logic based and does not contain complicated calculation, it is implemented on the FPGA chip and the modulator is implemented on the processor. The inverter is constituted of the IGBTs SKM50GB123D of SEMIKRON, commanded by SKHI22A drivers. The experimental setup is shown in Fig. 7. For the experimental setup, the load resistance, the load inductance, the switching frequency, the fundamental frequency, the DC link capacitors, the DC link voltage and modulation index are 27.7 Ω, 9 mH, 1 kHz, 50 Hz, 2.2 mF, 50 V and 0.8, respectively. The open-circuit fault condition is obtained by removing the gate signal of the relevant switch. In the experimental results, switching pattern is illustrated by four IGBTs gate signals. Based on these four IGBTs gate signals, the switching state can be determined according to Table IV because the command signals corresponding to the other four IGBTs are complementary. Moreover, similar to the simulation section, the results are only represented for fault occurrence in case of a positive current to avoid the verbosity. In this section, first of all, experimental results obtained for healthy operation of the inverter are presented in Fig. 8. Then, the operation of inverter under open circuit fault condition in S11 without fault diagnosis is illustrated. In order to avoid verbosity, solely the results concerning S11 are presented. Afterwards, the experimental results corresponding to the open-circuit fault localization approach for S12 (in the first step) are explained. Afterwards, the fault diagnosis procedures corresponding to the IGBTs S11 and S24 (in the second step) are represented by the experimental results.

As can be seen in Fig. 9, subsequent to fault occurrence in S11, the DC link capacitors' voltages diverge from their rated values. It can be deduced that in this inverter, in case of an open-switch fault, one of the DC link capacitors would be subject to overvoltage. It should be mentioned that in this case, the inverter is not equipped with open-switch fault diagnosis. Thus, in case of fault event, a fast and efficient fault diagnosis method is required to stop operating as quick as possible.

As shown in Fig. 10, during interval 1, the inverter operates in healthy mode. According to the gate signals and referring to Table IV, the switching state 2 is applied, which conforms to the terminal voltage +Vdc/2. Once the open-circuit fault occurs at instant t_a (by setting the gate signal of S12 to 0), the terminal voltage drops to -Vdc/2, which can be justified by the failure mode analysis presented in Table V. At the instant t_b, the counter reaches the maximum predefined value and the fault is declared and subsequently the faulty component is identified immediately.

As depicted in Fig. 11, during interval 1, the inverter operates in healthy mode. In accordance with the represented command signals and Table IV, just before the open-circuit fault generation at the instant t_b, switching state 1 is applied (corresponding to the terminal voltage +Vdc). Once the open-circuit fault is generated in S11 at instant t_b, the terminal voltage attains +Vdc/2 (which complies with the Table V). Due to the established discrepancy between the measured terminal voltage (+Vdc/2) and the terminal voltage corresponding to switching state 1 (+Vdc according to the Table IV), the counter starts to count. At the end of the interval 2, the counter reaches the maximum predefined value. Hence, the fault is declared at instant t_c and the localization procedure is triggered. According to the Table V, it is not still possible to distinguish the defected component between S11 and S24. Thus, once the fault occurrence is declared, the gate signal of S24 is set to zero (complying with the Table V for the fault localization purpose). Thus, the terminal voltage drops to zero and at instant t_d, the faulty switch is identified. As mentioned in the analysis of the simulation results, interval 3 (chosen in accordance with N_{max} value for fault detection procedure) prevents wrong fault localization due to the existing dead times and delays. Likewise, a similar analysis is employed to justify the fault localization procedure represented in Fig. 12 for faulty switch S24. In case of the fault occurrence in S24, the terminal voltage after removing the gate signal of S24 in the second step remains equal to +Vdc/2.

VI. Conclusion

This paper presents an open-switch fault diagnosis method for an NPC/H-bridge inverter. In this paper, a single-phase structure is considered. The same approach can be applied to three-phase NPC/H-bridge converter. The presented strategy not only detects the open-switch fault occurrence but can also in any case identify the defected component fast and efficiently. The necessary signals and measurements such as the DC link voltage, the terminal voltage, the switching pattern and the current sign are available in the control section. In this respect, any additional sensors or circuits are not required compared with the surveyed researches. Furthermore, the proposed strategy does not require complicated calculations, component modeling or load parameters. In addition, for fault detection procedure, an efficient method using a voltage quantifier, independent of determining the error threshold value has been presented to avoid erroneous fault detection due to the components voltage drop and measurement errors. The represented simulation results confirm the effectiveness and fastness of the presented fault diagnosis strategy (the fault detection in 20 µs according to the chosen N value). Failure mode analysis used for fault localization procedure is logic based and does not require complicated and tedious calculation. Thus, the failure mode analysis can be implemented on a small size FPGA chip and the modulator can be implemented on a processor. An FPGA chip is used for fast fault detection and fault localization in parallel with the control system, which leads to high time performance. The only parameters limiting the temporal performance of the presented approach are intrinsic characteristics and imperfection of the components that cannot be avoided. The simulation and experimental results validate the effectiveness and rapidity of the proposed approach.

During fault identification procedure, the diagnosis module takes action independently from the modulator. In other words, during fault localization, the FPGA chip still receives the commands generated by the modulator but it does not apply them to the power switches. Thus, the feed-back signals or switching frequency variation does not affect the diagnosis procedure. Furthermore, by employing the counter and voltage quantification, the consequences arising from the noise are suppressed and misdiagnoses are avoided.

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