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# Reliable FPGA-based Solar Energy Production

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**Abstract**—This paper presents a stand-alone photovoltaic (PV) system with a hybrid storage unit operation under normal and faulty condition. An energy management method based on the use of a hybrid storage for the solar energy production system is presented. The storage system consists a battery and an Ultra Capacitor (UC) pack. The UCs are used for facing high frequency variation of the load/source, while the batteries are in charge of slow load /source variations. Generally, in a PV system boost converters are used to connect solar panels to the DC bus. These converter allows to achieve the maximum power of the PV source by applying a Maximum Power Point Tracking (MPPT) algorithm. On the other hand, the power electronic semiconductor switch faults are popular in DC-DC converters. In order to improve the micro-grid service continuity and reliability, a fast fault detection method based on the converter current shape and one redundancy based fault tolerant converter for PV source is proposed in this paper. The validity of the proposed energy management and associated control system, the fault detection method and fault tolerant strategy are confirmed by the simulations, HIL and experimental results.

**Keywords**—Solar energy; photovoltaic; energy management; hybrid power system; Fault detection; Fault tolerant.

## I. INTRODUCTION

The last decades have shown a growing interest in DC-DC power conversion in industrial applications mainly in renewable energy power systems. Nowadays, islanded PV systems have a significant penetration in many applications such as space systems, telecommunication, solar battery charging stations, electric vehicles, meteorology stations, residential and commercial installations, as well as parts of hybrid power systems [1], [2]. In such embedded or safety critical applications, a high level of system reliability is mandatory [3]. In this paper two important issues that can affect the reliability and service continuity of the system are considered: energy management strategy and fault tolerant operation.

The energy balance on the common bus of the system is the first important criteria to have reliable normal operation. To ensure energy balance between sources and loads in a system, an effective energy management strategy is required.

Several papers have studied energy management methods in microgrids [4]–[7]. In these works, different types of energy sources, such as wind energy, fuel cell, photovoltaic, micro turbine and etc. are considered. The major challenge to use photovoltaic system as a main power supply is that PV power is not available during night and cloudy days. That is why the integration of the ESS is mandatory to reduce the uncertainty of the PV generation and to enhance the stability and reliability of such microgrids [4].

On the other hand, PV systems have a complex structure and are vulnerable to faults. A failure may occur in any part of the system such as PV panel, power converter or sensor. The DC-DC step-up converters that are usually used to perform MPPT in PV systems [8]–[10], have the failure rate up to 41% [11] where, the semiconductor failures take up 34% of power electronic

system failures [12]. Therefore, a fast Fault Detection Method (FDM) and Fault Tolerant (FT) operation for these converters should be proposed in PV systems reliability studies.

A few works have studied switch fault detection for isolated DC-DC converter and associated FT topologies, especially based on H-bridge as in [13], [14]. In [15], Ribeiro *et al* have proposed a switch FDM in DC-DC converters and FT converter topologies dedicated to PV systems. In [16], an Open Circuit Fault (OCF) detection method based on comparison of the duty cycle with the inductor current slope. In [17] and [18], a FPGA-based switch fault detection method for non-isolated DC-DC converter is proposed. This approach is based on the inductor current slope observation. The proposed method in [17] can detect both types of fault (OCF and Short Circuit Fault (SCF)) in two switching periods but cannot identify the type of failure, while, the proposed method in [18] identifies the both types of failures and it has fault tolerant capability. In [25], an alternative OCF diagnosis method for boost interleaved DC-DC converters operating in unidirectional power flow, using in PV system, is studied. This method is based on features of the DC-link current derivative sign during fault and healthy operations.

In this paper, an energy management strategy is studied and verified by simulation on a DC microgrid. The studied power system consists of a PV source, a battery pack, an ultra capacitor and some different loads, which are also connected to a common DC bus. Also a fast fault tolerant operation based on FPGA is proposed for the DC-DC converter of the PV source. The validity of the proposed method is confirmed by the experimental results.

In the following section, the studied system and its modeling is first introduced. In section III, the energy management strategy and system control are presented. Fault diagnosis and fault tolerant operation is expressed in section IV. Simulation and experimental results, which validate the performances of the proposed method, are presented in Section V. The paper is finalized by some conclusions in section VI.

## II. SYSTEM DESCRIPTION AND SYSTEM MODELING

The studied system is shown in Fig. 1. This system consists of a photovoltaic (PV source) that is connected to the DC bus via a fault tolerant boost converter to guaranty the service continuity. A MPPT (Maximum Power Point Tracking) algorithm is applied on this boost converter to achieve the PV maximum produced power.

A model of moderate complexity for a solar cell was used as shown in Fig. 2 (a). This model, which is presented in many papers, is a current source in parallel with a diode and a series resistance  $R_s$ . In this model, the net current  $I$  can be expressed as follows:

$$I = I_{ph} - I_D = I_{ph} - I_0 \left( e^{\frac{q(V+IR_s)}{mkTc}} - 1 \right) \quad (1)$$

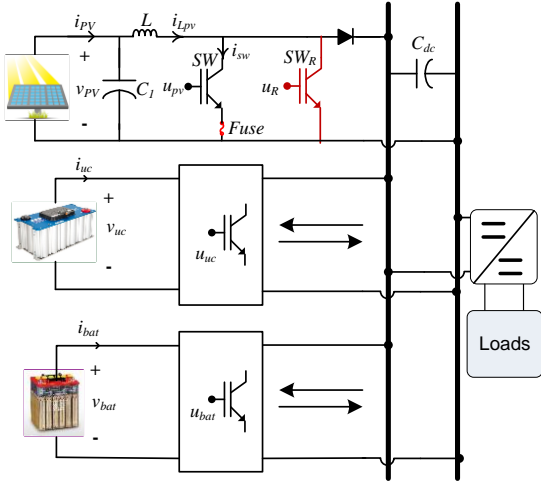


Fig. 1 Studied microgrid.

Where  $m$  is the idealizing factor,  $k$  is the Boltzmann's gas constant,  $T_c$  the absolute temperature of the cell,  $q$  the electron charge and  $I_0$  is the dark saturation current, which is strongly depending on the temperature.

An Ultra Capacitor (UC) that have fast dynamics, is used as a storage element in order to smooth fast fluctuations of the PV power and the loads in short-term (from seconds to minutes). The model proposed by Zhang and Yu in [26] which is shown in Fig. 2 (b) is used in this paper. This model consists of three parameters: a capacitance  $C_{UC}$ , an equivalent series resistance  $R_{UCS}$  representing the charging and discharging resistance, and an equivalent parallel resistance  $R_{UCP}$  representing the self-discharging losses. The voltage  $v_{UCi}$  over the capacitance  $C_{UC}$  is the open-circuit voltage.

Since the dynamic of the battery pack is slower than that of the UC, therefore the batteries are used to smooth the difference between the PV produced power and load demand in long-term (from minutes to hours). Among the various battery models are published in the literature, the one was proposed in [7], [27], [28] is used in this paper and is shown in Fig. 2 (c). The relationship of the battery terminal voltage  $v_{bat}$ , open-circuit voltage  $V_{emf}$ , charge/discharge current  $i_{bat}$  and internal resistance  $R_1$  and a parallel  $R_C$  circuit which illustrates charge transfer and the diffusion between the electrode and the electrolyte [10], [28] is expressed by (2):

$$V_{bat} = V_{emf} - I_{bat} * \left( R_1 + \frac{R_2}{1 + C_b * R_2 * s} \right) \quad (2)$$

The UCs and the battery are connected to the DC bus through the bi-directional DC-DC converters that allows energy exchange between them, loads and PV source.

Losing the instantaneous balance between supply and load can be affected the stability of the system that is the most important problem in normal operation. Therefore, an energy management algorithm is mandatory. The system control is detailed in the following section. And then the fault tolerant operation will be presented.

### III. ENERGY MANAGEMENT STRATEGY AND CONTROL

To control and optimize energy management in DC networks some methods have been presented in the literature [6], [10], [13], [26]-[30]. In this paper, a global control loop based on DC bus energy balancing is proposed for system's energy management.

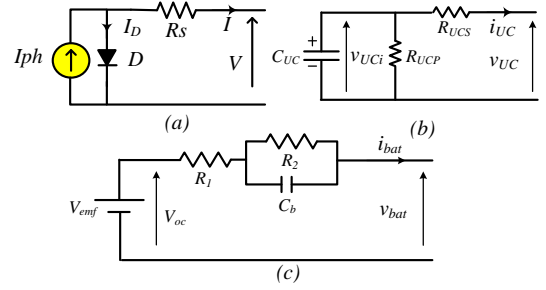


Fig. 2 (a) Pv celul model, (b) UC model (c) Battery model.

#### A. DC bus voltage control

The DC bus voltage control is shown in Fig. 3. The energy of the DC bus ( $y_{dc}$ ) varies according to the power consumed or supplied by the connected subsystems. If we can maintain constant  $y_{dc}$ , the DC bus voltage can be regulated to its set value ( $V_{dcref}$ ). The control strategy used for the battery pack, the UC and the PV source has different dynamic and aims different objectives:

- The UC, which is the fastest energy storage element, is responsible for regulating the DC bus when a rapid change appears in the load.
- The battery pack is supposed to regulate the energy stored in the UC.
- The power of the PV source depending on irradiation and temperature, controlled by MPPT.

As Fig. 3 shows DC voltage control consists of two loops. The outer loop's role is to regulate the energy  $y_{dc}$ , while the inner loop regulates the current  $i_{uc}$  of the UC (see Fig. 3). The stored energy in the DC bus capacitor ( $y_{dc} = \frac{1}{2} C_{dc} v_{dc}^2$ ). As we have already mentioned, the sum of all powers in and out of the DC bus must be zero at any time. The derivative of the  $y_{dc}$  may be expressed by equation (3). The  $p_{pv}$ ,  $p_{bat}$ ,  $p_{uc}$  and  $p_L$  are provided (or absorbed) powers by the PV, the battery, the UC and the load respectively.

$$\dot{y}_{dc} = p_{dc} + p_{bat} + p_{pv} - p_L \quad (3)$$

The reference value of the UC's power ( $p_{ucref}$ ) which compensates the rapid load variations can be expressed as in equation (4), where the  $p_{uc/dc}$  is the power that must be provided (or stored at a given time) by the UC. This assures the DC bus energy ( $y_{dc}$ ) regulation.

$$p_{ucref} = p_{uc/dc} - p_{bat} - p_{pv} + p_L \quad (4)$$

Finally, the reference of the UC's current ( $i_{ucref}$ ) can be calculated by dividing  $p_{uc/dc}$  by the voltage measured at the UC.

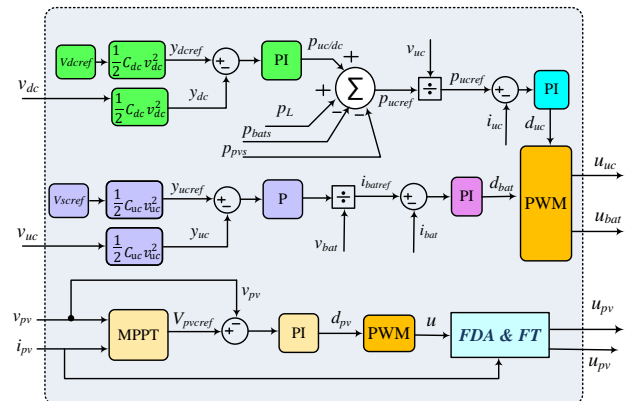


Fig. 3 Energy management control and fault diagnosis bloc diagram.

### B. Ultracapacitor energy control

According to the control strategy previously established, the battery pack regulates the energy of the UC ( $y_{uc} = \frac{1}{2} C_{uc} v_{uc}^2$ ). For this, a control architecture including two loops is proposed. The outer loop is responsible for the regulation of energy  $y_{uc}$  stored in the UC and the inner loop is used to regulate the current of the battery at its set-point value. The control method is identical to that used for the control of the  $y_{dc}$ . Fig. 3 shows the control strategy.

### C. PV maximum power extraction and control

In order to optimize the operation of a PV source, it is important to follow the maximum power by a MPPT algorithm. In recent years, several MPPT methods have been published [10], [31]–[33]. Among these methods, we have chosen in this paper the P&O algorithm (Perturb and Observe) which is based on the principle of a small amplitude voltage disturbance  $v_{pv}$  on its initial value, by acting directly on the duty cycle of the PV's DC-DC converter. As illustrated in Fig. 3 after setting the reference value of the  $v_{pv}$  by MPPT algorithm, the PV converter control system is generated through a PI controller and a PWM block. The FDA & FT bloc is the fault diagnosis algorithm that will be presented in the next section. The energy management and voltage control is detailed in [26].

## IV. FAULT DIAGNOSIS AND FAULT TOLERANT OPERATION

Fault tolerance in a power converter requires three steps: fault detection, fault identification and remedial actions. The proposed FDM has the capability to do the first two steps (detection and identification) simultaneously by using the switch command signal and the sign of the inductor current slope, provided by the current sensor used in the system control. The maximum detection time is one switching period. The proposed method is described in the following.

Fig. 4 shows a boost converter, its switch command signal ( $u$ ) and inductor current  $i_L$ . According to Fig. 4, one switching period ( $T_{sw}$ ) can be subdivided into two cycles of converter operation: Cycle1 for switch SW on and Cycle2 for switch SW off. The proposed algorithm is based on the fact that when the switch is on (Cycle1) the inductor current ( $i_L$ ) increases and when the switch is off (Cycle2) it decreases. If  $i_L$  is always increasing or decreasing during one switching period, it can be concluded that a failure has occurred.

To realize the proposed fault detection method, a State Machine (SM) with five inputs ( $T_1$ ,  $T_2$ ,  $T_3$ ,  $T_4$  and the sign of the inductor current slope ( $sgn$  signal)), eight states and two outputs (SCF and OCF) is used, as shown in Fig. 5. The PWM switch commands,  $T_1$  and  $T_2$ , are generated by a 15 kHz carrier triangular signal (Fig. 6). According to this Figure,  $T_1$  and  $T_2$  are corresponding to rising-edges and falling-edges of the switching command ( $u$ ) respectively. It is clear that by each pulse of  $T_1$ , the inductor current  $i_L$  increases and by  $T_2$  this current decreases. The  $T_3$  and  $T_4$  signals are activated in the middle of the Cycle1 and Cycle2 respectively. When the carrier signal is equal to zero  $T_3=1$  and  $T_4$  goes to '1'. Thus, these two signals ( $T_3$  and  $T_4$ ) are

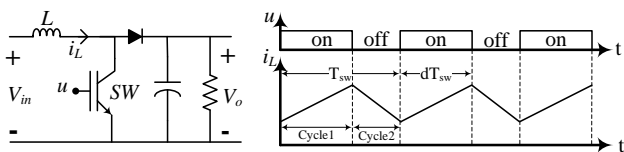


Fig. 4 Boost converter and operation cycles.

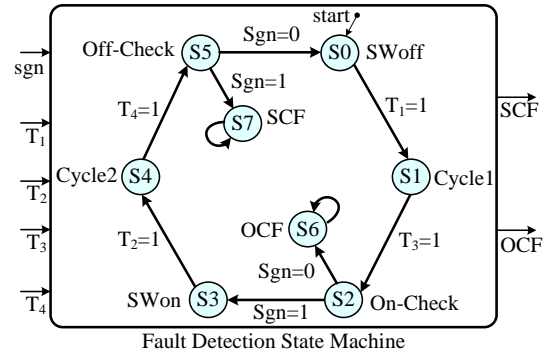


Fig. 5 The state machine used for FDM.

independent from the system controller and just depend on the carrier signal.

Besides, this algorithm only needs the sign and not the exact value of the inductor current slope. This one is obtained by comparing the value of  $i_L(t)$  with its value at  $T_{sgn}=4T_s$  before, where  $T_s$  stands for the sampling time. When  $i_L$  increases,  $sgn=1$  and it is equal to '0' when the current decreases.

### A. Open Circuit Fault detection

As illustrated in Fig. 5, in initial state ( $S_0$ ), the switch is off, i.e.  $u=0$ , and SM stays in this state until  $u=1$  and  $T_1=1$ ; then a transition to state  $S_1$  (Cycle1) occurs. In state  $S_1$ , when  $T_3$  goes to '1', a transition to  $S_2$  occurs, this state allows to verify the on state of the switch SW. In state  $S_2$  (On-Check), the converter is in the middle of Cycle1:

- If no failure has occurred, the switch SW should be on,  $i_L$  increases and  $sgn=1$  thus a transition to state  $S_3$  occurs.
- If an OCF has occurred,  $i_L$  decreases and  $sgn=0$ . Therefore, a transition to  $S_6$  occurs and SM stays in this state.
- In  $S_6$ , the OCF signal (output of the SM) goes to '1' and an OCF is declared. Fig.7 (a) shows the signals and transitions for OCF detection.

### B. Short Circuit Fault detection

For SCF detection, the SM transits from  $S_0$  to  $S_2$  are the same as in OCF case. In  $S_2$  (On-Check), the converter is in the middle of Cycle1, if no failure has occurred (or in a SCF case), the switch SW is in on state,  $i_L$  increases and  $sgn=1$  thus a transition to  $S_3$  occurs. State  $S_3$  corresponds to the on state of switch SW, SM stays in this state until  $u=1$  and then a transition to  $S_4$  occurs when  $T_2=1$ . According to Fig. 5,  $S_4$  coincides with Cycle2. In the middle of Cycle2, signal  $T_4$  goes to '1' and then a transition to  $S_5$  occurs. In state  $S_5$  (Off-Check), the converter is in Cycle2 and the switch SW should be off:

- If no failure has occurred,  $i_L$  decreases and  $sgn=0$  thus a transition to  $S_0$  occurs.
- If a SCF has occurred,  $i_L$  increases and  $sgn=1$ , thus a transition to  $S_7$  occurs and SM stays in this state.

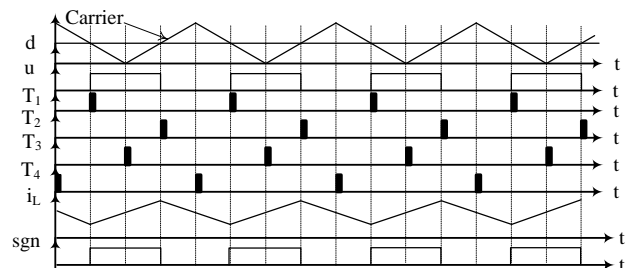


Fig. 1. Input signals of the State Machine.

- In state S7 the signal SCF goes to '1' and a short circuit fault is declared. Fig. 7 (b) shows the signals and SM transitions for SCF detection.

It should be noted that as a result of non-ideal behavior of power switches, delays and dead times are inevitable. Furthermore, the needed time ( $T_{\text{delay}}$ ) to determine the sign of the inductor current (sgn) should be considered. Therefore, even in healthy operation of the converter, the sgn signal is delayed with respect to the switching commands. This is why the state (on or off) of the switch SW is verified right in the middle of Cycle1 (S2) and Cycle2 (S5) in order to take into account these delays and dead times.

### C. Fault tolerant operation

To ensure service continuity of the PV boost converter after a fault detection and identification, remedial actions are necessary. These actions consist of two parts: fault isolation and system reconfiguration. The proposed FT topology is depicted in Fig.3. According to the type of switch failure (OCF or SCF), different reconfiguration strategies are considered. If an OCF occurs, after fault identification by FDM block, the faulty switch can be immediately replaced by the redundant switch SW<sub>R</sub> (Fig.3). But, in case of SCF, as long as the SCF is present on the switch, SW cannot be replaced by the redundant switch. In fact, in SCF case, after fault detection, first the faulty switch should be isolated by means of fuse protection [24]. After fault detection, identification and isolation, the faulty switch (SW) will be replaced by the switch SW<sub>R</sub>. Then, the converter can operate in normal conditions.

### D. fault-tolerant control implementation on a FPGA chip

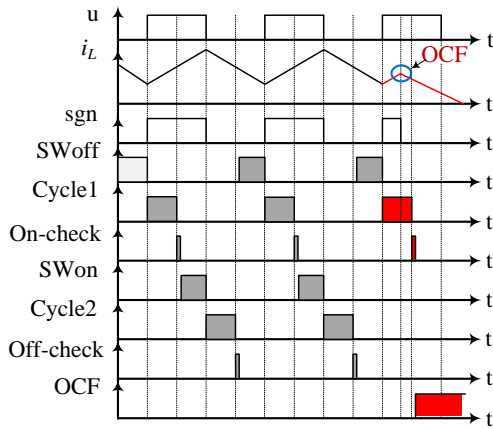


Fig. 7 OCF detection based on FDM signals.

In this paper, a design methodology based on FPGA (Field Programmable Gate Array) rapid prototyping, so called "FPGA

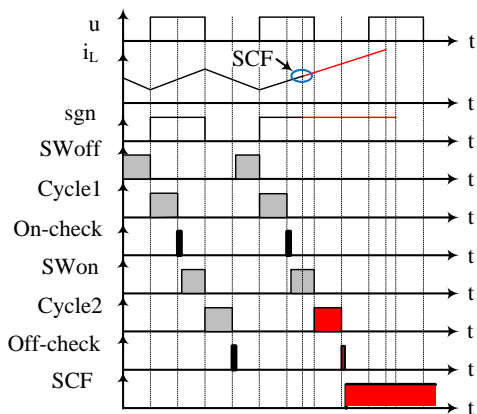


Fig. 8 SCF detection based on FDM signals.

in the loop" [24] is used to test experimentally the proposed fault tolerant operation. The proposed FDM and FT strategies are implemented in a FPGA chip, as presented in Fig.3. Before FPGA implementation for HIL experiments, the studied system has been modeled and successfully simulated in Matlab/simulink environment, in continuous-time and then discrete-time. Then, the control, FD and FT blocks are translated into a synthesizable VHDL model. Finally, the development board which contains the FPGA can be programmed and used in the HIL simulation. After validation of the fault tolerant method by HIL results, the FPGA can be programmed and the fully experimental tests can be performed. In our case, a Stratix DSP S80 development board is used, which includes the Stratix EP1S80B956C6 FPGA chip. The Fig. 9 shows a synoptic of the HIL.

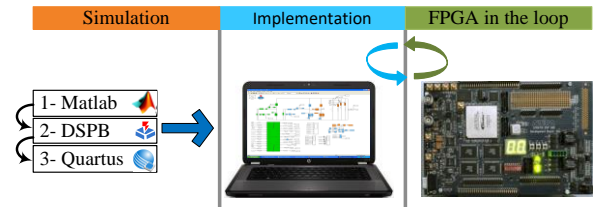


Fig. 9 Hardware-In-the-Loop (HIL) synoptic.

## V. Simulation, HIL and experimental results

### A. Energy management simulation results

In this section, simulation results are provided to verify the validity of the proposed energy management approach. The system is emulated under Matlab-SimPowersSystems environment.

As it mentioned before, the PV source is controlled by a P&O -MPPT algorithm. The obtained results correspond to the BP 3170 photovoltaic module of the BP solar company. To validate the proposed energy management strategy for the studied microgrid, the DC bus voltage reference is fixed to 200V. The implemented profile of the residential load is focused on the summer season presented in the first curve ( $p_{\text{load}}$ ) of Fig. 10. This figure presents the hourly average power consumption by the domestic appliances during 24 hours.

DC bus voltage is presented in the top of Fig. 11. It is the same as reference voltage regardless of the load's variations.

In reality, the daily solar irradiation has the general shape of a curve called "bell", which is modeled here by a Gaussian curve. That is why the PV generated power is null from 17h00 to 6h00 in Fig.10. Excepted this period, the PV provides the possible maximum power and supplies the DC bus, as shown in Fig.11. Corresponding to solar energy variation, the  $P_{\text{max}}$  of PV has been also varied. As Fig. 10 illustrates, the MPPT algorithm increases progressively  $V_{\text{pv}}$  and converges towards the MPP voltage to achieve the power peak.

As it mentioned before, the UC is responsible for the rapid load and PV energy variations. It can be seen in Fig. 10, the UC power compensated perfectly the rapid variation either from the load profile or from the PV. This action of the UC allows to have a constant DC bus voltage.

The battery pack which has a slower dynamic compared to the UC, supplies or absorbs the required energy to smooth the difference between the PV produced power and load demand in longer time, as shown in Fig. 10. From 10h00 to 14h00, the PV production is more than the load demand, thus the battery

absorbs and stocks energy, that is why the  $P_{bat}$  are negative in this time interval (in Fig. 10). The battery also controls the UC voltage around its nominal voltage (see Fig. 11).

### B. Fault Detection Hardware-In-The-Loop Results

For HIL experimentation, the PV Boost converter given in Fig. 1 is considered. Fig. 12 shows detailed HIL results for an open circuit fault detection. At  $t = 240\mu s$  an OCF occurs. At this time, the SM is in state S1 corresponding to Cycle1. When T3 goes to '1' a transition to S2 occurs, as in normal condition. But, because of the OCF, the current ( $i_L$ ) decreases ( $sgn = 0$ ) thus the SM cannot move to S3 and must generate a transition to the state S6. In this state, the output signal OCF goes to '1' and the fault is detected successfully at  $t = 253\mu s$ . The fault detection time is 13s which is less than one switching period (here  $T_{sw} = 67s$ ).

The HIL results for a SCF detection are depicted in Fig. 13. At  $t = 240\mu s$  when the SM is in state S1 a SCF occurs. The transitions from S1 to S5 occur normally. In state S5, because of the SCF, the current  $i_L$  increases and consequently  $sgn$  is equal to '1', thus a transition to S7 occurs. In S7 the output signal SCF goes to '1' and the SCF is detected at  $t = 287\mu s$ . The fault detection time in this case is 47s ( $< 67s$ ). All these results confirm the validity of a very fast fault detection method.

### C. Fault tolerant experimental results

Experimental tests are performed, based on the PV boost converter with a redundant switch, as depicted in Fig. 1. To simulate a switch fault, the  $u_{pv}$  signal is forced to '0' for an OCF and '1' for a SCF. The  $u_R$  is the redundant switch command, which is equal to zero for pre-fault operation and copies  $u_{pv}$  for post-fault operation.

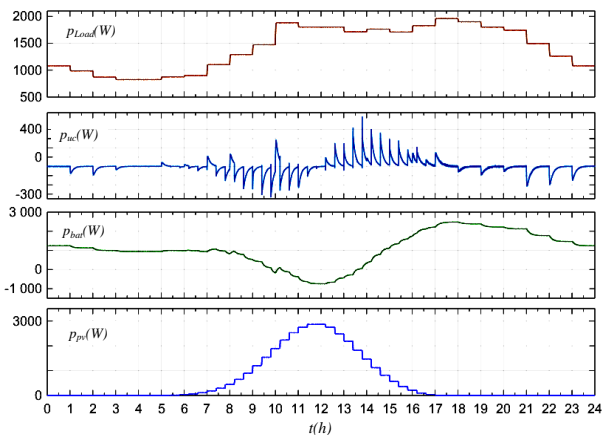


Fig. 10 From up to down: power of Load, DC-bus, UC, Battery pack and PV.

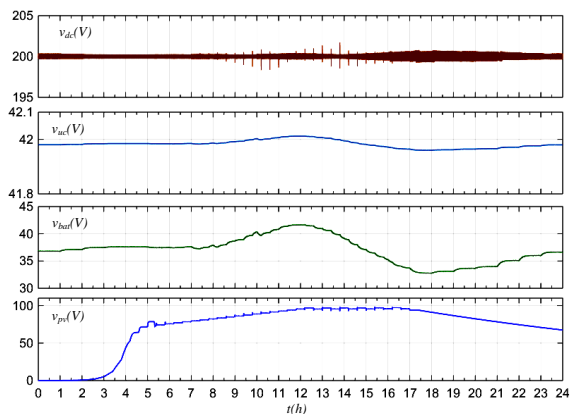


Fig. 11 From up to down: DC-bus, UC, Battery pack and PV voltage.

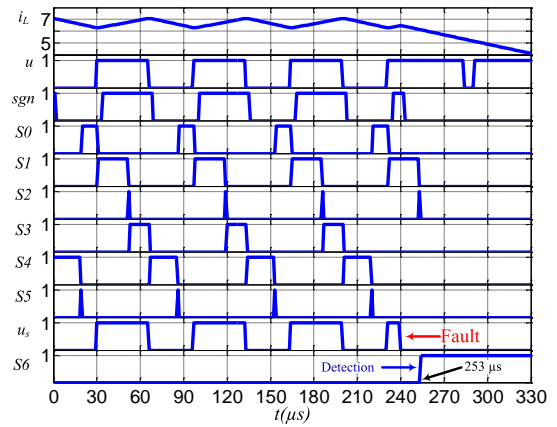


Fig. 12 Detailed HIL results for OCF detection case.

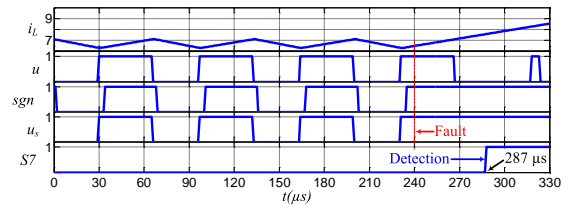


Fig. 13 HIL results for SCF detection.

the validity of the FT operation in case of an OCF is verified in Fig.14. In this case, the OCF is detected after 20  $\mu s$ . According to the proposed reconfiguration strategy, the redundant switch replaces the faulty switch immediately after fault detection and then the system continues to operate in normal conditions.

Fig.15 shows the same results for a SCF. According to these experimental results, the SCF is detected after 42  $\mu s$  but the current continues to increase until the end of the fuse action. As soon as the faulty switch is removed by the fuse (after 500  $\mu s$ ), the current decreases ( $sgn=0$ ), the faulty switch is replaced by the redundant switch and then the system continues to operate normally.

## VI. CONCLUSION

This paper presents the energy management in a stand alone DC microgrid based on a photovoltaic as a main renewable

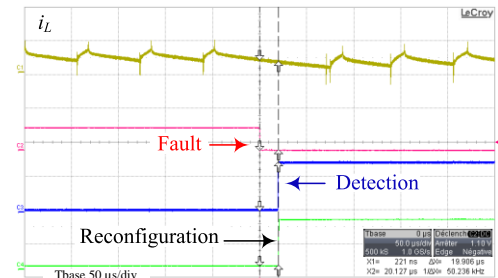
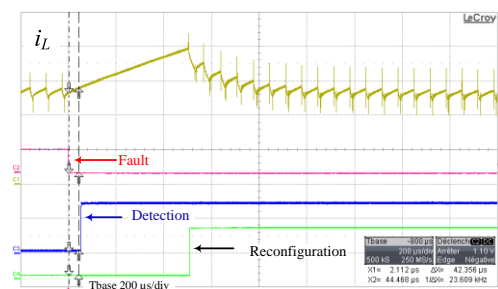


Fig. 14 OCF detection and reconfiguration.



Fi. 15 SCF detection and reconfiguration.

energy source with fault tolerant capability. In order to smooth the load and PV production variations an ultra capacitor and a battery pack are used. The UC, due to its rapid dynamic, is responsible to regulate DC bus voltage during fast power variations. The battery pack compensates the difference between PV production and load demanded power in long term. An energy management based on energy balance on DC bus capacitor is proposed in this paper. Proportional-Integral controllers are used in order to control the system and achieve energy management objectives. To guarantee reliability and service continuity a switch fault diagnosis algorithm is applied on the DC-DC converter of the PV source. Performances of the proposed energy management method are validated by simulations The fast fault tolerant operation is implanted on a FPGA chip and some experimental test are performed to verify the validity of the proposed method.

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