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Abstract: In this paper, we analyze the effect of an enhanced voltage flip technique on the power performance of a piezoelectric energy harvester. The enhanced voltage flip principle is based on a synchronized-switch-based architecture, and is referred to as FAR (Full Active Rectifier). It uses a tiny amount of the stored charge to boost the voltage flip. This work aims to demonstrate that, beside the enhanced flip efficiency, the FAR also contributes to improve the power efficiency of the harvester, especially under changing load constraint. Therefore, the paper proposes a thorough comparison between the FAR and its conventional counterpart, the Switch-only technique. The FAR is easy to implement and does not require any external inductor or capacitor. It only needs a reduced set of switches, an active diode and a simple control sequence, and can thus be implemented on a fully integrated circuit. The FAR can be used as a standalone voltage flip solution or in addition to further boost the flip efficiency in a state-of-the-art architecture such as SSHC for example. Tests were performed on a 0.35-µm process CMOS prototype IC. Experimental results revealed that the FAR extracts 19.1 μW from an off-the-shelf piezoelectric transducer when the output voltage is regulated at 1 V with 1 V open-circuit voltage and delivers up to 20% more power than the conventional Switch-only technique under load constraint. It also shows over 11× power efficiency improvement compared to a conventional diode-based full bridge rectifier.

Keywords: energy harvesting; piezoelectric transducer; active rectifier; integrated circuit

Citation: Frick, V.; Wassouf, L.; Jamshidpour, E. Voltage Flip Efficiency Enhancement for Piezo Energy Harvesting. *Electronics* **2021**, *10*, 2400. https://doi.org/10.3390/electronics10192400

Academic Editor: Fabian Khateb

Received: 1 September 2021
Accepted: 27 September 2021
Published: 1 October 2021
Corrected: 21 April 2022

1. Introduction

With the advent of IoT, the need for portable, and self-powered devices has been dramatically increasing. Batteries are still the most common way of powering embedded applications. Yet, due to their size, weight, impractical replacement, limited lifetime, and above all environmental impact, batteries tend to become unwelcomed in ultra-compact ultra-low power applications.

Harvesting energy from ambient background (solar, eolian, thermal, kinetic, etc.), has been a hot research topic over the last years. The goal is to do without batteries by implementing highly efficient dynamic power generators. In particular, the literature reports many implementations of kinetic harvesters involving piezoelectric devices Çiftci et al. [1], Chen et al. [2], Du and Seshia [3], Sanchez et al. [4], inductive devices Rahimi et al. [5], and electrostatic (capacitive) devices Tao et al. [6], Stanzione et al. [7].

Piezoelectric energy harvesters (PEH) are among the most investigated and popular kinetic energy harvesting systems, first because of the wide availability of ambient vibration sources, and second because they can achieve relatively high power density, i.e., from tens to several hundreds of microwatts per cubic centimeter, compared to the capacitive or inductive conversion principles. Moreover, they are easy to combine with conventional integrated circuit technologies Stanzione et al. [7]. Figure 1 shows the basic topology of a PEH system. It breaks down into three core parts: (1) A piezoelectric transducer (PT). (2) An interface and control circuit (IC). (3) Storage and load elements.

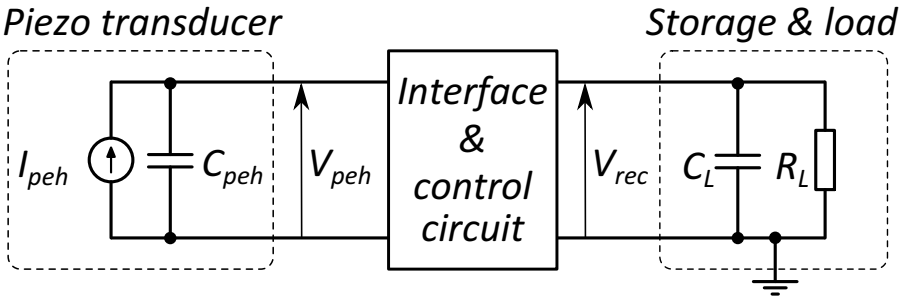


Figure 1. Piezoelectric harvesting system.

Thanks to the piezoelectric properties of its material, the PT turns the mechanical energy into electrical energy. The equivalent electrical model of the PT consists in the parallel combination of an AC current source, which provides the current I_{peh} proportional to mechanical excitation, with an inherent piezoelectric capacitor C_{peh}. The storage element can be a supercapacitor C_L, and the load is usually modelled as a resistor R_L. Note that R_L may change dynamically according to the power requirements of loads such as sensors or wireless modules for instance. The main role of the interface circuit is to rectify the AC voltage of the PT, V_{peh}, and provide the system with stable voltage supply. Ideally, the voltage supply should be independent of the load but in practice, a change in the value of R_L can strongly affect the power efficiency of the harvester.

The most common interface circuit for rectifying V_{peh} is a Full-Bridge Rectifier (FBR). Yet, the voltage drop across the rectifying diodes makes the FBR unsuitable for low-voltage PT (i.e., V_{peh} in the 1 V range or below). In order to circumvent the diodes' threshold issue, Herbawi et al. [8] proposed the principle of active rectification that uses a negative voltage converter (NVC) combined to a series-connected active diode (AD) instead of the FBR Peters et al. [9]. The NVC acts like an FBR but uses transistors instead of diodes, thus yielding lower voltage drop across the rectifier. The AD prevents C_L-to-PT current backflow.

Furthermore, the combination of the inherent capacitor C_{peh} in parallel with I_{peh} causes I_{peh} and V_{peh} to be normally in phase quadrature. This contributes to further dramatically hamper FBR efficiency because C_{peh} needs to discharge and recharge at each zero-crossing moment of I_{peh}. Numerous interface topologies and architectures have been proposed to improve power efficiency by applying nonlinear synchronous switching Richard et al. [10]. All these architectures use external devices, i.e.inductor and/or capacitor, to handle the charge of C_{peh}. Synchronous Electric Charge Extraction (SECE) consists in extracting the energy accumulated in C_{peh} by transferring it into an inductor, which in turn transfers it into the storage device Hehn et al. [11], Dini et al. [12], Shi et al. [13], Morel et al. [14,15]. SECE alleviates the load dependency of the system but requires a bulky inductor and tends to have degraded performance for periodic excitation of PT. Synchronized Switch Harvesting architectures reuse the own charge of C_{peh} to invert the polarity of V_{peh} upon I_{peh} zero-crossing. They employ either an inductor (SSHI) (Sanchez et al. [4], Du et al. [16], Ramadass and Chandrakasan [17], Wu et al. [18], Chamanian et al. [19,20]) or a set of capacitors (SSHC) (Chen et al. [2], Du and Seshia [3], Chen et al. [21], Hong et al. [22]) to store the charge of C_{peh} temporarily before sending it back once the electrodes of the PT have been swapped. Architectures combining both an inductor and a capacitor have also been reported in Çiftci et al. [23] and Çiftci et al. [1]. Synchronized-switch-based architectures globally achieve better power efficiency than SECE for both shock and periodic excitation. According to Ramadass and Chandrakasan [17], full voltage flip of V_{peh} could theoretically allow very high (i.e., infinite) efficiency. Yet, in practice the characteristics of the components strongly limit the voltage flip efficiency, and I_{peh} still needs to provide C_{peh} with complementary charge prior to transferring energy from the PT to C_L and R_L. Moreover, SSHC and SSHI architectures have load-dependent performance, which means that the power efficiency strongly depends on changes in R_L and/or the excitation's amplitude. Çiftci et al. [1]

proposed a circuit that reduces the load-dependency of the power efficiency. But such systems require more complex control.

Therefore, there is a genuine interest in proposing an easy-to-implement synchronized switch architecture that both achieves high-efficiency voltage flip and is able to maintain fair power efficiency during transient changes of the load R_L. Enhancing the voltage flip minimizes the charge needed by C_{peh} and thus allows to extract energy from the PT shortly after the voltage flip. This point is particularly critical in low-voltage systems, i.e., $V_{peh} \leq 1$ V, that harvest power in the tens of microwatts range.

In this paper, we demonstrate the benefit of a synchronized-switch-based architecture, referred to as full active rectifier (FAR) and first proposed in Wassouf et al. [24], to alleviate the load influence of the piezoelectric energy harvester. The FAR is based on the SSHC concept that consists in flipping V_{peh} by means of a capacitor, but has much simpler control and needs no additional capacitors. In terms of power performance, the FAR is similar to the Switch-only principle Ramadass [25], and thus performs worse than state-of-the-art SSHI or SSHC. But it is important to note that, discussing raw absolute performance is not the point of this paper. The key result we propose here is the theoretical and experimental proof that thanks to the voltage flip enhancement, the FAR achieves better power efficiency under load constraint than Switch-only. It is yet also important to note that the proposed technique may be applied in addition to state-of-the-art voltage flip architectures that reuse the charge of C_{peh} (i.e., SSHI and SSHC), and hence contribute to enhance their performance.

The paper is organized as follows: Section 2 presents the enhanced voltage flip concept, the FAR IC topology, its operation principle, and provides a thorough analysis of charge loss and power performance compared to Switch-only. Section 3 provides experimental results. Finally, Section 4 concludes this paper.

2. Enhanced Voltage Flip

The voltage flip enhancement technique that we propose consists in recharging C_{peh} with C_L. At first glance, the concept of reusing the stored charge may appear as counter intuitive but in this section, we demonstrate that it contributes to enhance the power efficiency of the harvester. At each zero-crossing instant of I_{peh}, the piezo capacitor C_{peh} is first shorted, and then immediately recharged with a fraction of the charge from the storage capacitor C_L Wassouf et al. [24]. In the following sections, the proposed concept will be referred to as the FAR.

The concept is based on the use of a large storage capacitance C_L, which should be at least one order of magnitude greater than C_{peh}. This can easily be admitted because storage capacitances have usually large values. As discussed in Section 2.3, the concept also imperatively needs the rectified voltage V_{rec} to be regulated, in order to ensure optimal power extraction of the proposed harvester.

For comparison purpose, because the FAR and the conventional Switch-only principle have a priori the same energy balance, we designed the FAR integrated circuit architecture presented below. This circuit allows to implement both FAR and Switch-only modes.

2.1. FAR IC Topology

Figure 2 presents the topology of the FAR IC. A set of switches (SW_0 to SW_3) consisting of transmission gates (TG) is connected to an active diode (AD) to form the rectifying part of the system. The logic control block (CB) of Figure 3 performs the switching sequence described below. The circuit also features a voltage regulator (VR) Du and Seshia [3], a ring oscillator (RO) Ferreira and Galup-Montoro [26], and switch drivers (SD). The later include a charge pump Tsuji et al. [27] and level shifters Du and Seshia [3], Matsuzuka et al. [28] that are needed to control the switches properly. Note that blocks VR, RO and SD are standard functions, which are largely documented in the state-of-the-art literature. Therefore, they are not further detailed in this paper.

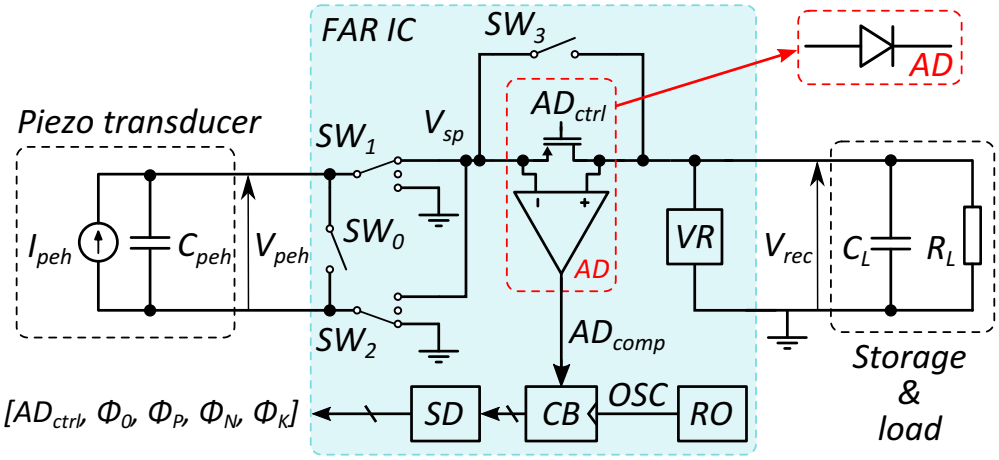


Figure 2. Full Active Rectifier (FAR) IC architecture Wassouf et al. [24].

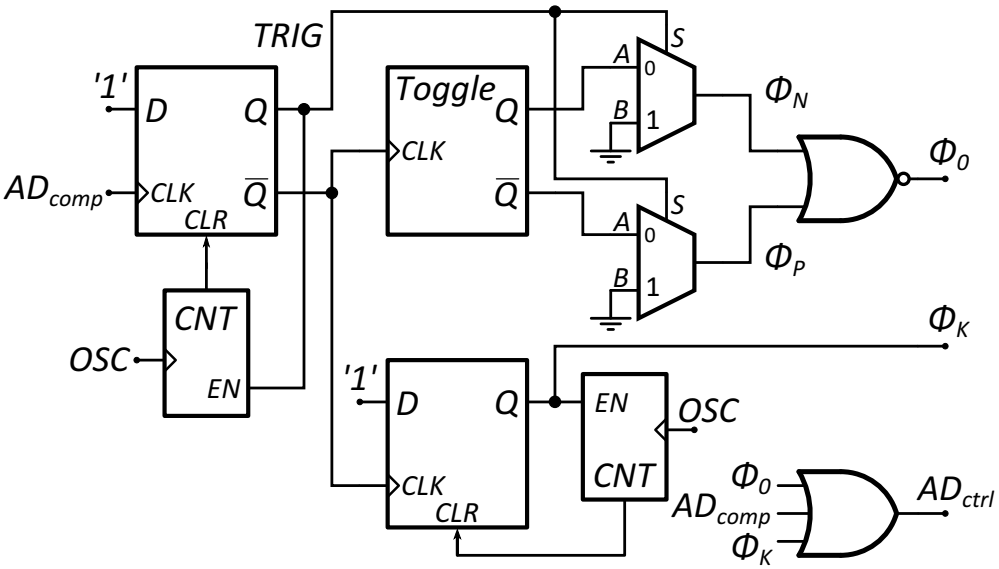


Figure 3. Architecture of the control block.

The AD is used for both preventing the current from flowing back from C_L and detecting the zero-crossing moment of I_{peh}. It comprises a PMOS switch and an ultra-low power comparator proposed in Du and Seshia [3]. When the voltage at node V_{sp} drops below the rectified output voltage V_{rec} (Figure 2), the PMOS switch of AD is turned off, and the voltage flip operation is triggered as explained below.

2.2. FAR Operation Principle

The zero-crossing of I_{peh} causes the AD's comparator output signal AD_{comp} to go high. AD_{comp} triggers the signal sequence generated by CB. The CB signals control in turn the AD and the switches SW_0 to SW_3.

Figure 3 shows the architecture of CB. Signal AD_{ctrl} controls the PMOS switch of AD, signal Φ_0 controls SW_0, signals Φ_P and Φ_N both control switches SW_1 and SW_2, and signal Φ_K controls SW_3. Figure 4 shows the sequence and its effect on the PEH's voltages, while Table 1 shows the operating scheme of the switches according to the control signals. It is worth noticing that the voltage flip operation is triggered by signal AD_{ctrl} and thus the control block auto-adapts according to the zero-crossing moment of I_{peh} regardless of the PT's excitation frequency f_{ex}.

The operation of the FAR breaks down into 3 phases.

2.2.1. Shorting Phase

Signal AD_{comp} acts as the clock signal of a D flip-flop whose data input is set to a constant logic "high" state (Figure 3). When AD_{comp} goes high, a trigger signal $TRIG$ turns on signals Φ_P and Φ_N simultaneously, which puts switches SW_1 and SW_2 in high impedance, i.e., off (Table 1). In the meantime, signal Φ_0 turns on SW_0 (Figure 4), which shorts C_{peh}. Signal $TRIG$ remains high until C_{peh} is discharged. The duration of the shorting phase τ_{Φ_0} depends on the value of C_{peh} and the resistance of SW_0. The TGs used to implement the switches have very low ON-resistance, typically around 15 Ω. Assuming $C_{peh} = 100$ nF, based on the off-the-shelf transducer characteristics (S118-J12S-1808YB, Piezo.com, accessed on 1 September 2021) used in the experiments (Section 3), the corresponding RC time constant is thus 1.5 µs. The duration τ_{Φ_0} is controlled by means of a counter (CNT in Figure 3) clocked by the RO signal OSC. This signal is initially used to clock the charge pump used in the switch drivers, and has a frequency of 125 kHz. Therefore, OSC allows controlling τ_{Φ_0} with 8 µs accuracy. In the proposed system, we used a modulo 4 counter, which thus yields $\tau_{\Phi_0} = 32$ µs. This duration is largely sufficient to ensure complete discharging of C_{peh}.

2.2.2. Sharing Phase

Once $TRIG$ is reset, i.e., $\overline{TRIG}$ goes high, a toggle sets either Φ_P or Φ_N to high depending on whether I_{peh} is positive or negative, respectively. When Φ_P is high, SW_1 is connected to node V_{sp} and SW_2 is connected to ground, and inversely when Φ_N is high (Table 1). In the meantime, Φ_K goes high, which closes SW_3 and causes C_L to share its charge with C_{peh}. During this sharing phase, SW_3 is in series with either SW_1 or SW_2. Since all switches are implemented with the same TGs, the RC time constant is thus 3 µs. Therefore, we also used a modulo 4 counter (Figure 3) to set the duration of the sharing phase $\tau_{\Phi_K} = 32$ µs, which is also sufficient to complete the charge transfer.

Table 1. Switches states according to control signals.

Signal \ Switch	SW_0	SW_1	SW_2	SW_3
Φ_0	ON	OFF	OFF	OFF
Φ_K	OFF	$\begin{matrix} V_{SP}\ (I_{peh} > 0) \\ gnd\ ^{(a)}\ (I_{peh} < 0) \end{matrix}$	$\begin{matrix} gnd\ ^{(a)}\ (I_{peh} > 0) \\ V_{SP}\ (I_{peh} < 0) \end{matrix}$	ON
Φ_P	OFF	V_{SP}	gnd [(a)]	OFF
Φ_N	OFF	gnd [(a)]	V_{SP}	OFF

[(a)] gnd = ground.

At the end of the sharing phase, the value of V_{peh} across C_{peh} is V_{built}:

$$V_{built} = \frac{\left(Q_L + Q_{peh}\right)}{\left(C_L + C_{peh}\right)} \tag{1}$$

V_{built} only depends on the charge Q_L stored in C_L, the charge of C_{peh} being $Q_{peh} = 0$ after the shorting phase. If $C_L \gg C_{peh}$, then $|V_{built}| = V_{rec} \simeq V_{recmax}$, which is the value of V_{rec} right before the voltage flip operation is triggered (see Figure 4). Note that, V_{built} continuously increases as C_L charges.

2.2.3. Power Extraction Phase

Once C_{peh} is recharged, SW_3 turns off while either SW_1 or SW_2 remains on, depending on whether I_{peh} is negative (Φ_N high) or positive (Φ_P high), respectively (Figure 4). Since the terminals of the PT are swapped by SW_1 and SW_2 at each phase inversion of I_{peh}, this

procudes the rectifying of V_{peh} (i.e., $V_{sp} = \left|V_{peh}\right|$). In this phase, the AD's PMOS switch turns on as soon as $\left|V_{peh}\right| > V_{rec}$, which in turn connects the PT to C_L. As a result, most of the charges transfer directly from PT to C_L and R_L.

Note that the PMOS switch turns on very shortly after the sharing phase, since the voltage at node V_{sp} is $\left|V_{peh}\right| = |V_{built}| = V_{rec}$ as mentioned in Section 2.2.2. This has significant consequence on the power efficiency as discussed in Section 2.3.

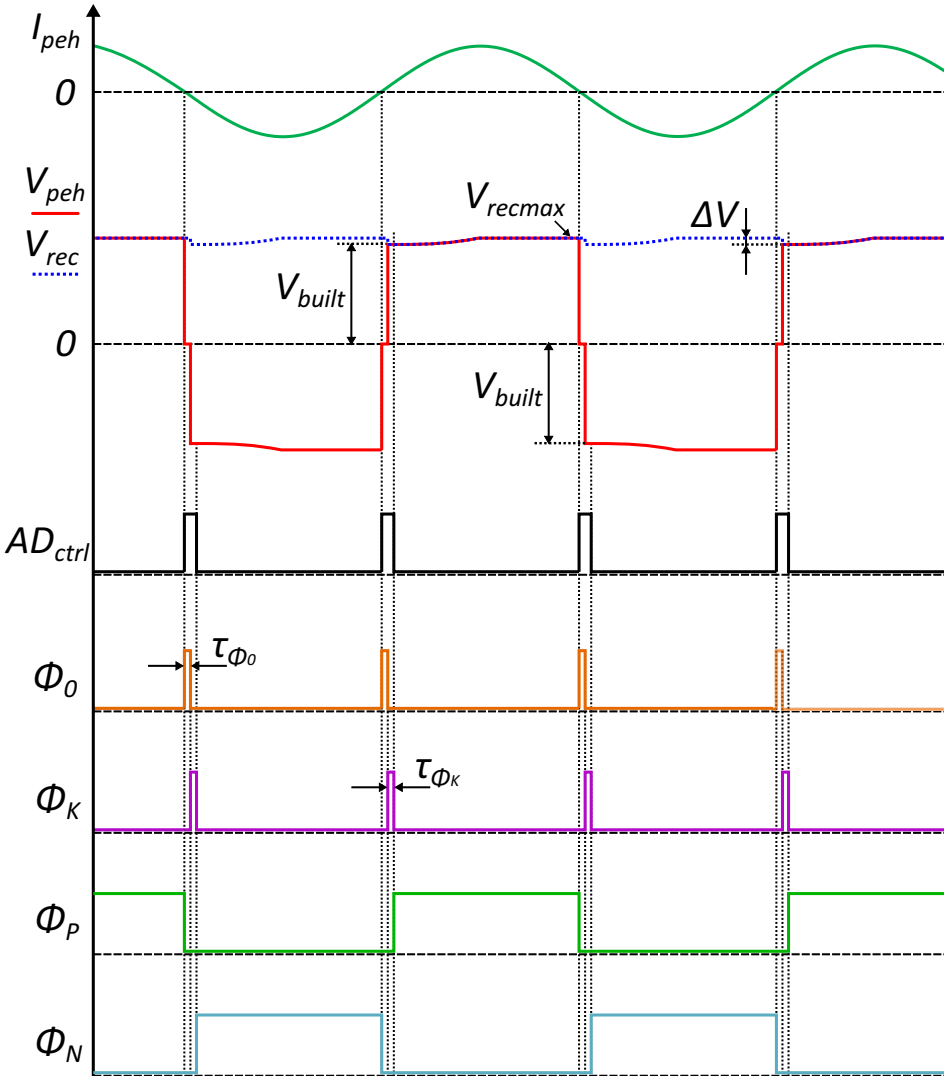


Figure 4. Voltage and current waveforms of PEH, and control signals.

2.3. Power Performance Analysis

If we suppose that I_{peh} is a sine current source such as

$$I_{peh}(t) = \hat{I}_{peh} \cdot \sin(2\pi f_{ex} t) \tag{2}$$

where $\hat{I}_{peh}$ represents the amplitude and f_{ex} is the vibration frequency, then the expression of the open-circuit voltage V_{OC} across the PT is given by:

$$V_{OC}(t) = \hat{V}_{OC} \cdot \sin\left(2\pi f_{ex} t + \frac{\pi}{4}\right) = \frac{1}{C_{peh}} \int I_{peh}(t) dt \tag{3}$$

with $\hat{V}_{OC}$ the open-circuit amplitude. When $V_{OC}(t)$ shifts from $-\hat{V}_{OC}$ to $+\hat{V}_{OC}$, the total amount of charge generated by the PT in half a period is thus (Du and Seshia [3], Ramadass [25]):

$$Q_{peh} = 2C_{peh}\hat{V}_{OC} = \int_0^{1/(2f_{ex})} I_{peh}(t)dt = \frac{2\hat{I}_{peh}}{\omega} \tag{4}$$

where $\omega = 2\pi f_{ex}$.

2.3.1. With Infinite R_L

The total charge loss Q_{loss} breaks down into two main contributions: Q_1, lost by C_L during the recharging of C_{peh} (sharing phase) and Q_2, the charge that goes to C_{peh} during the power extraction phase, i.e., when C_{peh} is in parallel with C_L.

In steady state, when V_{rec} reaches its maximum value V_{recmax} (Figure 4) imposed by VR, the expressions for Q_1 and Q_2 are

$$Q_1 = V_{built}C_{peh} = \Delta V \cdot C_L \tag{5}$$

$$Q_2 = (V_{recmax} - V_{built}) \cdot C_{peh} = \Delta V \cdot C_{peh} \tag{6}$$

where ΔV represents the ripple of V_{rec} caused by the recharging of C_{peh}. The total charge loss is then

$$Q_{loss} = C_{peh} \cdot (\Delta V + V_{built}) = C_{peh} \cdot V_{rec} \tag{7}$$

From (1) and (5), we may consider $\Delta V \approx 0$ provided that $C_L \gg C_{peh}$. Therefore, we can consider that C_L fully recharges C_{peh}, making $Q_1 = V_{built} \cdot C_{peh}$ the principal charge loss (i.e., $Q_1 \approx Q_{loss}$). We can thus express the total charge stored on C_L in half a period as

$$Q_L = Q_{peh} - Q_{loss} = C_{peh} \cdot \left(2\hat{V}_{OC} - V_{rec}\right) \tag{8}$$

and then the total charge on a full period is then $2Q_L$.

Thus, the output power is given by

$$P_{rec} = 2V_{rec}f_{ex}Q_L = 2V_{rec}f_{ex}C_{peh} \cdot \left(2\hat{V}_{OC} - V_{rec}\right) \tag{9}$$

From (9), we can deduce that the maximum power extraction is achieved when $V_{rec} = \hat{V}_{OC}$, which corresponds to a maximum power

$$P_{recmax} = 2C_{peh}\hat{V}_{OC}^2 f_{ex} \tag{10}$$

This result shows that the power efficiency is inherently load-dependent because applying a finite value load R_L affects V_{rec}, as it would for any synchronized switch harvesting system (Çiftci et al. [1], Chen et al. [21], Du et al. [29]) and suggests VR should regulate V_{rec} to $\hat{V}_{OC}$ (Ramadass and Chandrakasan [17]). Moreover, it is identical to Switch-only, the architecture and signals of which are presented in Figure 5.

When R_L is infinite and V_{rec} is regulated to $\hat{V}_{OC}$, the amount of charge needed to recharge either C_L (FAR) or C_{peh} (Switch-only) is $Q_{peh}/2$. Yet, energy harvesting systems are meant to supply a finite value load with charges delivered by C_L and PT. As demonstrated in the next section and in Section 3.2, the proposed FAR architecture has an impact on the power performance when R_L has finite value. Furthermore, since FAR and Switch-only have the same power performance a priori, we compared both architectures.

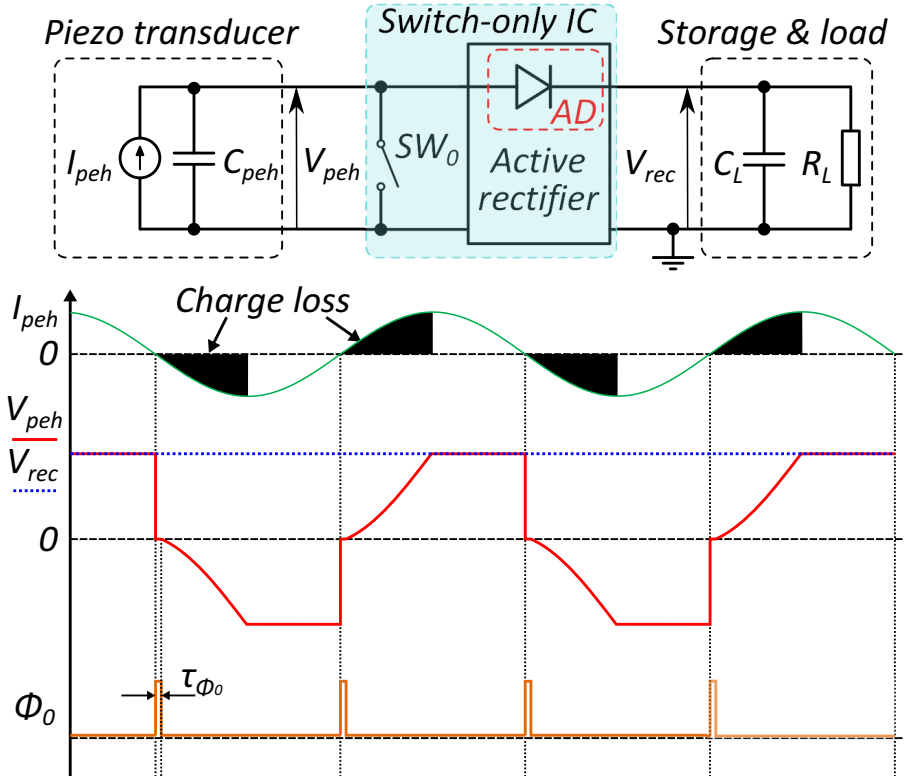


Figure 5. Switch-only architecture and related signal when V_{rec} is regulated to $\hat{V}_{OC}$.

2.3.2. With Finite R_L

Figure 6 shows the equivalent electrical model of the PEH during the power extraction phase (i.e., AD is "ON"), when R_L has a finite value. Note that this model assumes the series resistances of the switches and ADs are negligible, which is realistic considering R_L is around several tens of kilo-ohms as discussed below. The expression of V_{rec} is given by:

$$V_{rec}(t) = Ke^{-\frac{t}{\tau}} + \frac{R_L \hat{I}_{peh}}{1+(\tau\omega)^2}\sin(\omega t) - \frac{R_L \tau\omega \hat{I}_{peh}}{1+(\tau\omega)^2}\cos(\omega t) \tag{11}$$

where $\tau = R_L C_{//}$ and K is the initial condition constant such as $V_{rec}(0) = V_{built}$, considering $t = 0$ s corresponds to the zero-crossing moment of I_{peh}. Equation (11) applies for V_{rec} lower than $\hat{V}_{OC}$. When V_{rec} reaches $\hat{V}_{OC}$, it is regulated to this value by VR. Figure 7a shows $V_{rec}(t)$ for the FAR architecture ($V_{rec|_{FAR}}$) simulated on half a period of I_{peh} when applying a finite load R_L at $t = 0$ s. The parameters of PT are: $C_{peh} = 100$ nF and $I_{peh} = 20\pi e^{-6}$ A, and the excitation frequency is $f_{ex} = 100$ Hz. This corresponds to $\hat{V}_{OC} = 1$ V. The load is $R_L = 48$ kΩ, and K is set so that $V_{rec}(0) = K - {}^{R_L\tau\omega\hat{I}_{peh}}/_{(1+(\tau\omega)^2)} = {}^{\hat{V}_{OC}\cdot C_L}/_{(C_{peh}+C_L)}$, which is the value of V_{built} when $V_{rec} = \hat{V}_{OC}$ at the zero-crossing moment of I_{peh} (See Section 2.2.2).

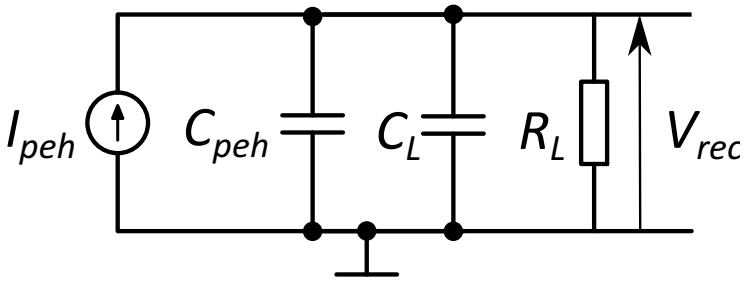


Figure 6. Equivalent of PEH during power extraction phase.

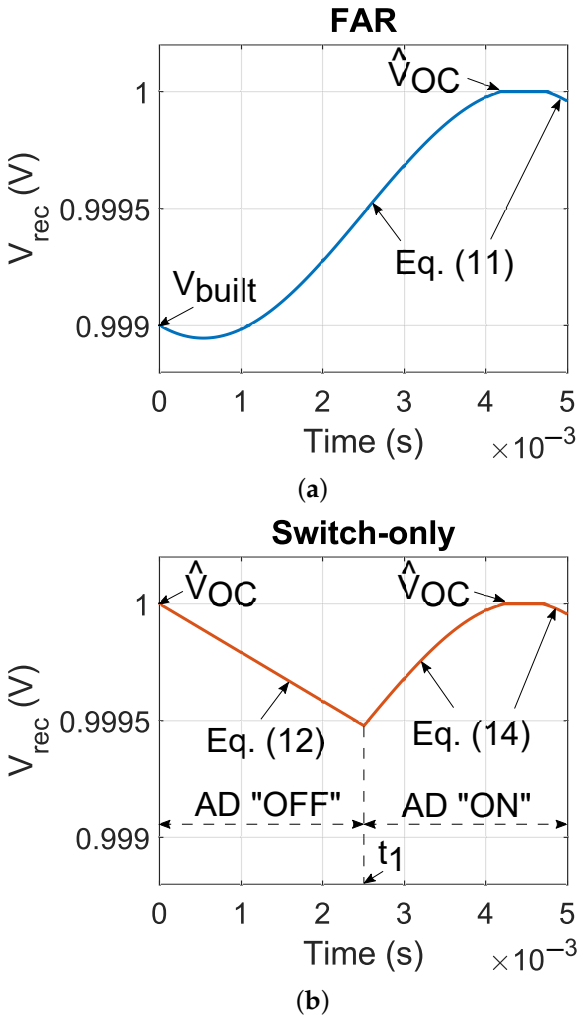


Figure 7. Simulated transient evolution of $V_{rec}(t)$ on half a period if I_{peh} (**a**) FAR, (**b**) Switch-only. The parameters are $C_{peh} = 100\,\text{nF}$; $C_L = 100\,\mu\text{F}$; $R_L = 48\,\text{k}\Omega$; $\omega = 200\pi\,\text{rad/s}$; and $I_{peh} = 20\pi e^{-6}\,\text{A}$.

In the Switch-only architecture, the evolution of V_{rec} breaks down into two phases. First, its AD is "OFF" and C_{peh} recharges, while in the meantime, C_L discharges into R_L. Therefore, in this phase, V_{rec} and V_{peh} evolve separately. On the one hand, the expression of V_{rec} is

$$V_{rec}(t) = K_{SO} e^{-\frac{t}{R_L C_L}} \tag{12}$$

where K_{SO} is the initial value of V_{rec} at the zero-crossing moment of I_{peh}. On the other hand, the expression of V_{peh} is

$$V_{peh}(t) = \hat{V}_{OC} - \hat{V}_{OC} \cdot \cos(\omega t) \tag{13}$$

The second phase of V_{rec} for the Switch-only starts when AD is "ON" (i.e., $\left|V_{peh}\right| = V_{rec}$). In this phase, the equivalent schematic of the Switch-only architecture is exactly the same as for the FAR (cf. Figure 6). Therefore, the expression of V_{rec} is deduced from (11) but with an offset V_{off}:

$$V_{rec}(t) = Ke^{-\frac{t}{\tau}} + \frac{R_L \hat{I}_{peh}}{1+(\tau\omega)^2}\sin(\omega t) - \frac{R_L \tau\omega \hat{I}_{peh}}{1+(\tau\omega)^2}\cos(\omega t) + V_{off} \tag{14}$$

This offset V_{off} is induced by the decay of V_{rec} during the first phase of Switch-only. Furthermore, just as for the FAR architecture, when V_{rec} reaches $\hat{V}_{OC}$, it is regulated by VR. Figure 7b shows V_{rec} for the Switch-only architecture ($V_{rec|_{SO}}$) simulated with the same parameters as for the FAR simulation presented in Figure 7a. Note that, for Switch-only $V_{rec}(0) = K_{SO} = \hat{V}_{OC} = 1\,\text{V}$.

To establish whether V_{off} is positive or negative, i.e., which one yields the greater value (11 or 14, FAR or Switch-only), we first needed to find the moment t_1 when V_{rec} of Switch-only caught up with V_{peh}, which corresponds to the moment when AD turns "ON":

$$K_{SO} e^{-\frac{t_1}{R_L C_L}} = \hat{V}_{OC} - \hat{V}_{OC} \cdot \cos(\omega t_1) \tag{15}$$

Note: there is no analytic expression to solve (15). Therefore, to evaluate t_1 we need to apply a numerical method, such as Newton–Raphson (Conejo and Baringo [30]). The value t_1 is then injected into (14) to determine V_{off} so that Equations (12)–(14) yield the same value. Numerical simulations (Figure 8) reveal that, whatever the values of the parameters in (11) and (14), $V_{off} < 0$, which means that for $t \geq t_1$, $V_{rec|_{FAR}} > V_{rec|_{SO}}$.

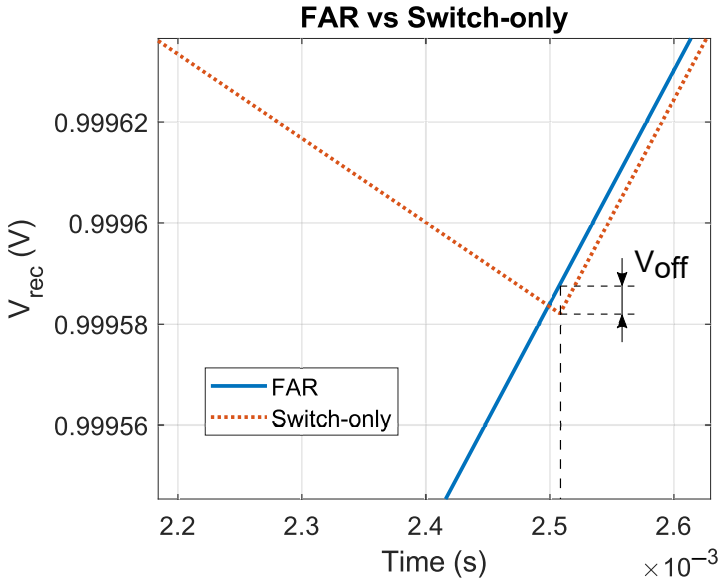


Figure 8. Detail plot around $t = t_1$ of Figure 7a,b superimposed.

This result has significant consequences for the power efficiency of the systems as R_L evolves. More specifically, from (11) we found the limit value $R_{L_{\text{lim}}}$ of R_L for which $V_{rec|_{FAR}}$ reached $\hat{V}_{OC}$ at $t = T/2$. Applying $R_{L_{lim}}$ in (14) yielded $V_{rec|_{SO}}(T/2) < \hat{V}_{OC}$. Since the value of $V_{rec}(T/2)$ set the initial conditions of V_{rec} for the next half period of I_{peh}, we verified that for $R_L = R_{L_{\text{lim}}}$, the average value of $V_{rec|_{SO}}$ decreased to compensate for the presence of R_L while the average value of $V_{rec|_{FAR}}$ remained constant. More generally, when $R_L < R_{L_{\text{lim}}}$, V_{rec} decreased in both architectures, $V_{rec|_{SO}}$ decreased faster and, more importantly, stabilized to a lower value than $V_{rec|_{FAR}}$. Note that, for either architecture, V_{rec} adjusted to a steady-state average value that depended on the amount of energy the harvester transfered from the PT to R_L. This amount was lower in Switch-only because the power extraction phase was shorter than in FAR. Furthermore, the value of C_L only affected the evolution speed of V_{rec} when R_L changed. The faster decreasing speed of $V_{rec|_{SO}}$ cames from the smaller time constant $R_L C_L$ when the ADwas "OFF" (see 12). The same reason explains why $V_{rec|_{SO}}$ stabilized at a lower value than $V_{rec|_{FAR}}$. Figure 9 shows the numerical simulations of both architectures with $R_L = 48\ \text{k}\Omega$ and the same initial conditions as above. We noticed that $V_{rec|_{SO}}$stabilized around 3 mV below $V_{rec|_{FAR}}$.

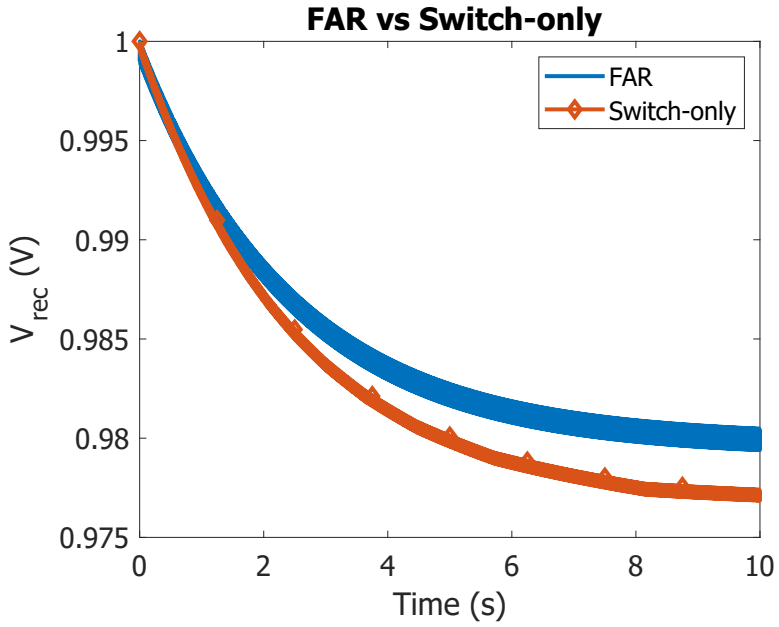


Figure 9. Simulated transient evolution of V_{rec} in FAR and Switch-only when $R_L = 48\,\text{k}\Omega$, with 1 V initial condition.

For power, FAR was also more efficient than Switch-only once V_{rec} had been stabilized. Figure 10 shows the average power difference $\Delta P = P_{FAR} - P_{SO}$ between FAR and Switch-only. It is worth noticing that at $t = 0\,\text{s}$, i.e., before and shortly after applying R_L, Switch-only achieved slightly better power performance than FAR ($\Delta P < 0$). This was due to the fact that without R_L, the FAR principle yielded lower average values of V_{rec}. However, energy harvesting systems are not just meant to charge a storage device; they are intrinsically designed to supply energy to a load. Therefore, as shown here in the FAR implementation, there was a benefit in using voltage flip enhancement to improve power performance.

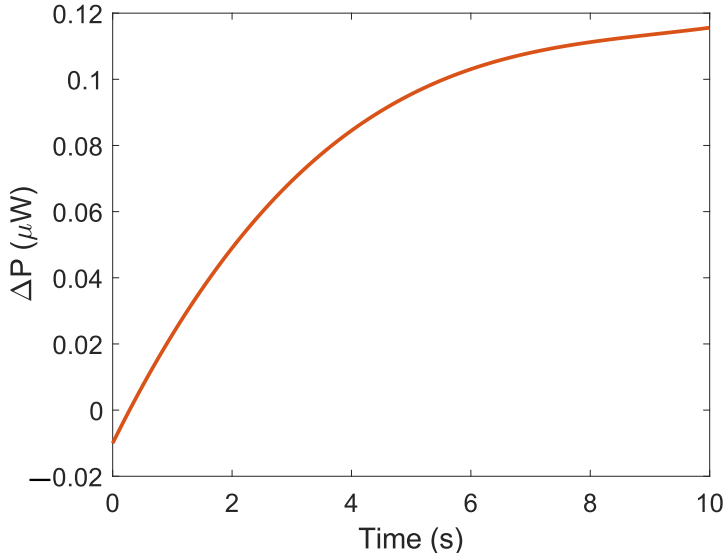


Figure 10. Simulated transient evolution of average power difference ΔP between FAR and Switch-only for $R_L = 48\,\text{k}\Omega$.

Furthermore, we believe that combining the voltage flip enhancement principle to SSHI or SSHC might contribute to further improve the power performance under load

constraint. But for the time being, this statement is based on theoretical assumptions and needs to be further investigated.

3. Experimental Results and Discussion

3.1. Prototype Design and Experimental Setup

We designed and tested a fully integrated prototype fabricated using AMS 0.35 µm High-Voltage CMOS technology. The circuit features all the blocks of the FAR architecture presented in Figure 2. The voltage supply was 3.3 V for AD, SD and VR and 1.2 V for CB and RO (Figure 2). Note that CB can be configured either in FAR or in Switch-only mode to allow performance comparison between both architectures.

To validate the voltage flip efficiency, we performed post-layout transistor-level 1 s transient simulations with $C_L = 10\,\mu F$ and no load resistance R_L. The model of the PT was based on the off-the-shelf device S118-J12S-1808YB by Piezo.com (accessed on 1 September 2021) with $C_{peh} = 100\,nF$. We set $\hat{I}_{peh}$ and f_{ex} to achieve an open-circuit amplitude $\hat{V}_{OC} = 1\,V$. According to (3), this corresponds to $\hat{I}_{peh} = 20\pi e^{-6}\,A \simeq 62.8\,\mu A$ and $f_{ex} = 100\,Hz$. Since there was no R_L, we set VR to regulate V_{rec} to $\hat{V}_{OC}$, which corresponded to the theoretical maximum power efficiency, $P_{recmax} = 20\,\mu W$ according to (10).

Figure 11 shows the simulation results performed with Cadence®. Note that C_L was pre-charged with $V_{rec} = 0.7\,V$ by a cold start circuit, not detailed here. Once $V_{rec} \geq 0.7\,V$, the control block CB was activated and the the FAR system started to operate. The middle plot in Figure 11 shows that when V_{rec} was regulated to $\hat{V}_{OC}$, V_{built} was around 0.99 V ($\Delta V \simeq 10\,mV$, see inset zoom view), which corresponded to 99% voltage flip efficiency. It also revealed the effect of the "ON" resistance of the non-ideal AD PMOS switch, which caused $\left|V_{peh}\right| = V_{sp}$ to exceed V_{rec}. The bottom plot focusedon a voltage flip sequence following a zero-crossing of I_{peh}. The voltage flip duration was 64 µs. One noticed that the AD output signal AD_{comp} returned to a low level almost instantly after the voltage flip operation started. This was due to a temporary increase in voltage at node V_{sp} (Figure 2) caused by charge injection when switches SW_1 and SW_2 opened. Therefore, to prevent spurious behavior of the FAR, the signal AD_{ctrl} was locked by the combinatorial OR function of AD_{comp}, Φ_0 and Φ_K. Signal AD_{comp} went high again as C_{peh} recharged during the sharing phase, and eventually returned to low leveld shortly after this phase was complete, as $\left|V_{peh}\right| = V_{sp}$ increased and power extraction started.

Figure 12 shows a micrograph of the ASIC and the test bench. For mechanical excitation, we used an LDS® V400 series shaker by Brüel & Kjær, driven by an AC power source 6813B by Agilent®. The excitation signal was a 100 Hz sine waveform and the acceleration was set to get $\hat{V}_{OC} = 1\,V$. For these experiments, the extracted energy was stored on a conventional capacitor $C_L = 100\,\mu F$. A LabVIEW® platform performs shaker control and raw signal acquisition via a Tektronix® TDS series digital oscilloscope.

3.2. Experimental Results

Figure 13 shows the measured waveforms of V_{peh} and V_{rec} corresponding to the above mentioned parameters and operating conditions of the FAR architecture. After the voltage flip operation, the voltage across C_{peh} was $V_{built} = 0.864\,V$. This corresponded to 86.4% voltage flip efficiency, which was lower than the Cadence simulated value. There were two reasons for this. First, when operating the PT close to its mechanical resonance frequency (130 Hz), the strong coupling effect induced harmonic oscillations that prevented complete voltage flip, as can be seen in Figure 13a. Second, the series resistance of the T-gate switches combined with the various interconnections between the test board and the PT induced a larger time constant. As can be seen on Figure 13b, this effect was greater during the sharing phase when the charge from C_L transited through SW_3 and $SW_{2/3}$, and the series resistance was thus larger than during the shorting phase. One solution to circumvent this issue was to extend the duration of the sharing phase, but this had only limited benefit because the

deleterious effect of harmonic oscillations prevailed. We experimentally determined that a 32 µs sharing phase duration yielded optimal voltage flip efficiency.

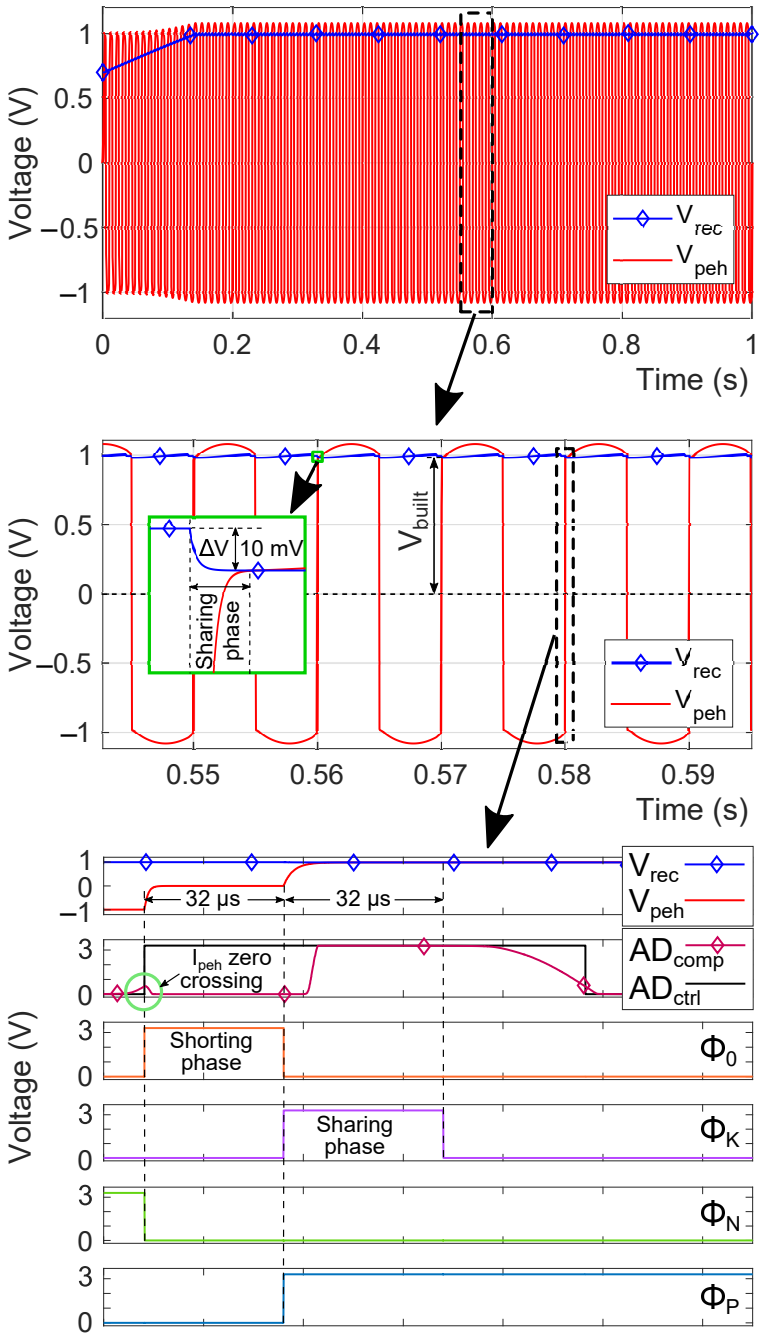
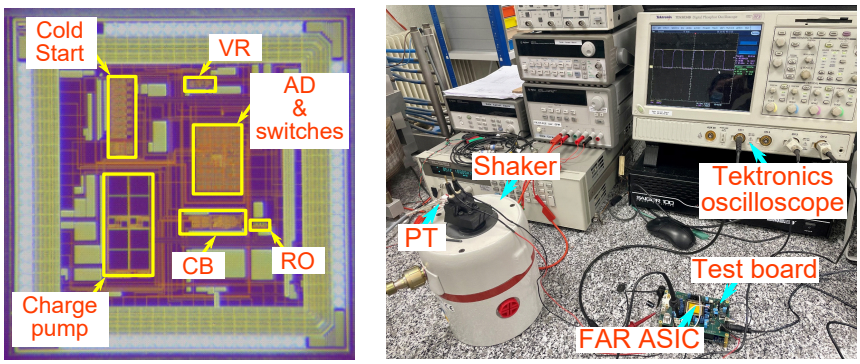


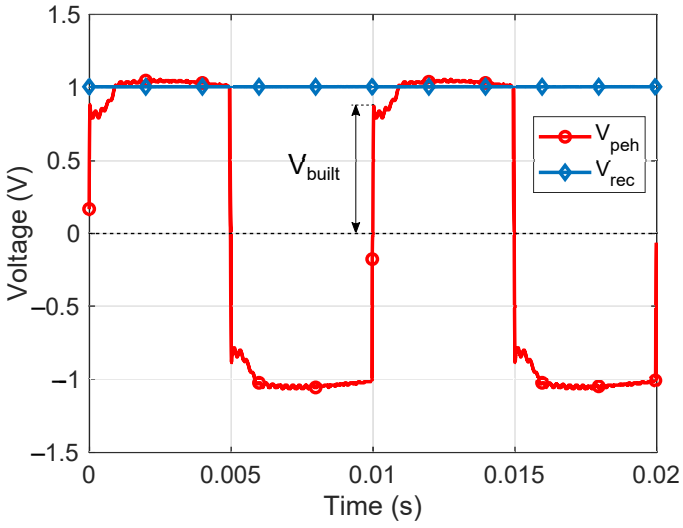
Figure 11. Transistor-level transient simulation results: V_{peh}, V_{rec} and control signals.



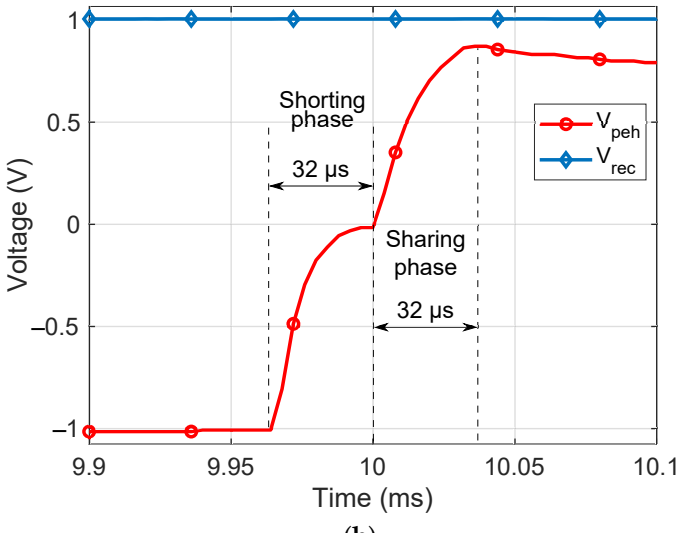
(**a**) (**b**)

Figure 12. (**a**) FAR ASIC micrograph. (**b**) Experimental test bench.

Note that with $C_L = 100\,\mu F$, the voltage ripple ΔV on V_{rec} is negligible (i.e., below 1 mV).



(**a**)



(**b**)

Figure 13. (**a**) Measured waveform of V_{peh} and V_{rec}, and (**b**) Zoom view during the voltage flip operation. VR regulatedV_{rec} to $\hat{V}_{OC} = 1\,V$.

To evaluate the benefit of the proposed voltage flip enhancement principle on power efficiency, we measured the output power in both FAR and Switch-only mode. For this experiment, we applied a variable load resistance and disabled VR. Figure 14a shows the output power as a function of $1/R_L$. One can clearly see that FAR achieved better power performance as $1/R_L$ increased and delivered around 100% more power than Switch-only for $1/R_L \simeq 0.024\,\mathrm{S}$ ($R_L \simeq 41\,\mathrm{k\Omega}$). Yet, as demonstrated in Section 2.3.2 (see Figure 9), for a given value of R_L, both architectures did not yield the same output voltage. Therefore, for a more realistic comparison, Figure 14b shows the output power as a function of V_{rec}. For both architectures maximum power was achieved when $V_{rec} \simeq \hat{V}_{OC}$. As mentioned in Section 2.3.2, Switch-only achieved slightly better performance than FAR with $P_{SO_{max}} = 19.3\,\mu\mathrm{W}$ and $P_{FAR_{max}} = 19.1\,\mu\mathrm{W}$, respectively. Yet, for a given value of $V_{rec} < \hat{V}_{OC}$, FAR delivered up to 20% more power than Switch-only. This result confirmed the theoretical demonstration (Section 2.3.2) that FAR achieved better power efficiency than Switch-only under load constraint. It is also worth pointing out that FAR kept operating, and the efficiency improvement ratio remained almost constant (around 20%), for V_{rec} as low as 0.7 V, i.e., as the load constraint increased (when R_L drained more current from C_L). Note that for $V_{rec} < 0.5\,\mathrm{V}$, the ASIC was unable to work properly.

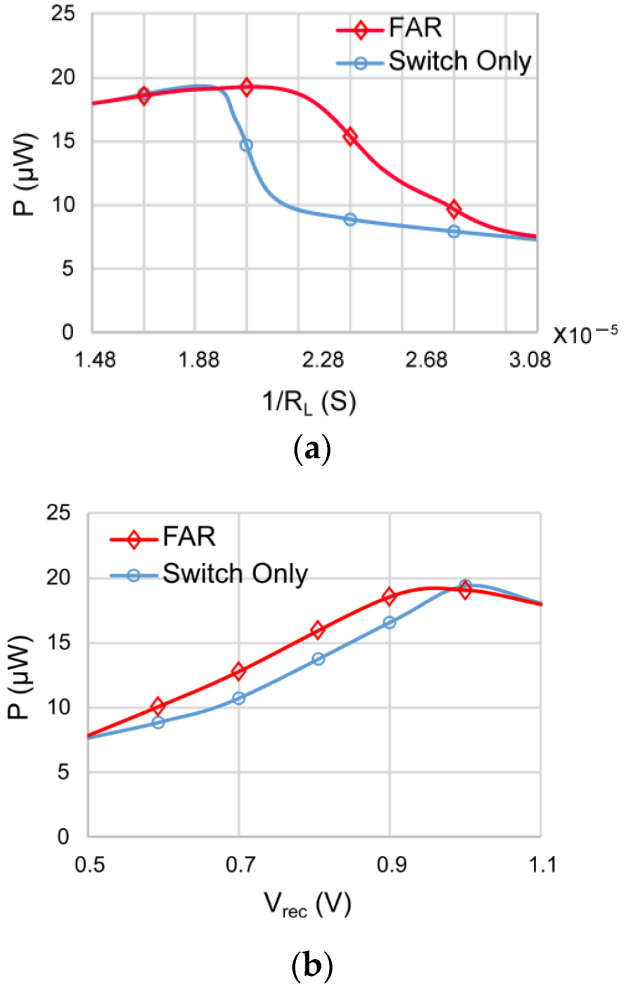


Figure 14. Output power as a function of (**a**) $1/R_L$, (**b**) V_{rec}.

Concerning absolute value, the measurements revealed that the power improvement of FAR over Switch-only was much more significant than the simulations presented in Figures 9 and 10. The reason is that FAR was more robust against circuit non-idealities than Switch-only, and particularly against the offset of the AD comparator, which can be as high as a few millivolts. Indeed, in FAR, during the sharing phase SW_3 shorted the inputs

of the AD comparator and the voltage at node V_{sp} was pre-charged to V_{rec}. This caused the comparator to flip state shortly after the sharing phase had been completed, as mentioned in Section 2.2.3. Conversely, in Switch-only V_{peh} first had to overcome the offset of the AD comparator before power extraction started. The influence of the offset was particularly important for large C_L as a few millivolts difference between V_{rec} and V_{peh} may represent a large amount of charge and thus a large power difference. For the time being, this was the most tangible assumption, but further investigations are currently under way to gain a better understanding of this phenomenon.

The maximum output power improving rate (MOPIR) (Ramadass and Chandrakasan [17], Chen et al. [21]) allows the comparison of FAR power performance with that of a conventional FBR.

$$MOPIR = \frac{P_{FAR}}{P_{FBR}} \tag{16}$$

where P_{FAR} and P_{FBR} are the output powers of FAR and FBR, respectively. The maximum output power of FBR is (Ramadass and Chandrakasan [17])

$$P_{FBR_{max}} = C_{peh} f_{ex} \left(\hat{V}_{OC} - 2V_{th} \right) \tag{17}$$

where V_{th} is the diodes' threshold voltage. If we consider a conventional Schottky-diode based FBR with high-performance diodes having a low V_{th} ()around 0.3 V), using a FBR under the same operating condition as the FAR yielded $P_{FBR_{max}} = 1.6\,\mu W$. The MOPIR was thus around 11.94×.

Table 2 compares the proposed FAR concept with some of the best results available in the recent literature. As mentioned in the introduction, discussing absolute raw performance was not the object of this paper. When considering the FAR as a stand-alone rectifier solution, the power efficiency was equivalent to Switch-only, which was much lower than the SSHI or SSHC systems referenced in the table. Hence, the PIC was lower compared to the state-of-the-art. Nevertheless, the FAR operated with an open circuit V_{OC} of only 1 V while the latest systems usually have a larger V_{OC}. Therefore, compared to a conventional diode-based FBR, the output power ratio of FAR was much higher, and above all, helped keep power efficiency as the load constraint increased.

Table 2. FAR performance compared to the state-of-the-art architectures.

Reference	JSSC [3]	ISSCC [2]	ISSCC [31]	JSCC [17]	This Work
CMOS process	0.35 µm	0.18 µm	40 nm	0.35 µm	0.35 µm
Energy Harvesting Technique	SSHC	SPFCR	SECE	SSHI	SSHC
PT model	Mide V21BL	Mide PPA1021	Mide PPA1011	Mide V22B	S118-J12S-1808YB
C_{peh}	45 nF	22 nF	43 nF	18 nF	100 nF
f_{ex}	92 Hz	200 Hz	75.4 Hz	225 Hz	100 Hz
$\hat{V}_{OC}$	2.5 V	1.6 V	2.85 V	2.4 V	1 V
PIC [(a)]	161.8 µW	64 µW	82.6 µW	56 µW	19.1 µW
MOPIR	2.7–9.7	9.3	3.14	4	11.94

[(a)] PIC: maximum output Power of the Interface Circuit.

4. Conclusions

This paper reported on a simple concept of voltage flip enhancement for piezoelectric energy harvesting. A thorough analysis of the power performance revealed that, besides the boost effect on the voltage flip, the FAR principle also helped improve the power efficiency of the PEH, especially as the load constraint increased. The FAR can be used as a fully integrated standalone rectifier solution, and is particularly well suited for low-voltage operation. Yet, it may also be considered as an additional boost solution to improve the

performance of more a complex PEH architecture such as SSHI or SSHC. Experimental results performed on a CMOS prototype confirmed that, under load constraint, the FAR principle achieved better performance compared to Switch-only, and is more robust against circuit non-idealities. These conclusive results opened interesting research perspectives that we are currently working on, consisting of combining the FAR principle with SSHI or SSHC to improve both voltage flip and power efficiency.

Author Contributions: Conceptualization, V.F., L.W.; methodology, V.F., E.J.; resources, V.F., L.W., E.J.; writing—original draft, V.F.; writing—review and editing, V.F., E.J. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the Agence Nationale de la Recherche: ANR-18-CE09-0033.

Conflicts of Interest: The authors declare no conflict of interest.

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