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Abstract— **In this paper, application of a five-leg converter in Doubly Fed Induction Generator (DFIG) for Wind Energy Conversion Systems (WECS) is investigated. The five-leg structure and its PWM control are studied and performances are compared with the classical six-leg topology. The main drawback of five-leg converter with respect to the six-leg back-to-back converter is the need to increase the dc-link voltage for the same operation point, i.e. the same powers in case of WECS. So, different methods for the reduction of the required dc-link voltage in the five-leg case are studied. The five-leg converter is used to replace the conventional six-leg one, with the same ability. For the performance evaluation of this structure and its fully digital controller in a more realistic and experimental manner, Hardware in the Loop experiments are carried out. It is shown that efficient control of active and reactive powers and dc-link voltage is performed. Hardware in the Loop results demonstrate the high performance of the proposed fully digital control which is implemented on an Altera FPGA target.**

Keywords: Wind Energy Conversion System (WECS), Five-leg converter, Doubly-Fed Induction Generator (DFIG), Hardware in the Loop (HIL).

1. INTRODUCTION

Wind energy is the fastest growing type of renewable energy. One can notice an average growth rate of about 30% for installed wind turbines in the past 10 years. At the end of 2020, the installed capacity of wind turbines is expected to be around 1900 GW [1]. For European wind energy association, the goal is to produce 26 to 34% of the electricity of Europe from wind in 2030 [2]. Global market of wind energy is clearly expanding steadily, and consequently the technologic competition in this area has been accelerated.

The most widely used structure in currently installed wind turbine is the Doubly-Fed Induction Generator (DFIG) -based wind turbine. One of its major advantages over other variable-speed turbine structures with a series converter is the reduced rating of the power electronic converter. The maximum power that the power converter has to handle in steady state condition is reduced to a fraction (20-30%) of the output rated power [3].

On the one hand, repairing a Wind Energy Conversion Systems (WECS) is a very time consuming process [4], and actually, in most cases, the repairing is scheduled annually [5]. Therefore, continuity of service and reliability are mandatory for such applications. This is again more important for islanded smart or micro grids where wind power has a major role, and the higher reliability of the converter of wind turbine is highly recommended.

On the other hand, five-leg converter topology has been proposed for drive applications such as independent control of two three-phase motors [6], fault tolerant reversible AC motor drive systems [7] and AC/AC supply of a three-phase induction machine [8]. It has been shown that this converter topology could give satisfactory results in such applications. Moreover, it has better performances over other component-minimized topologies like nine-switch converter [9] and half-bridge-based converters [7]. In [9], it is shown that in this topology, the switches rating and losses are lower compared to 9-switch converter. In [7] it is stated that in contrary to the half-bridge-based converters, there is no AC current flowing through dc link capacitors in the five-leg converter, and also the required dc-link voltage can be minimized. Finally, the use of a reduced number of power devices leads to higher converter reliability compared with the conventional back-to-back six-leg topology.

However, as far as DFIG-based WECS is concerned, the application of a five-leg converter topology and the study of the suited control and dc-link voltage minimization has never been reported in the literature. We think that such a converter topology might be interesting and efficient for this purpose.

In this paper, a five-leg converter-based structure as the back to back converter of a DFIG based wind turbine is studied. It is shown that it might have some benefits compared to conventional 6-leg "back to back" converters. In the next section, the overall system under study is explained. Moreover, control of the DFIG, the dc-bus voltage and the five-leg converter is developed. In the third section, a comparative study of five-leg and six-leg converter topologies in WECS with DFIG is presented. Also different schemes for the minimization of the required dc-link voltage in the five-leg converter for wind application are discussed. Two PWM

patterns for five-leg converter are studied in the forth section. Finally, Hardware in the Loop (HIL) experiments are presented for a 3 MW WECS, based on a FPGA-based HIL platform, developed in our laboratory [10].

2. FIVE-LEG CONVERTER IN WECS WITH DFIG

The structure and control of a WECS with DFIG fed by a five-leg converter is different from the conventional scheme with 6-leg converter, but there are also some similarities. A conventional WECS with a six-leg converter is shown in Fig. 1. The stator is directly connected to the grid, and the rotor is connected through a back-to-back (six-leg) converter to the mains. This converter allows controlling the dc-link voltage, the input power factor, and also controls the DFIG (electromagnetic torque and stator power factor).

Different methods for controlling WECS with DFIG are suggested in the literature [11-13]. In [11] a discrete power control for DFIG is presented. In [12] a modulated hysteresis current controller is used to control the rotor currents. The classical DFIG control consists of calculating the suitable voltage references for each three-leg converter. Then, by using PWM control units, the suited gate signals for switches are computed. For the Rotor Side Converter (RSC) voltage references calculation, a grid-voltage oriented method is used [13]. The reference frame is chosen so that the q-axis component of the stator flux vector is null. In this reference frame, the electromagnetic torque (T_e) and the stator reactive power (Q_s) are related to q and d axis components of the rotor currents and are expressed by:

$$T_e = -p\frac{(mL_m)}{L_s}\varphi_{sd} i_{rq} \quad (1)$$

$$Q_s = V_{sq}\ \varphi_{sd}\ L_s - V_{sq}\frac{(mL_m)}{L_s} i_{rd} \quad (2)$$

$$V_{rq} = R_r i_{rq} + \frac{(\sigma L_r di_{rq})}{dt} - \sigma L_r \omega_r i_{rd} + \frac{(\omega_r mL_m)}{L_s}\varphi_{sd} \quad (3)$$

$$V_{rd} = R_r i_{rd} + \frac{(\sigma L_r di_{rd})}{dt} - \sigma L_r \omega_r i_{rq} \quad (4)$$

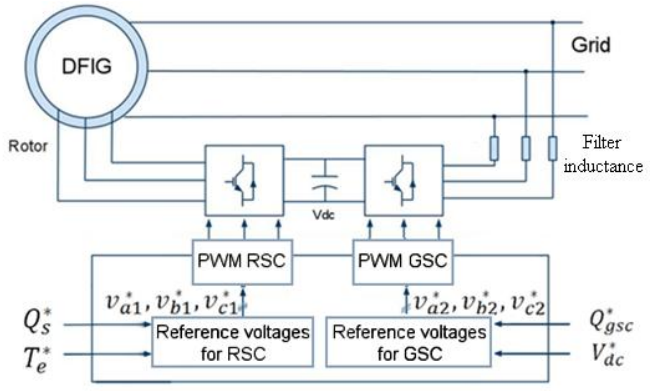

Figure 1. Conventional WECS with DFIG based on a six-leg converter.

By using PI controllers and by applying feed-forward compensation terms, the control of torque and reactive power is performed. Fig 2 shows the block diagram of the RSC control [13].

The grid-side converter (GSC) is normally controlled in order to regulate the dc-bus voltage and provide unity power factor at the point of connection to grid. This is done using another well known grid-voltage oriented control for the three phase controlled rectifiers [13, 14].

Two sets of voltage reference obtained from these control schemes are normally sent to the two respective PWM blocks in conventional systems, as is shown in Fig. 1.

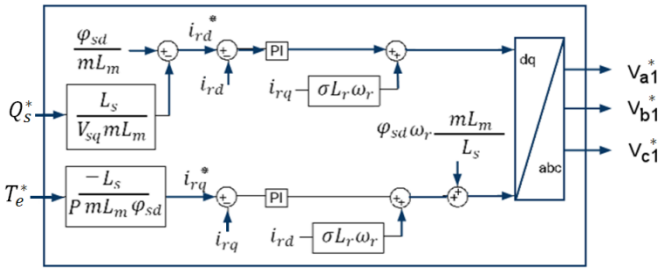

Figure 2. RSC control [13].

However, for a 5-leg converter the procedure is different. For the proposed scheme with a five-leg converter, as the converter topology is different, the PWM control must be changed. Fig. 3 shows the proposed WECS with DFIG based on a five-leg converter. Since the number of legs is reduced, the number of output control signals should be reduced too. Therefore a modified and suited PWM scheme for five-leg converter must be used. However, the voltage references generation units remain the same in five and six-leg cases. Thus, with an appropriate PWM method, the generation of the two desired set of three-phase voltages at grid and rotor sides is possible. The PWM method is explained later in section 4.

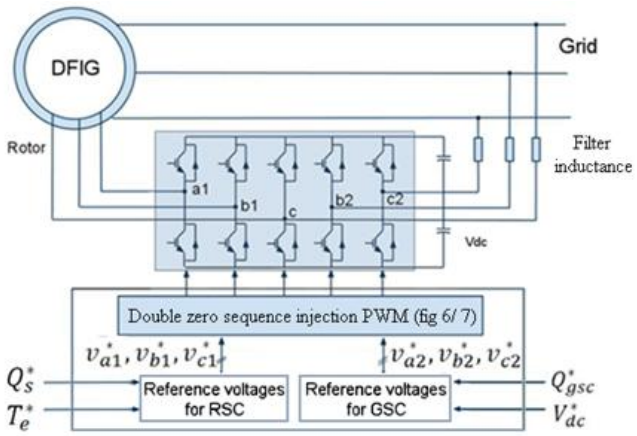

Figure 3. WECS with DFIG based on a five-leg converter.

3. COMPARISON OF FIVE-LEG AND SIX-LEG CONVERTERS IN WECS WITH DFIG

DFIG systems based on five-leg and conventional back-to-back converters may be compared in different ways. However, notice that in our work both are supposed to produce the same active power.

In [15], general 3n-leg and (2n+1)-leg converters topologies are compared. It is demonstrated that in component-minimized converters there is a limit on the sum of the voltages on the two side of converter (in this case, rotor side or grid side) for a given dc-bus voltage. Let us consider a six-leg converter with a dc-link voltage equal to V_{dc}. Such a converter can produce three-phase sinusoidal voltages with a maximum peak phase voltage of V. The modulation index M is defined as $2V/V_{dc}$. So, the peak value of the phase to phase voltage will be:

$$V_{ll} = M\sqrt{3}V_{dc}/2 \qquad (5)$$

Consequently, the maximum of the modulation signal is $2/\sqrt{3}$, because the produced line to line voltage cannot be larger than V_{dc}.

For the five-leg converter, the peak value of line to line voltage between legs j_1 and i_2 $(i, j \in \{a,b\})$ can be written as:

$$V_{j1} - V_{i2} = V_{j1} - V_c + V_c - V_{i2} = V_{jc(1)} + V_{ic(2)} \qquad (6)$$

where subscripts 1 and 2 point to two different sides of the converter (rotor side and grid side). In the other words, the peak value of line to line voltage of V_{j1i2} is equal to the sum of two line-line voltages from two sides of the converter, meaning V_{j1} and V_{i2}. Substituting (5) in (6) we will have:

$$V_{j1i2} = V_{j1} - V_{i2} = \frac{(M_1 + M_2)\left(\sqrt{3}V_{dc}\right)}{2} \qquad (7)$$

where M_1 and M_2 are the modulation indexes for two sides of the converter. Therefore, in the five-leg converter with the same dc-link voltage (compared with a six-leg topology), the magnitude of peak sinusoidal phase voltages at the two sides of converter must satisfy $V_1 + V_2 \le V$, in which the voltages V_1 and V_2 are peak phase voltages from two different sides of the five-leg converter. In the proposed WECS with DFIG, one side of the five-leg converter is connected to the grid via an inductive filter. Since the impedance of filter is not very high, the magnitudes of the voltages in two sides of the filter are of the same order. Depending on the design of the power system, different possibilities should be considered. For example, if the power system is designed in such a way that the maximum voltage to be generated across the rotor slip rings is the same as the grid side voltage, then to guaranty the same capability as for six-leg converter, the five-leg converter has to work with a dc-link voltage twice larger than for a six-leg one.

In the following, the available complementary solutions and approaches to reduce the required dc-bus voltage for the proposed structure of five-leg converter in DFIG case are proposed and studied.

If the maximum voltage required on the rotor side is only a fraction of voltage on the grid side (for example with a stator to rotor turn ratio of 1, and considering that in steady state $v_r / v_s = s$, where s stands for the induction machine slip) in this case only a small increase of dc-link voltage is needed, compared to the case of a conventional back-to-back converter (about 1.3 times, considering a classical maximum slip equal to 0.3). Therefore by designing correctly the rotor to rotor turn ratio, a minimization of the required dc-link voltage in the five-leg converter can be obtained. Choosing a larger stator to rotor turn ratio also has other advantages, like enhancing the compensated capability for network unbalance [16].

Current rating of the switches in both converters are the same, except for the common leg of the 5-leg converter. Current rating for this leg is smaller than the sum of the current ratings in the two corresponding legs of a six-leg converter. Overall, one can say that power rating of switches used for the five-leg converter is larger than for the 6-leg converter. This ratio based on the design of WECS with DFIG is approximately about 1.3 with a DFIG stator to rotor turn ratio of 1 and without any other modifications.

More, the required dc-link voltage may be still reduced by other appropriate modifications in the control scheme, discussed in the following. Three optimization approaches are proposed here.

First, a reduction of the voltage references of the grid side and therefore that of the dc-link voltage is proposed, based on the modification of the reference Q_s^* while active power is unchanged. In fact, by increasing the d-axis component of the GSC, the required voltage at the grid side of the converter might be reduced. Fig. 4 illustrates this matter. The q-axis component of the input current is calculated based on dc-voltage control scheme. However, modifying i_d in order to decrease the required voltage in the grid side will result to reactive power absorption from the grid.

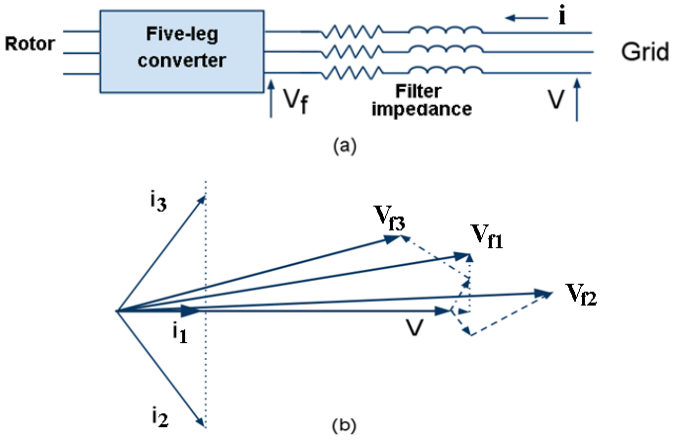

Figure 4. (a) converter to grid connection- (b) V_f for three different grid currents.

In a similar manner, a reduction of the voltage references for the rotor side voltages is proposed. For these voltages in steady state, using (3) and (4) and neglecting rotor resistance we have:

$$V_{rq} = R_r i_{rq} + \sigma L_r \omega_r i_{rd} + \frac{\omega_r m L_m}{L_s} \varphi_{sd} \quad (8)$$

$$V_{rd} = R_r i_{rd} + \sigma L_r \omega_r i_{rq} \quad (9)$$

$$|V|^2 = \omega_r^2 \left(\sigma^2 L_r^2 + (\frac{mL_m}{L_s} \varphi_{sd})^2 + 2 \frac{mL_m}{L_s} \varphi_{sd} \sigma L_r i_{rd} \right) = f(\omega_r, i_{rd}) \quad (10)$$

Therefore the required voltage is a function of ω_r and i_{rd} . Clearly decreasing $|\omega_r|$ will result in the reduction of the required rotor voltages. This means that by using a narrower speed variation range around the synchronous speed, required rotor-side voltage will decrease. In the areas where the wind speed variation is not severe, like in offshore areas, narrowing the speed-variation range of the rotor will be an interesting solution for reducing the required voltage at the rotor-side and consequently at the dc-link. On the other hand, the magnitude of the rotor voltage is also related on i_{rd} . For studying the effect of i_{rd} , we consider ω_r as constant, therefore one can see that $|V|^2$ is a second order function of i_{rd} , and it can be shown that for a negative i_{rd} will decrease $|V|^2$. Its minimum value is reached for

$$i_{rd(opt)} = -\frac{\varphi_{sd}(mL_m)}{L_s \sigma L_r} \quad (11)$$

This could be a large value. Overall it is evident that reduction in the required rotor-side voltages is possible in both cases, but it seems that the reduction of the rotor voltage by ω_r is more efficient.

In summary, to achieve the same performances as a six-leg converter in any case, a five-leg converter needs a larger DC-link voltage. However it is possible to reduce this increase by:

- using a larger stator to rotor turn ratio ;
- changing the d-axis component of input current of grid side (Fig 4);
- changing the d-axis component of input rotor current;
- narrowing the speed range around the synchronous speed.

On a different subject of comparison, five-leg converter has two switches less than the conventional converter. Such reduction of the devices and drivers number results in cost reduction. Moreover, the lower number of devices will lead to higher reliability. This is essential in WECS, especially as far as small grids and micro grids are concerned. That is true for large grids too, where the power converter is a key element, because of the time-consuming process of WECS repairing. Note that in many cases, WECS are installed in areas with difficult access (particularly offshore), and maintenances are programmed annually [5].

4. PWM FOR FIVE-LEG CONVERTERS

Several PWM approaches are proposed for five-leg converter [6, 8 and 17]. Different PWM methods for a five-leg converter topology for motor drive applications have been compared in [17], and the authors conclude that the method suggested in [6], using all 32 possible voltage vectors, produces less voltage harmonics. In this approach, the so-called "double zero-sequence injection method" is used. Six fundamental voltage reference signals $v_i^*(i = a,b,c)$ for the two sides are calculated using classical methods based on field oriented or voltage oriented control. Each set of three-phase voltage references are sent to the corresponding PWM unit. Then, a zero sequence signal (ZSS) is added to those references to form the modulation signals. In fact, ZSS does not change the output line-to-line and phase voltages, therefore it is used as a degree of freedom to reduce the current harmonics and improve the dc-bus utilization [14, 17].

$$v_i(t) = v_i^*(t) + v_{zs}(t) \quad (12)$$

This procedure is shown in Fig. 5. New calculated reference voltages $(v_i \ , i = a,b,c)$ are then sent to a PWM unit.

Different zero-sequence signals are proposed in the literature, but a few of them have gained wide acceptance. The PWM methods with ZSS addition can be divided into continuous and discontinuous methods. In continuous PWM method, modulation signals vary between the limits imposed by the triangular carrier signal. In discontinuous PWM method, the modulation signals are alternatively clamped to one of the dc-link rails. In [18] different PWM methods with ZSS addition are studied and their relationship with Space Vector Modulation (SVM) methods are established. The most widely used ZSS for a three-phase system is calculated as below:

$$v_{zs}(t) = -1/2(max(v_a^*(t) + v_b^*(t) + v_c^*(t)) + min(v_a^*(t) + v_b^*(t) + v_c^*(t))) \quad (13)$$

Using (13), ZSS for a three voltage references can be calculated. This value is added to the three voltage references to form modified references.

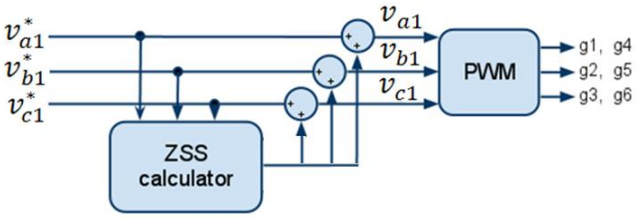

Figure 5. Conventional ZSS for three reference voltages

Repeating this process for two sets of three-phase voltages, we will have 6 voltage references. Now, since we have 6

voltage references and only 5 legs, a reduction of the voltage references number is required. In [17], a simple method is studied that suggests to to add a modified ZSS dedicated to the converter configuration in five-leg mode. For the PWM generation in the five-leg converter, five voltage references are calcuated as below:

$$\begin{aligned} v_{A1} &= v_{a1} + v_{c2} \quad ; \quad v_{B1} = v_{b1} + v_{c2} \\ v_{C} &= v_{c1} + v_{c2} \quad ; \quad v_{A2} = v_{a2} + v_{c1} \\ v_{B2} &= v_{b2} + v_{c1} \end{aligned} \tag{14}$$

Since the same signal is added to all of the three reference values of each side, it does not affect the fondamental output voltage of that side. Fig.6 shows the principle of this method.

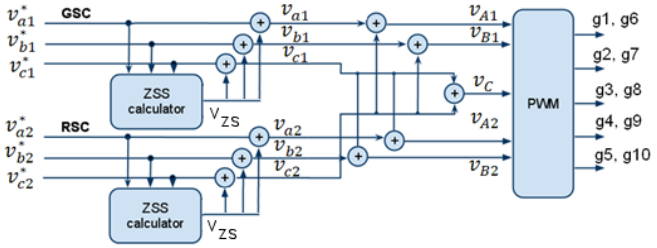

Figure 6. Principle of PWM control for a 5-leg converter

We will call this method ZSS1. But in a different scheme [15], it is possible to change the order of these two steps of ZSS addition. In fact, the ZSS shown in (13), which is widely used in three-phase systems, can be used for systems with higher phase numbers. Thus, in a more general form, ZSS for voltage references $\left(v_1^*, v_2^*, \ldots v_N^*\right)$ can be calculated as:

$$\begin{aligned} v_{zs}(t) = -1/2(max(v_1^*(t) + v_2^*(t) + \ldots + v_N^*(t)) + \\ min(v_1^*(t) + v_2^*(t) + \ldots + v_N^*(t))) \end{aligned} \tag{15}$$

Using this approach first a reduction in the number of voltage references is done:

$$\begin{aligned} v_{A1}^* &= v_{a1}^* + v_{c2}^* \quad ; \quad v_{B1}^* = v_{b1}^* + v_{c2}^* \\ v_{C}^* &= v_{c1}^* + v_{c2}^* \quad ; \quad v_{A2}^* = v_{a2}^* + v_{c1}^* \\ v_{B2}^* &= v_{b2}^* + v_{c1}^* \end{aligned} \tag{16}$$

and then using a second ZSS the final references are calculated:

$$\begin{aligned} v_{A1} &= v_{A1}^* + v_{zs} \quad ; \quad v_{B1} = v_{B1}^* + v_{zs} \\ v_{C} &= v_{C}^* + v_{zs} \quad ; \quad v_{A2} = v_{A2}^* + v_{zs} \\ v_{B2} &= v_{B2}^* + v_{zs} \end{aligned} \tag{17}$$

This is proposed in [15] for a 2n+1 leg converter and is examined for a 7 leg converter. However it seems that this is not validated for the five-leg converter, and a comparison of these two methods is not reported. This method will be called as ZSS2. The principle of this method is shown in Fig. 7.

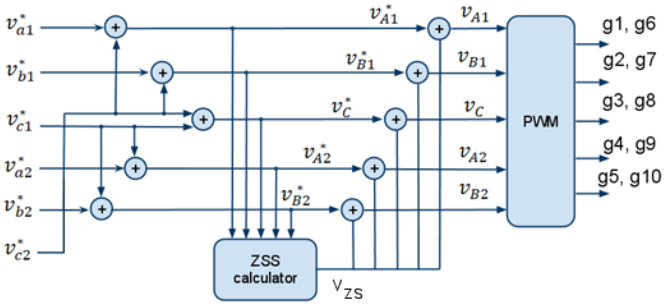

Figure 7. Principle of ZSS2 PWM control.

These two PWM methods will be used in the later experiments. In both cases, the voltage references for the GSC and RSC will be computed using the mentioned methods in section 3, and then these two sets of voltage references will be sent to the PWM unit which produces the gate signals for the converter. All control and PWM units will be implemented on a FPGA target. Details of the implementation and verification of the digital controller are provided in the following section.

5. HARDWARE IN THE LOOP PRINCIPLE

Fully digital Control of a WECS with DFIG, based on a five-leg converter, is possible by implementing the control scheme on a single FPGA chip. Effectiveness of FPGA for control of power-electronic converters has been proved in [19, 20]. For verifying the digital controller, we use a HIL–based platform, developed in our laboratory for implementation and verification of electrical system digital controllers [10].

Designing and testing digital control systems for power electronic applications can be expensive and time consuming. Traditional simulations cannot exactly reproduce the real conditions, because they do not take into account some limitations of real controllers, like the finite resolution of registers or saturation of values in fixed point systems during the intermediate steps of calculation. Also, the fully experimental tests may not be always possible or may bring the risk of serious damage. One interesting solution to eliminate the risk of damaging the real plant while testing the digital controller in a realistic manner is Hardware-in-the-loop (HIL) analysis [21]. For FPGA in the loop prototyping, we have used Dspbuilder blocks to implement the developed fully digital control in Simulink environment. This solution gives us the possibility of visual programming and therefore is very interesting for rapid FPGA prototyping. However, some of the desired functions are not available in these blocks and must be constructed from other blocks or imported using HDL programming. The designed system is then translated to VHDL and compiled and sent to the FPGA chip. During FPGA in the loop simulations, the FPGA receives at each step the required signals from Simulink (i_{a1}, i_{b1}, i_{a2}, i_{b2}, v_{dc}, speed…) and calculates the control signals of the system based on the implemented programs and sends them back to Simulink. Data communication between the FPGA and the computer is performed via a Joint Test Action Group (JTAG) interface.

In this experiment a Stratix DSP S80 development board is used. This board includes the Stratix EP1S80B956C6 FPGA chip which contains 79,040 programmable logic elements. The development board has an on-board 80-MHz oscillator.

Fig 8 shows the FPGA in loop prototyping. Fig 9 shows the "FPGA in the loop" implementation flow.

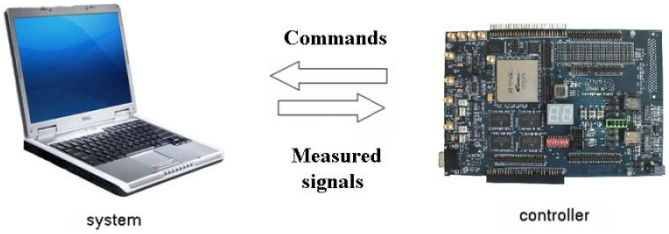

Figure 8. "FPGA in loop" prototyping.

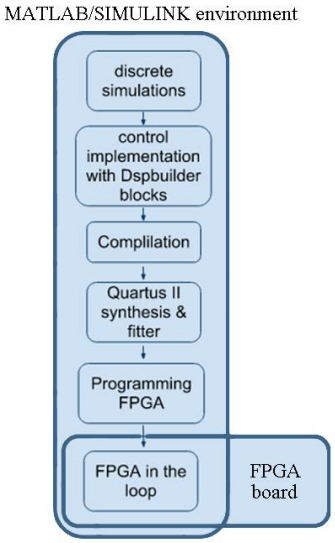

Figure 9. The FPGA implementation flow.

6. HARDWARE IN THE LOOP EXPERIMENTS

First, Hardware in the Loop experiments are carried out in order to evaluate the effectiveness of the five-leg converter for WECS with DFIG and to compare the performances of the two PWM methods ZSS1 and ZSS2 for this application. The effectiveness of the proposed schemes for the minimization of the required dc-link voltage is also studied. Data of the studied 3 MW WECS with DFIG are summarized in Table 1. Subscripts s and r point to stator and rotor parameters, respectively.

In order to have a minimum dc-link voltage, a stator to rotor turn ratio equal to 1 is chosen [22, 23] (see table 1). Further studies of the other methods of reducing the required dc-link voltage are presented later. Results are obtained using the ZSS1 PWM scheme for the five-leg converter and later a comparison with the ZSS2 is made.

TABLE I. WECS WITH DFIG PARAMETERS

Electrical grid	Phase to phase voltage: $U_n = 690V$ Frequency: f=50 Hz
Wind turbine	Diameter= 80m Gear box ratio= 100 Inertia: $J_T = 1.4*10^6 Kg.m^2$
DFIG	$R_s = 2.97m\Omega, R_r = 3.82m\Omega, L_s = 12.241mH,$ $L_r = 12.177mH, M = 12.12mH$ $P_n = 3MW, f = 50Hz, J_m = 114Kg.m^2$
DC bus	$V_{dc} = 1500V$ C= 38 mF
GSC filter	$R_f = 0.1\Omega, L_f = 1mH$

Results are divided in two parts. First in Figs 10-17, the ability of five-leg converter for the WECS with a DFIG is studied. It is shown that five-leg converter can work well for this application, meaning that active and reactive powers and dc-link voltage are controlled very well. Then, in the second part in Figs 18-22, the results of the methods of minimizing the required dc-link voltage are presented. Figs 10-14 show dc-link voltage, active and reactive powers of stator of DFIG and d and q components of rotor current respectively. Input active power is changed via a ramp change in wind speed from 1s to 1.15s. Zero, negative and positive values are used as reactive power reference, and these steps are applied at 0.8s, 1.2s and 1.6s respectively. It is shown that good control of active and reactive powers is obtained. Also these changes in the references of reactive powers help us to study later their effect on the magnitude of the voltage references of the grid-side and the rotor-side.

Moreover, control of the dc-link voltage is also well performed. Dc-link voltage is constant and equal to its reference, i.e. 1500V. The waveform of V_{dc} is presented in Fig. 10.

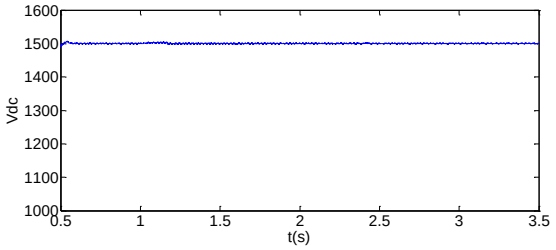

Figure 10. DC- link voltage.

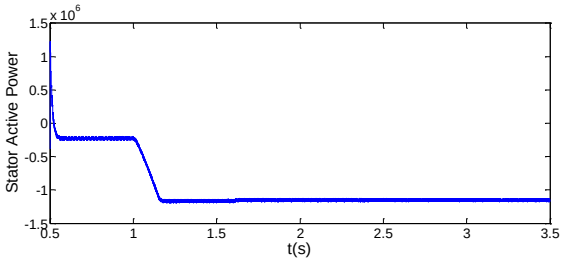

Figure 11. Active power control for a ramp in wind speed.

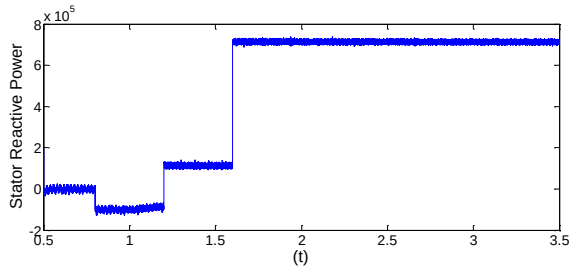

Figure 12. Stator Reactive power control.

Increasing wind speed has resulted in increased input power; therefore stator active output power is increased also, as shown in Fig. 11. Fig 12 shows the response of stator reactive power to positive and negative steps. d and q-axis components of rotor current are shown in Figs 13, 14. The relation between these currents and active and reactive stator powers is visible in these figures.

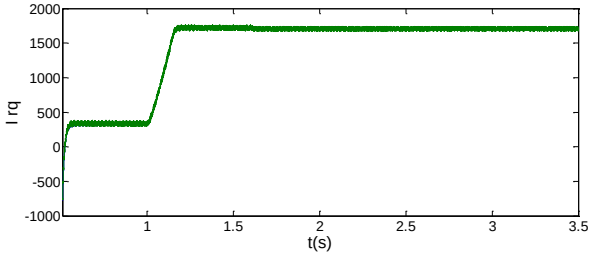

Figure 13. q-axis component of rotor current.

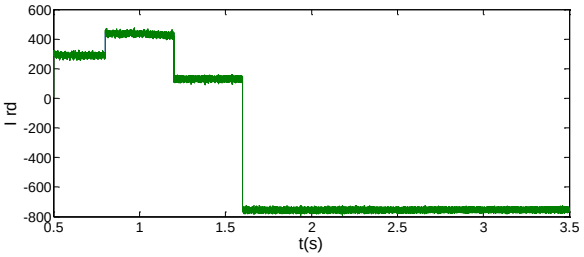

Figure 14. d-axis component of rotor current.

Figs 15-17 present the reactive power of grid side, the currents of the legs a_1, b_1 and c of the five-leg converter and a zoomed view of these currents respectively. Changing the reactive power of the grid-side also helps us later to evaluate its influence on the grid-side reference voltages and to evaluate the performances of the control system. Efficient control of the grid side reactive power can be seen in Fig 15. Clearly control of DFIG is well done with five-leg converter.

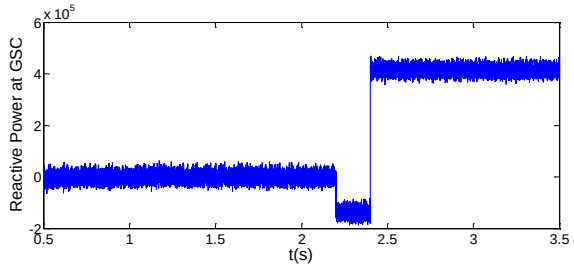

Figure 15. Reactive power control of the grid side.

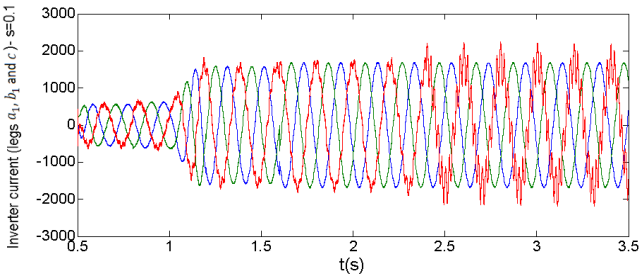

Figure 16. Current of legs a_1, b_1 and c for s=0.1 .

Fig 16 shows the currents of legs a_1, b_1 and c of the five-leg converter. Currents of the legs a_1 and b_1 are equal to their corresponding rotor currents. However the current in the leg c is the sum of two currents (phase c of rotor side and phase c of grid side), therefore it is different and larger than the others. Fig 16 is zoomed in Fig 17. Clearly current rating in the common leg is larger than the other legs.

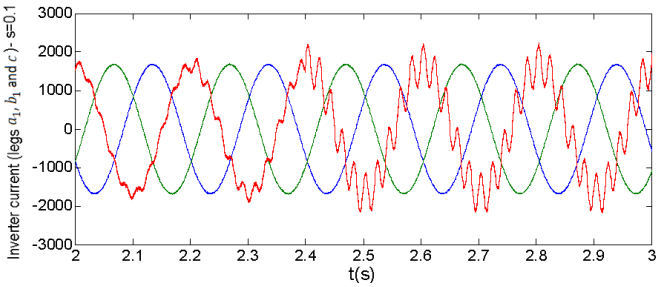

Figure 17. Zoomed view of current of legs a_1, b_1 and c.

Moreover, the reference value of the grid-side reactive power is changed at 2.2s to evaluate its effect on the grid-side voltage references. As it is shown in Fig 18, a larger I_d at grid side leads in the reduction of required voltage of the grid-side, at the expense of increase in the input reactive power and currents, as shown in the Fig. 4. On the other hand, effect of change of stator reactive power on the rotor-side voltage references is shown in Fig 19. As is shown in (10), it results in a reduction of the rotor-side reference voltages, but it is not as effective as in the previous case. Simulation is repeated for a smaller slip value in Fig 20 and clearly, using a smaller value of the slip has more effect in the reduction of the required rotor voltage.

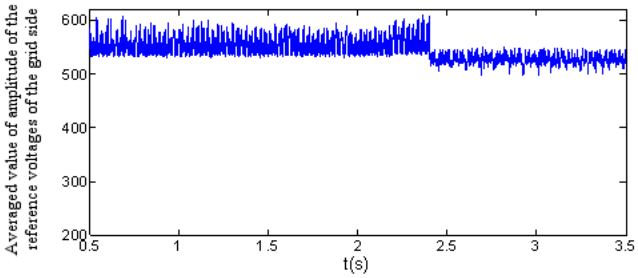

Figure 18. Averaged value of the grid-side voltage reference.

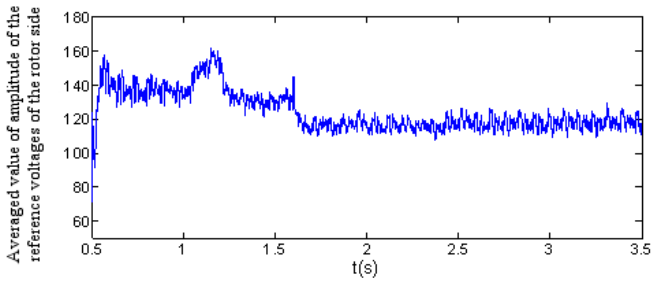

Figure 19. Averaged value of the rotor-side voltage reference for s=0.25.

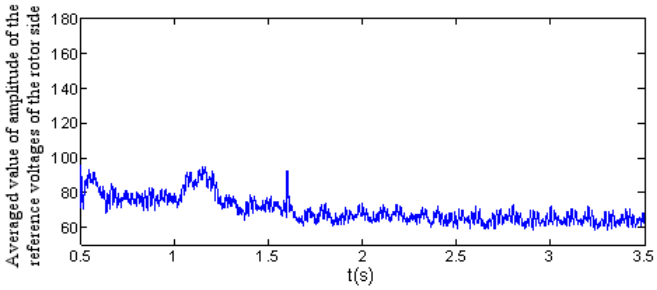

Figure 20. Averaged value of the rotor-side voltage reference for s=0.1.

The effect of the proposed methods for minimization of the required dc-link voltage on the instantaneous values of the voltage references in the PWM unit is studied in Figs 21 and 22. Fig. 21 shows the maximum of the five voltage references at the output of the ZSS1 unit. For ZSS2 the results are similar. In this test, the minimum required voltage at the dc-link in different situations is studied while s=0.1. At t=2.4s the reference of the stator reactive power is changed, based on (10), and then at t=2.8s the reference of the grid-side reactive power is changed based on Fig. 4. This is repeated for s=0.25 and the results are shown in Fig. 22. The transients can be seen in Fig. 21 at the changing moments of the reactive power references.

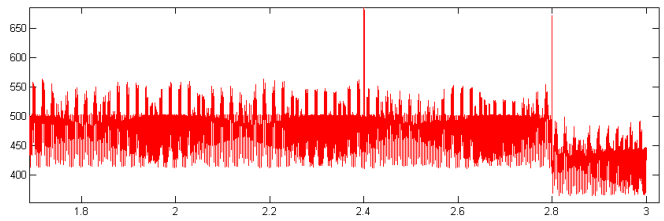

Figure 21. Maximum reference voltage for s=0.1 .

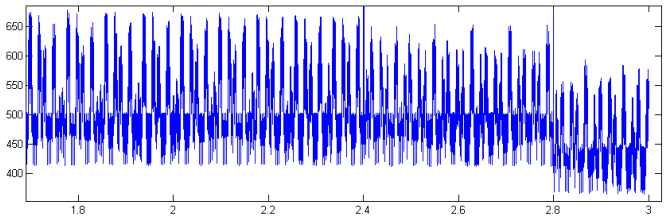

Figure 22. Maximum refrence voltage for s=0.25 .

It is shown again in these figures that the minimization of the required dc-link voltage using the proposed methods is effective. In the situation shown in Fig. 22 with s=0.25, a dc-link voltage about 1340 V (2*670V) is required. Changing the voltage reference of stator reactive power, this value may be reduced to 2*655=1310 V. Therefore, the effect of stator reactive power on the required dc-link voltage is not so important, as predicted in the theory. However after changing the reference of the grid-side reactive power, the required dc-link voltage maybe reduced to around 1160 V. Also it is evident that using a narrower band of operation around the synchronous speed (using smaller values of s) the reduction of required dc-link voltage is possible. The required voltage in the case with s=0.1 is about 1160 V and may be reduced to 970 V by changing the grid side reactive power reference.

On the other hand, the second PWM (ZSS2) approach is studied to be compared with the ZSS1. For the second PWM method, fundamental output voltages of the converter are the same; therefore all results (active/ reactive powers, dc-link voltage, etc) in both methods appear similar. The only difference is in the THD of the stator currents. These values are compared in Table II.

TABLE II. COMPARISON OF THD IN STATOR CURRENTS FOR ZSS1 AND ZSS2

	THD of i_a (%)
PWM ZSS1	0.62
PWM ZSS2	0.56

THD is slightly smaller for ZSS2. Eventually, one can conclude that these methods have similar performances for this application.

7. CONCLUSION

In this paper direct use of five-leg converter for WECS with DFIG is proposed. Using fewer devices, five-leg converter has better reliability which might be essential for some applications like in wind energy conversion systems, where repairing is a very time consuming process, and higher reliability of the converter is highly recommended.

Comparison with conventional six-leg converter in this application is carried out and dc-link voltage limit of this converter is studied. Different methods for minimizing the required dc-link voltage are proposed and studied. Also two PWM schemes for five-leg converter for this application are studied and compared. FPGA in the loop experiments are realized to verify the effectiveness of this converter for a 3MW turbine. It is shown that desirable control of active and reactive powers of DFIG and dc-link voltage is possible. Also the efficiency of the proposed methods for minimization of the required dc-link voltage is proved and their impacts are compared.

The proposed five-leg converter topology could also be interesting when considering a fault tolerant six-leg converter for WECS with DFIG. In such fault tolerant application, a conventional six-leg converter could be reconfigured to a five-leg converter after the occurrence of a fault in one of its

semiconductors or driver devices, therefore higher reliability and continuity of service will be achieved. In this application, it would be very efficient to reduce as low as possible the required dc-link voltage by narrowing the speed range around synchronous speed and changing the grid side reactive power. Then, the over-rating of the six-leg fault tolerant topology would be reduced as low as possible.

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