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A Novel PWM Control for a Bi-directional Full-Bridge DC-DC Converter with Smooth Conversion Mode Transitions

V.R.H. Lorentz, H. Schwarzmann, M. März, A.J. Bauer, H. Ryssel, L. Frey
Fraunhofer IISB, Erlangen, Germany
vincent.lorentz@iisb.fraunhofer.de

P. Poure

LIEN, Nancy Université, Vandœuvre-les-Nancy, France
philippe.poure@lien.uhp-nancy.fr

F. Braun

InESS, Strasbourg, France
francis.braun@adm-ulp.u-strasbg.fr

Abstract—A novel CMOS integrated pulse-width modulation (PWM) control circuit allowing smooth transitions between conversion modes in full-bridge based bi-directional DC-DC converters operating at high switching frequencies is presented. The novel PWM control circuit is able to drive full-bridge based DC-DC converters performing step-down (i.e., buck) and step-up (i.e., boost) voltage conversion in both directions, thus allowing charging and discharging of the batteries in mobile systems. It provides smooth transitions between buck, buck-boost, and boost modes. Additionally, the novel PWM control loop circuit uses a symmetrical triangular carrier, which overcomes the necessity of using an output phasing circuit previously required in PWM controllers based on sawtooth oscillators. The novel PWM control also enables to build bi-directional DC-DC converters operating at high switching frequencies (i.e., up to 10 MHz and above). Finally, the proposed PWM control circuit also allows the use of an average lossless inductor-current sensor for sensing the average load current even at very high switching frequencies.

In this paper, the proposed PWM control circuit is modelled and the integrated CMOS schematic is given. The corresponding theory is analyzed and presented in detail. The circuit simulations realized in the Cadence Spectre software with a commercially available 0.18 μm mixed-signal CMOS technology from UMC are shown. The PWM control circuit was implemented in a monolithic integrated bi-directional CMOS DC-DC converter ASIC prototype. The fabricated prototype was tested experimentally and has shown performances in accordance with the theory.

Index Terms—Integrated DC-DC converter, full-bridge topology, PWM control, mixed-signal CMOS technology.

I. INTRODUCTION

This paper presents a novel pulse-width modulation (PWM) control method for bi-directional DC-DC converters. In a first section, the theory of the basic DC-DC converter topologies are presented. In a second section, their combinations are used to analyze state-of-the-art operating principles of the full-bridge topology and compare them to the novel proposed PWM control. In a third section, the theory of the PWM control is presented and in a fourth section, the CMOS schematics of the whole PWM control unit is shown. In a fifth section, the

experimental results obtained from the manufactured demonstrator are analyzed. Finally, in a sixth and last section, the presented work is summarized and an outlook is given.

In battery powered mobile systems (e.g., cellular phones, digital cameras), the voltage provided by the battery decreases during its discharging, as it is shown in Fig. 1. To provide a constant voltage to the system electronic during the whole battery runtime, the battery voltage must be regulated by a DC-DC converter [1]. The basic step-down and step-up voltage conversion topologies are shown in Fig. 2 and Fig. 3, respectively.

To regulate the output voltage in the range of the voltage provided by the battery, the DC-DC converter must use a topology allowing both step-up and step-down voltage conversions, like the buck-boost topology shown in Fig. 4, which is a concatenation of the buck and the boost topologies shown in Fig. 2 and Fig. 3. However, the buck-boost topology generates more switching losses, because it requires two power switches to be switched during each PWM period t_{sw} , thus providing a lower conversion efficiency. Therefore, other topologies like the SEPIC and the zeta topologies which are using only one power switch were investigated [2], [3], [4]. Unfortunately, these topologies have other drawbacks. They require two power inductors (or one power inductor with two separate windings), which make them unpopular in compact mobile systems. Furthermore, since none of these two topologies are symmetrical, they are not well suited topologies for being used in a bi-directional DC-DC converter, because the charging and the discharging of the battery would need to be controlled by a different law, thus providing different performance, increasing the complexity of the control and therefore the costs of the DC-DC converter. The Ćuk topology is a symmetrical topology but it inverts the polarity of the provided output voltage [3].

The full-bridge topology shown in Fig. 5 is a fully symmetrical topology which provides a bi-directional conversion and does, therefore, not require different controls for the charging and discharging phase of a battery [5]. Depending on how

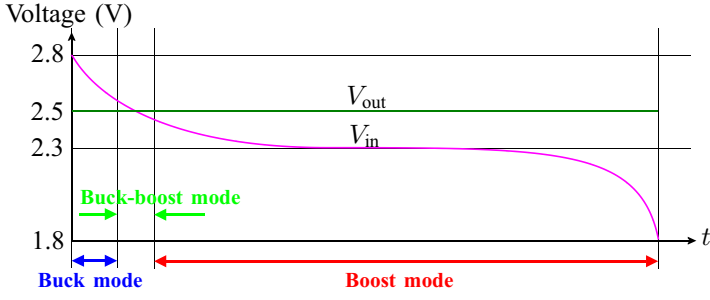


Fig. 1. Voltage characteristic of a discharging 2.3 V lithium-titanate battery.

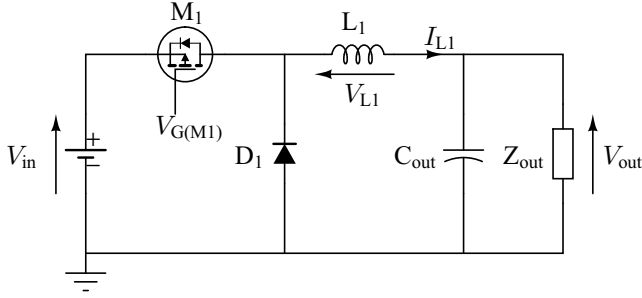


Fig. 2. Buck converter topology.

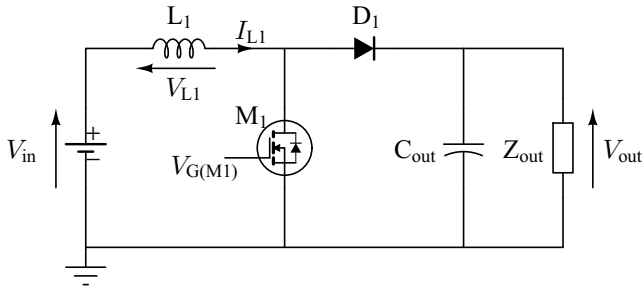


Fig. 3. Boost converter topology.

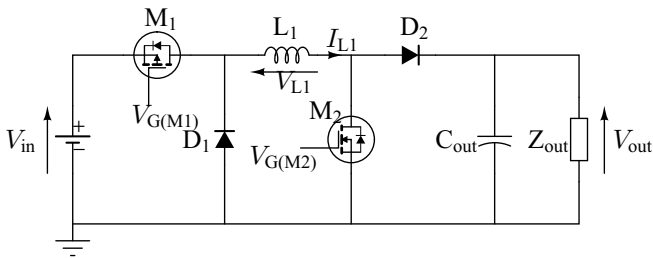


Fig. 4. Noninverting buck-boost converter topology.

the four power transistors are driven, as illustrated in Fig. 6, the full-bridge can be configured as a noninverting buck, buck-boost, or boost converter, thus minimizing the switching losses and providing a high efficiency. Additionally, the full-bridge requires only a single power inductor and a single filter capacitor, thus making it a well suited topology to be monolithic integrated in a CMOS DC-DC converter.

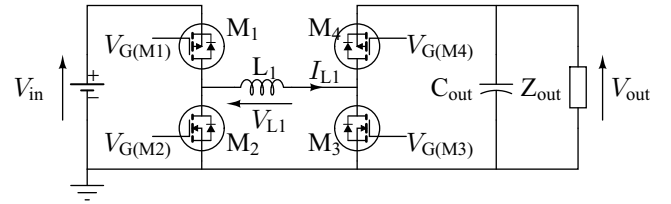


Fig. 5. Full-bridge converter topology.

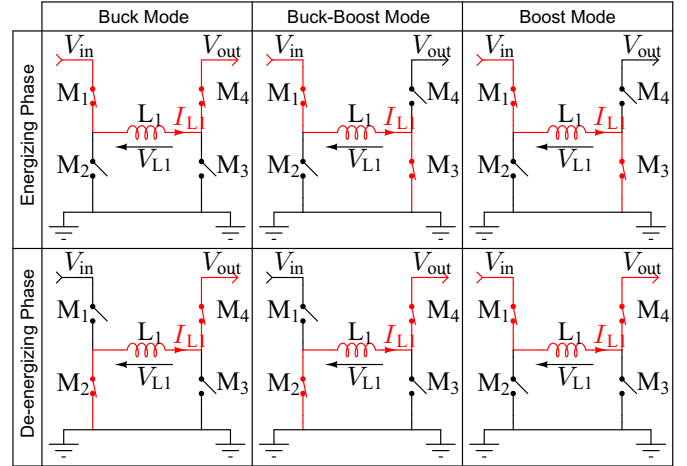


Fig. 6. Realization of the buck, noninverting buck-boost and boost modes with a full-bridge topology.

A typical voltage discharge characteristic of a battery is illustrated in Fig. 1. If the battery voltage V_{in} is higher than the desired regulated voltage V_{out} on the load side, the DC-DC converter operates in the buck mode (i.e., step-down voltage conversion). If the battery voltage V_{in} is lower than the regulated voltage V_{out} on the load side, the DC-DC converter operates in the boost mode (i.e., step-up voltage conversion). The following definitions are used in this paper:

$$\left\{ \begin{array}{l} M = \frac{V_{out}}{V_{in}} \\ f_{sw} = \frac{1}{t_{sw}} \\ t_{sw} = t_{on} + t_{off} \\ D = \frac{t_{on}}{t_{sw}} \end{array} \right. \quad (1)$$

where M is the voltage conversion ratio, f_{sw} the switching frequency of the PWM signal, t_{sw} the period of the PWM signal, t_{on} the time during which the energizing transistor is turned-on during one PWM period t_{sw} , t_{off} the time during which it is turned-off, D the duty cycle (expressed in %) of the PWM signal.

Due to the fact that the battery voltage decreases during discharge, it is possible that the control loop has to switch from buck mode to boost mode to maintain the output voltage level V_{out} above the input battery voltage V_{in} . If hard transitions between these two modes are used, the output voltage on the load side shows a step when the operating mode is commuted,

because the voltage conversion ratio is not continuous. A buck converter can reach a maximum voltage conversion ratio M_{buck} of 1:

$$M_{\text{buck}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{t_{\text{on}}}{t_{\text{sw}}} = D \quad (2)$$

A boost converter can reach a minimum voltage conversion ratio M_{boost} of 1:

$$M_{\text{boost}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{t_{\text{sw}}}{t_{\text{sw}} - t_{\text{on}}} = \frac{1}{1 - D} \quad (3)$$

However, since the generated PWM pulses turning-on and off the power switches cannot be infinitely narrow (i.e., t_{on} or t_{off} tending to 0), the values around 1 of the voltage conversion ratio M in the buck and boost modes are not practicable. To avoid the output voltage to drop in the full-bridge topology, a circuit providing smooth transitions between the buck mode and the boost mode must be used when the modes are switched. The solution consists in adding a buck-boost transition mode that is able to cover both buck and boost regions (i.e., $0 \leq M \leq 1$ and $M \geq 1$). The transfer function of the noninverting buck-boost converter shown in Fig. 4 is:

$$M_{\text{buck-boost}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{t_{\text{on}}}{t_{\text{sw}} - t_{\text{on}}} = \frac{D}{1 - D} \quad (4)$$

Fig. 7 shows the transfer functions of the common buck, buck-boost and boost converters presented in Fig. 2, Fig. 3 and Fig. 4 in continuous conduction mode (CCM).

II. OPERATING PRINCIPLE

Several methods for controlling buck and boost modes in DC-DC converters based on a full-bridge topology are described in the literature [6], [7], [8], [9], [10]. In 2005, B. Sahu *et al.* [11] have presented a control method which was based on smooth transitions between buck and boost mode. However, no analytical study of the proposed control method was presented. Simulation results in the case of an unidirectional DC-DC converter were provided but no experimental results were available. Further on, they have implemented a pulse-frequency modulation (PFM) mode additionally to the PWM mode [11], [12], [13], for increasing the light-load conversion efficiency [14]. Indeed, the PWM/PFM mode selection is done manually, because no load-current sensing circuit was available. For the PWM control circuit proposed in the following, an average inductor-current sensing circuit was developed and presented in [15]. This average inductor-current sensing circuit can be added to detect the load current at which the PWM/PFM modes must be switched.

Since the same control principle is used in both conversion directions, the silicon area can be optimized. Therefore, to simplify the description of the operating principle of the continuous control loop presented hereafter, only the direction when the battery is supplying the load is considered.

The basic idea behind the method of providing buck and boost mode regulation in a full-bridge converter topology consists in combining two PWM converters (i.e., a buck and a boost converter), as shown in Fig. 8. With this combination, the duty cycle D of both buck and boost converters can be controlled by a single internal control voltage V_{CI} , limited

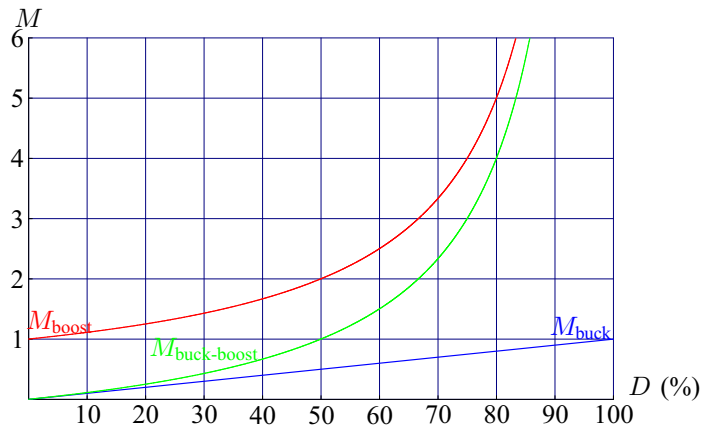


Fig. 7. Buck, noninverting buck-boost, and boost mode transfer functions in continuous conduction mode (CCM).

to $V_{\text{D(lim)}}$ so that unlimited energizing of the inductor L_1 is avoided in boost mode. Theoretically, both converters can be juxtaposed so that V_2 is equal to V_3 . However, in practice, it is mandatory to have an overlap between buck and boost regions, which means that V_2 is lower than V_3 , so that a third operating mode called *special buck-boost mode* is obtained. This overlap is a necessity because of the design implementation (e.g., offset of the CMOS comparator). A gap between the buck and the boost regions would result in a discontinuity in the regulation of the output voltage and would lead to instability.

The combination with overlapping of a buck and a boost converter, both driven by a common control voltage V_{CI} , provides buck, buck-boost and boost regulation, depending on the input voltage V_{in} on the battery side and the requested output voltage V_{out} on the load side. When the battery voltage is approximately the same as the desired load voltage, the converter operates in the special buck-boost mode. This mode has the same basic function as the buck-boost converter presented in Fig. 4, but does not have the same transfer function (this is analyzed hereafter). In practice, the special buck-boost mode could cover the whole output voltage range, but all four power transistors of the full-bridge must be switched during each cycle in this operating mode. Since the buck and boost modes only switch two of the four power transistors, these modes provide less switching losses and, therefore, a higher efficiency. To provide the highest overall efficiency, the range of operation in the special buck-boost mode must be kept to a minimum.

The V_{CI} voltage is a control voltage generated internally by the DC-DC converter on the base of the output voltage provided by the error amplifier shown on the complete PWM regulator schematic depicted later in Fig. 17, and analyzed in detail at the transistor's level in Section IV. The V_{CI} voltage is an integrated value of the feedback voltage V_{FB} . On one hand, the V_{CI} voltage increases when the V_{out} voltage on the load side is lower than the requested load voltage value. On the other hand, the V_{CI} voltage decreases when the V_{out} voltage on the load side is higher than the requested load voltage value. Two methods for implementing the combination of buck, buck-boost and boost regulation are described in the following.

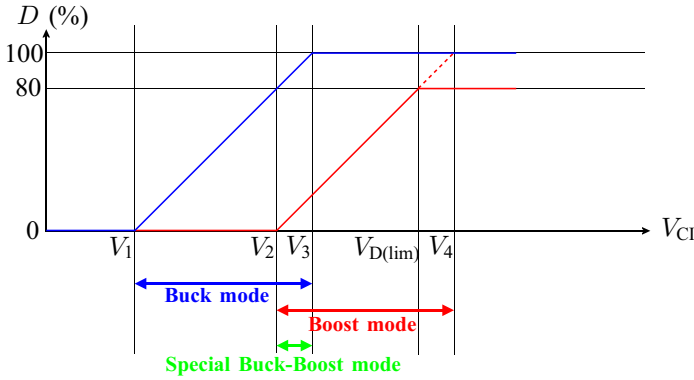


Fig. 8. Overlapping assembly of a buck and a boost converter, with duty cycle limitation of the boost converter to 80%.

A. State-of-the-Art of Continuous Control Loop

The first known implementation of smooth conversion mode transitions over buck, buck-boost, and boost modes came from the American ICs manufacturer Linear Technology [6], [7] in 2001 with its LTC3440, a commercial DC-DC converter [16]. This state-of-the-art solution consists of the combination of a buck and a boost converter, as shown in Fig. 9. This unidirectional converter topology, however, has some drawbacks. Since it uses two different sawtooth signals V_{osc1} and V_{osc2} , it requires an additional output phasing circuit which makes the circuit complex, thus more die area is consumed and the converter efficiency is reduced by wasting additional power through switching signals.

The operating principle of state-of-the-art solutions consists generally of a sawtooth oscillator that generates the carrier for the two PWM comparators COMP1 and COMP2. The voltage shifter on the buck side is connected to the noninverting input of COMP1. It adds a negative voltage shift to the sawtooth waveform generated by the oscillator, thus providing the V_{osc1} signal which switches between V_1 and V_3 (see Fig. 8 and Fig. 9). The voltage shifter on the boost side is connected to the inverting input of COMP2. It adds a positive voltage shift to the sawtooth waveform generated by the oscillator, thus providing the V_{osc2} signal which is switching between V_2 and V_4 . The control voltage V_{CI} is clamped to $V_{D(lim)}$ to limit the maximum duty cycle of the boost PWM comparator COMP2, as illustrated previously in Fig. 8. The BUCK and BOOST signals are digital outputs, which are used to control the digital level shifters [17] that are driving the power transistors M_1, M_2, M_3, M_4 shown in Fig. 5. These digital signals are processed in the PWM logic unit by adding dead-times to avoid crossconduction between M_1, M_2 , and between M_3, M_4 . All these signals are shown in the timing diagram plotted in Fig. 10. Gate drivers are located in the PWM logic unit for driving the power transistors M_1, M_2, M_3, M_4 . The BUCK and BOOST digital signals shown in Fig. 10 are processed by the PWM logic unit shown in Fig. 9. The resulting driver signals DRV_1, DRV_2, DRV_3 and DRV_4 drive the gates of the power transistors M_1, M_2 , and M_3, M_4 , respectively (see Fig. 5).

When the BUCK signal provides a logic 0, the transistor M_1 (PMOS) is switched on and the transistor M_2 (NMOS) is

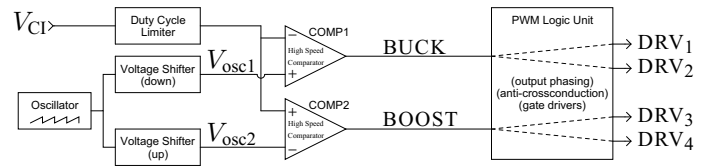


Fig. 9. Implementation of state-of-the-art continuous control loop in the LTC3440.

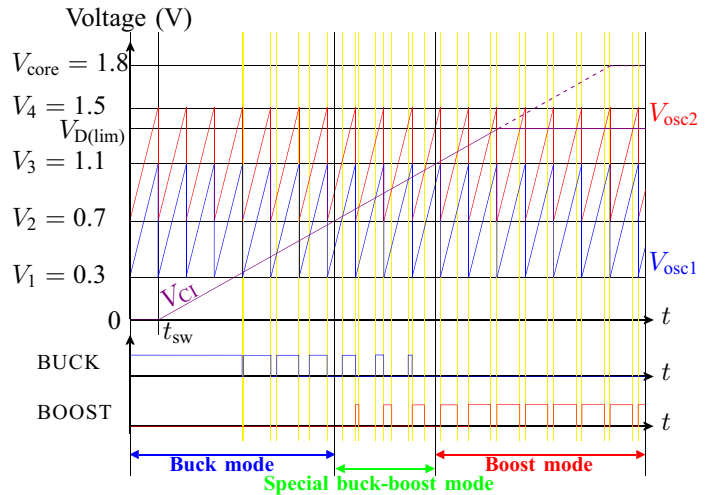


Fig. 10. Buck, boost and special buck-boost modes timing diagram in state-of-the-art full-bridge DC-DC converters. The control voltage V_{CI} is taken arbitrarily to show the transition between the different modes.

switched off. When the BUCK signal provides a logic 1, the transistors M_1 and M_2 behave the other way around. When the BOOST signal provides a logic 0, the transistor M_4 (PMOS) is switched on and the transistor M_3 (NMOS) is switched off. When the BOOST signal provides a logic 1, the transistors M_4 and M_3 behave the other way around. The control voltage V_{CI} is clamped to $V_{D(lim)}$, which is typically 75-95% of the maximum V_{osc2} voltage value. This limits the maximum duty cycle of the boost mode to 75-95% and avoids the unlimited energizing of the inductor L_1 through the turned on power transistors M_1 and M_3 , which would result in a failure by overcurrent (see Fig. 5).

For high frequency bi-directional DC-DC converters with synchronous rectification [18], however, this state-of-the-art control method is not well suited, because of the difficulty to control the dead-times (i.e., output phasing) when the converter is operating in the special buck-boost mode. In this operating mode, as shown in Fig. 10, the falling edge of a BUCK pulse and the rising edge of a BOOST pulse can clash and turn on simultaneously the transistors M_2 and M_3 , thus dissipating thermally a part of the energy stored in L_1 and, therefore, lowering the conversion efficiency. Adding a delay to the BOOST signal can be used to resolve this issue, however a more efficient solution was developed and is presented hereafter.

B. Novel Bi-directional PWM Control Circuit

For designing a DC-DC converter supporting bi-directional energy flows, a fully novel control method was developed. The proposed DC-DC converter implements a PWM buck and a PWM boost converter, which are both driven by a single oscillator. Fig. 11 shows the electrical block diagram of the combination of the buck and boost converters.

Unlike state-of-the-art solutions which uses two sawtooth carriers, a single symmetrical triangular carrier is generated by the oscillator, in the novel proposed PWM control circuit. This provides slower edges and, therefore, lower EMI at high switching frequencies [19], [20], [21]. A single high frequency symmetrical triangular carrier generates less noise than two shifted sawtooth carriers. When an on-chip power inductor is used, the bi-directional DC-DC converter must be able to operate at frequencies as high as 10 MHz.

The symmetrical triangular carrier is directly used by the two PWM comparators, COMP1 and COMP2, as shown in Fig. 11. Unlike state-of-the-art solutions, the novel control circuit performs no voltage shifting on this high frequency switching signal. Therefore, no high speed voltage shifters are needed and less power is consumed. It is the low frequency control voltage V_{CI} that is shifted up for the buck converter, and shifted down for the boost converter. The shifted up control voltage becomes V_{CI1} . The shifted down control voltage is additionally clamped, before becoming V_{CI2} . This clamping provides the boost mode duty cycle limitation. The advantage of this clamping method is that it is accurately done by the addition of only one transistor in the schematic design (see Section IV). The BUCK and BOOST digital signals drive the same circuit as these of state-of-the-art block diagram in Fig. 9. No gate drivers for the power transistors are considered here.

The reason of the presence of the inverter in Fig. 11 is explained by the properties of the high speed comparators COMP1 and COMP2. Due to their topology, these comparators have a noisy and a quiet input. The noisy input is non-inverting, while the quiet input is inverting. Both comparators get the same symmetrical triangular carrier on their noisy input. The quiet inputs are connected to the shifted control signals V_{CI1} and V_{CI2} , which are, therefore, not perturbed by the switching of the outputs of the comparators. The reason why it has been decided to shift both V_{CI1} and V_{CI2} remains from the CMOS implementation. Both control voltages are isolated from each other, and a perturbation on one has no effect on the other one. Additionally, when the triangular carrier gets a glitch due to the switching of the output of one of the high speed comparators, the other comparator sees exactly the same perturbation, thus ensuring that both comparators always use exactly the same carrier.

Fig. 12 shows the timing diagram of the novel PWM control circuit. As explained, the control voltage V_{CI} is not used directly by the high speed comparators. Only the shifted control voltages V_{CI1} and V_{CI2} are used by the comparators. Since V_{CI} is shifted upwards to become V_{CI1} and downwards to become V_{CI2} , V_{CI1} is always above V_{CI2} . When V_{CI2} is lower than V_1 , the converter runs in buck mode. When simultaneously V_{CI1} is above V_1 and V_{CI2} below V_2 , the converter runs in the

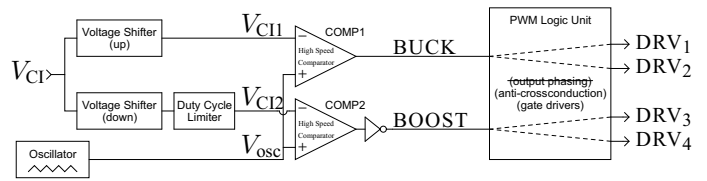


Fig. 11. Implementation of the novel continuous control loop.

special buck-boost mode. When V_{CI1} is above V_2 , the converter runs in boost mode. The timing diagram shown in Fig. 12 also illustrates the V_{CI2} clamping to $V_{D(lim)}$, thus limiting the maximum duty cycle of the BOOST signal.

When comparing the timing diagram of the novel PWM control circuit (see Fig. 12) and the timing diagram of the state-of-the-art PWM control circuit (see Fig. 10), a significant functional difference appears in the special buck-boost mode region. With sawtooth carriers, there is simultaneously a falling edge on the BUCK signal and a rising edge on BOOST signal, as illustrated in the timing diagram in Fig. 10. This introduces a timing violation, because two edges never occur simultaneously in practice. In worst case, the BUCK signal still provides a logic 1 when the BOOST signal has provided the rising edge. This turns on both NMOS M_2 and M_3 simultaneously in Fig. 5 (M_1 and M_4 are turned off). The consequence is lost power, because the inductor is de-energized in a ground loop (i.e., the inductor current flows through M_2 , L_1 , M_3). By using a symmetrical triangular carrier like it is done in the proposed PWM control circuit and illustrated in Fig. 12, this timing violation phenomenon is avoided, because the logic 1 pulses (i.e., the pulses at which the NMOS M_2 and M_3 are turned on) of both BUCK and BOOST signals are centered and cannot overlap themselves, providing always the longest possible blanking time between a BUCK pulse and a BOOST pulse. For this reason, no output phasing circuit is needed in this novel control method.

Further on, by the control method used in state-of-the-art solutions (see Fig. 9 and Fig. 10), when a sawtooth carrier is used in place of a triangular carrier, and especially when it is additionally shifted up and down, both shifted carriers are not absolutely identical (i.e., in phase and in distortion). A skew is then inevitably introduced between the V_{osc1} and the V_{osc2} signals. Therefore, an additional delay control circuit must be added to the PWM logic unit to control the phasing between the BUCK and the BOOST signals. This makes the PWM logic unit more complex. In the novel proposed control circuit, this phasing is automatically controlled since the logic 1 pulses on BUCK and on BOOST are automatically centered by using a unique triangular carrier (see Fig. 11 and Fig. 12). No skew is introduced on the carrier, since the same carrier signal is used with both comparators COMP1 and COMP2. The pulses are automatically centered when using a symmetrical triangular carrier. Additionally, by separating and centering the pulses on the BUCK and BOOST signals, the current peaks created by the gate drivers (due to gate capacitance charging/discharging and shortcut current in the inverters used in the gate drivers) are spaced and their amplitudes are reduced since the internal

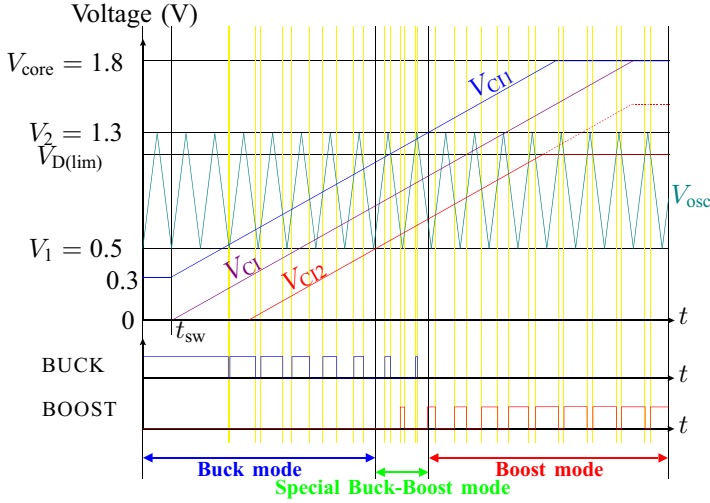


Fig. 12. Buck, boost and special buck-boost modes timing diagram for the proposed PWM control circuit. The control voltage V_{CI} is taken arbitrarily to show the transition between the different modes.

decoupling capacitors connected between the supply rails have more time to recharge themselves (the time separating two falling edges on BUCK and BOOST signals is the longest possible in Fig. 12).

III. MATHEMATICAL ANALYSIS OF THE TRANSFER FUNCTION

The voltage conversion factor M is the ratio of the output load voltage V_{out} divided by the input battery voltage V_{in} . It is only a function of the duty cycle D of the PWM signal when the converter is operating in the continuous conduction mode (CCM). The converter can be considered operating always in CCM since the inductor current can reverse at light loads when synchronous rectification is used. When the full-bridge performs voltage step-down conversion like a buck converter, the relation between V_{in} and V_{out} in a buck converter is given in Eq. (2). When the full-bridge performs voltage step-up conversion like a boost converter, the relation between V_{in} and V_{out} in a buck converter is given in Eq. (3). When the full-bridge has to supply a load voltage V_{out} which is close to the battery voltage V_{in} , the special buck-boost mode is entered. However, the special buck-boost mode resulting from the combination of the buck and the boost converters using the novel PWM control circuit does not provide a complete overlapping range between the buck and the boost converters. Therefore, when the DC-DC converter is performing in the special buck-boost mode, the logic 1 pulses generated by the comparators COMP1 and COMP2 are not complementary over one period t_{sw} . For example, when both M_1 and M_3 are turned off, M_2 and M_4 are not necessarily both turned on, as it would be the case in a typical buck-boost converter. This phenomenon is shown in Fig. 13 and is analyzed from the mathematical point of view hereafter.

To calculate the transfer function of the special buck-boost mode, the following hypotheses are considered (refer to Fig. 13):

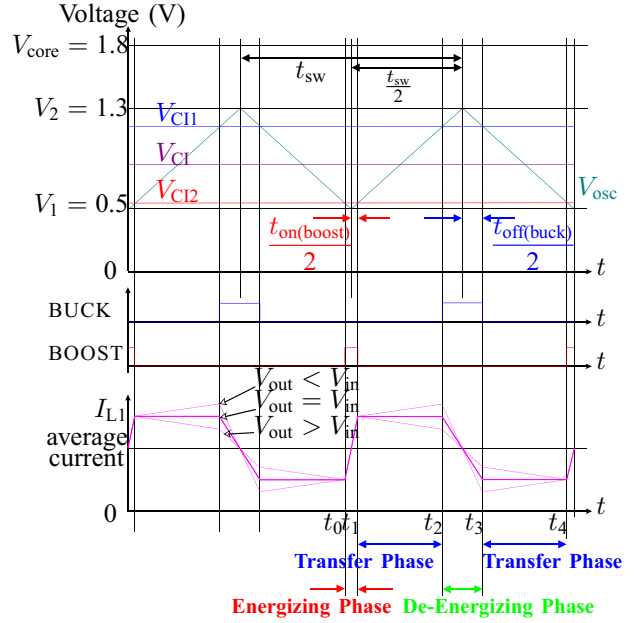


Fig. 13. Special buck-boost mode running in steady-state. The three different inductor current waveforms I_{L1} are only given as overview. They are not scaled on each other.

- The input voltage (V_{in}) is supposed to be constant over one period t_{sw} .
- The converter is operating in steady-state. The control voltages (V_{CI} , V_{CI1} , and V_{CI2}) are constant over one period t_{sw} .
- The output capacitor C_{out} filters out the voltage ripple. The small ripple approximation [3] allows to consider the output voltage (V_{out}) as constant over one period t_{sw} .
- The inductor current $I_{L1}(t)$ is continuous and periodic in steady-state. It satisfies the equation:

$$I_{L1}(t) = I_{L1}(t_{sw} + t) \quad (5)$$

- The shift voltage V_{shift1} is added to the control voltage V_{CI} to become V_{CI1} , while the shift voltage V_{shift2} is subtracted from V_{CI} to become V_{CI2} . These shift voltages are not necessarily equal, but they are both supposed to be positive.

$$V_{CI1} = V_{CI} + V_{shift1} \quad (6)$$

$$V_{CI2} = V_{CI} - V_{shift2} \quad (7)$$

- The converter provides a buck-boost region (i.e., region where buck and boost overlap) and is operating in the special buck-boost mode. This implies that the:

$$0 < V_1 < V_{CI2} < V_{CI} < V_{CI1} < V_2 < V_{core} \quad (8)$$

$$V_{shift1} + V_{shift2} < V_2 - V_1 \quad (9)$$

- The timings t_1 , t_2 , t_3 , t_4 in Fig. 13 are defined as follow:

$$\begin{cases} t_1 - t_0 = t_{on(boost)} \\ t_2 - t_1 = \frac{t_{sw}}{2} - \frac{t_{on(boost)}}{2} - \frac{t_{off(buck)}}{2} \\ t_3 - t_2 = t_{off(buck)} \\ t_4 - t_3 = \frac{t_{sw}}{2} - \frac{t_{on(boost)}}{2} - \frac{t_{off(buck)}}{2} \end{cases} \quad (10)$$

The signal waveforms used to calculate the transfer function of the special buck-boost mode are shown in Fig. 13. By considering the time interval t_0 to t_4 (i.e., one complete oscillator period t_{sw}), three schematic configurations occur. These configurations are shown in Fig. 14. The time interval t_0 to t_1 corresponds to the *energizing phase* in a basic boost converter. The inductor is connected between the input voltage V_{in} and ground, therefore its current I_{L1} increases. The time interval t_1 to t_2 corresponds to the energizing phase in a basic buck converter if the output voltage V_{out} is lower than the input voltage V_{in} . It corresponds to the de-energizing phase of a basic boost converter if the output voltage V_{out} is higher than the input voltage V_{in} (see Fig. 6). This period subinterval is hereafter simply called *transfer phase*. The configuration of the switches in an energizing buck and in a de-energizing boost is the same. The only difference is that if V_{out} is lower than V_{in} , the inductor current I_{L1} increases, and if V_{out} is higher than V_{in} , the inductor current I_{L1} decreases. The time interval t_2 to t_3 corresponds to the *de-energizing phase* of a buck converter. During this phase, the inductor current I_{L1} decreases. The time interval t_3 to t_4 corresponds to the same configuration as the time interval t_1 to t_2 .

Since the inductor current I_{L1} is continuous, the following equations are obtained:

- from t_0 to t_1 , the current variation in the inductor is expressed by:

$$\begin{aligned} \Delta I_{L1}(t_0, t_1) &= \frac{1}{L_1} \cdot \int_{t_0}^{t_1} (V_{L1} \cdot dt) \\ &= \frac{1}{L_1} \cdot V_{in} \cdot (t_1 - t_0) \end{aligned} \quad (11)$$

- from t_1 to t_2 , the current variation in the inductor is expressed by:

$$\begin{aligned} \Delta I_{L1}(t_1, t_2) &= \frac{1}{L_1} \cdot \int_{t_1}^{t_2} (V_{L1} \cdot dt) \\ &= \frac{1}{L_1} \cdot (V_{in} - V_{out}) \cdot (t_2 - t_1) \end{aligned} \quad (12)$$

- from t_2 to t_3 , the current variation in the inductor is expressed by:

$$\begin{aligned} \Delta I_{L1}(t_2, t_3) &= \frac{1}{L_1} \cdot \int_{t_2}^{t_3} (V_{L1} \cdot dt) \\ &= \frac{1}{L_1} \cdot (-V_{out}) \cdot (t_3 - t_2) \end{aligned} \quad (13)$$

- from t_3 to t_4 , the current variation in the inductor is expressed by:

$$\begin{aligned} \Delta I_{L1}(t_3, t_4) &= \frac{1}{L_1} \cdot \int_{t_3}^{t_4} (V_{L1} \cdot dt) \\ &= \frac{1}{L_1} \cdot (V_{in} - V_{out}) \cdot (t_4 - t_3) \end{aligned} \quad (14)$$

In steady-state operation, the inductor current $I_{L1}(t)$ is equal to $I_{L1}(t_{sw} + t)$, where t_{sw} is the period of the oscillator. Therefore,

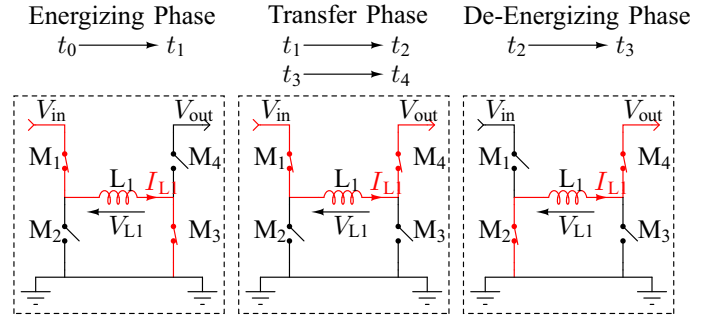


Fig. 14. Successive switches configuration in the special buck-boost mode.

the following equation is satisfied:

$$\begin{aligned} \Delta I_{L1}(t_0, t_1) + \Delta I_{L1}(t_1, t_2) + \Delta I_{L1}(t_2, t_3) + \\ \Delta I_{L1}(t_3, t_4) = 0 \end{aligned} \quad (15)$$

By developing Eq. (15), it is obtained:

$$V_{in} \cdot ((t_1 - t_0) + (t_4 - t_3)) = V_{out} \cdot ((t_2 - t_1) + (t_3 - t_2)) \quad (16)$$

Applying the definitions given in Eq. (10) to Eq. (16) gives:

$$V_{in} \cdot (t_{sw} - t_{off(buck)}) - V_{out} \cdot (t_{sw} - t_{on(boost)}) = 0 \quad (17)$$

By arranging Eq. (17), the transfer function of the special buck-boost mode is:

$$M'_{buck-boost} = \frac{V_{out}}{V_{in}} = \frac{t_{sw} - t_{off(buck)}}{t_{sw} - t_{on(boost)}} \quad (18)$$

The time intervals $[t_1, t_2]$ and $[t_3, t_4]$ shown in Fig. 13 when the special buck-boost mode is running can be expressed as:

$$(t_2 - t_1) = (t_4 - t_3) = \frac{t_{sw}}{2} - \frac{t_{on(boost)}}{2} - \frac{t_{off(buck)}}{2} \quad (19)$$

The time intervals $(t_2 - t_1)$ and $(t_4 - t_3)$ expressed in Eq. (19) are linked to the voltages $V_1, V_2, V_{shift1}, V_{shift2}$ in the following manner:

$$\left(\frac{t_{sw}}{2} - \frac{t_{on(boost)}}{2} - \frac{t_{off(buck)}}{2} \right) \cdot \frac{V_2 - V_1}{2} = V_{shift1} + V_{shift2} \quad (20)$$

By reordering Eq. (20), it is obtained:

$$\frac{t_{sw} - t_{on(boost)} - t_{off(buck)}}{t_{sw}} = \frac{V_{shift1} + V_{shift2}}{V_2 - V_1} \quad (21)$$

Eq. (21) shows that if the pulses (i.e., logic 1) on the digital BUCK output become wider, the pulses (i.e., logic 1) on the digital BOOST output become narrower from the same amount of time (i.e., only $t_{on(boost)}$ and $t_{off(buck)}$ are not fixed by design). Therefore, the time during which both BUCK and BOOST signals are low remains constant. This means that the time intervals $[t_1, t_2]$ and $[t_3, t_4]$ shown in Fig. 13 are independent of the control voltage V_{C1} when the special buck-boost mode is

running. Additionally, like the way used for obtaining Eq. (21), $t_{\text{on(boost)}}$ and $t_{\text{off(buck)}}$ can be written as:

$$\frac{V_2 - V_1}{\frac{t_{\text{sw}}}{2}} \cdot \frac{t_{\text{on(boost)}}}{2} = V_{\text{CI}2} - V_1 \implies \frac{t_{\text{on(boost)}}}{t_{\text{sw}}} = \frac{V_{\text{CI}2} - V_1}{V_2 - V_1} \quad (22)$$

$$\frac{V_2 - V_1}{\frac{t_{\text{sw}}}{2}} \cdot \frac{t_{\text{off(buck)}}}{2} = V_2 - V_{\text{CI}1} \implies \frac{t_{\text{off(buck)}}}{t_{\text{sw}}} = \frac{V_2 - V_{\text{CI}1}}{V_2 - V_1} \quad (23)$$

By using Eq. (2), the transfer function of the buck mode can also be written as a function of the control voltage V_{CI} :

$$M_{\text{buck}} = \frac{t_{\text{sw}} - t_{\text{off(buck)}}}{t_{\text{sw}}} = \frac{V_{\text{shift}1} + V_{\text{CI}} - V_1}{V_2 - V_1} \quad (24)$$

By using Eq. (3), the transfer function of the boost mode can also be written as a function of the control voltage V_{CI} :

$$M_{\text{boost}} = \frac{t_{\text{sw}}}{t_{\text{sw}} - t_{\text{on(boost)}}} = \frac{V_2 - V_1}{V_{\text{shift}2} - V_{\text{CI}} + V_2} \quad (25)$$

The special buck-boost mode transfer function from Eq. (18) can then also be written as a function of the internal control voltage V_{CI} :

$$M'_{\text{buck-boost}} = M_{\text{buck}} \cdot M_{\text{boost}} = \frac{V_{\text{shift}1} + V_{\text{CI}} - V_1}{V_{\text{shift}2} - V_{\text{CI}} + V_2} \quad (26)$$

Eq. (24), Eq. (25), and Eq. (26) are only valid when the control voltage V_{CI} is in the corresponding interval, as listed in Table I. The buck, buck-boost, and boost mode transfer functions M are plotted over the control voltage V_{CI} in Fig. 15.

The transfer function M of the bi-directional DC-DC converter is made continuous over the three operating modes by defining the transition points A_1 , A_2 and B as shown in Fig. 15. The location of these points is set up by $V_{\text{shift}1}$ and $V_{\text{shift}2}$. Their coordinates are obtained by solving Eq. (27) for V_{CI} at the points A_1 and A_2 (i.e., intersections between the buck-boost and the buck curve) and Eq. (28) at the point B (i.e., intersection between the buck-boost and the boost curve):

$$\exists V_{\text{CI}} = V_{A1} \in \mathbb{R} \text{ and } \exists V_{\text{CI}} = V_{A2} \in \mathbb{R}, \quad M'_{\text{buck-boost}}(V_{\text{CI}}) = M_{\text{buck}}(V_{\text{CI}}) \quad (27)$$

$$\exists V_{\text{CI}} = V_B \in \mathbb{R}, \quad M'_{\text{buck-boost}}(V_{\text{CI}}) = M_{\text{boost}}(V_{\text{CI}}) \quad (28)$$

The abscissas V_{A1} and V_{A2} of the intersection points A_1 and A_2 between the buck-boost and the buck curves are obtained by solving:

$$M'_{\text{buck-boost}} = M_{\text{buck}} \quad (29)$$

$$\implies \frac{V_{\text{shift}1} + V_{\text{CI}} - V_1}{V_{\text{shift}2} - V_{\text{CI}} + V_2} = \frac{V_{\text{shift}1} + V_{\text{CI}} - V_1}{V_2 - V_1} \quad (30)$$

$$\implies V_{\text{CI}} = \begin{cases} V_{A1} = V_1 - V_{\text{shift}1} \\ V_{A2} = V_1 + V_{\text{shift}2} \end{cases} \quad (31)$$

The two mathematical solutions obtained in Eq. (31) must be verified to be valid for the supposed operating range. The

TABLE I
OPERATING MODES WITH THEIR CORRESPONDING V_{CI} CONTROL VOLTAGE RANGES.

Op. Mode	$V_{\text{CI}1}$	$V_{\text{CI}2}$	V_{CI}
Buck	$V_{\text{CI}1} \geq V_1$	$V_{\text{CI}2} < V_1$	$V_{\text{CI}} \in [V_1 - V_{\text{shift}1}, V_1 + V_{\text{shift}2}]$
Buck-Boost	$V_{\text{CI}1} \leq V_2$	$V_{\text{CI}2} \geq V_1$	$V_{\text{CI}} \in [V_1 + V_{\text{shift}2}, V_2 - V_{\text{shift}1}]$
Boost	$V_{\text{CI}1} > V_2$	$V_{\text{CI}2} < V_2$	$V_{\text{CI}} \in [V_2 - V_{\text{shift}1}, V_2 + V_{\text{shift}2}]$

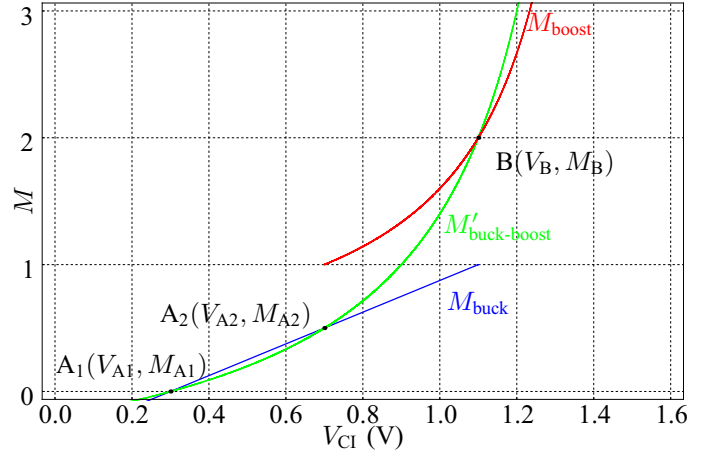


Fig. 15. Example of the buck, boost and special buck-boost transfer functions in the novel PWM control circuit with $V_{\text{shift}1} = V_{\text{shift}2} = 200$ mV.

control voltage V_{CI} is varying between V_1 and V_2 , therefore both following relations are obtained:

$$V_1 < V_1 - V_{\text{shift}1} < V_2 \implies 0 < -V_{\text{shift}1} < V_2 - V_1 \quad (32)$$

$$V_1 < V_1 + V_{\text{shift}2} < V_2 \implies 0 < +V_{\text{shift}2} < V_2 - V_1 \quad (33)$$

Eq. (32), however, is not verified since both $V_{\text{shift}1}$ and $V_{\text{shift}2}$ are supposed to be positive. Therefore, the transition between the buck and the buck-boost modes is obtained the point A_2 at a control voltage V_{CI} equal to $V_1 + V_{\text{shift}2}$.

By solving Eq. (28), the abscise V_B of the intersection point B (refer to Fig. 15) between the buck-boost and the boost curves is given by:

$$M'_{\text{buck-boost}} = M_{\text{boost}} \quad (34)$$

$$\implies \frac{V_{\text{shift}1} + V_{\text{CI}} - V_1}{V_{\text{shift}2} - V_{\text{CI}} + V_2} = \frac{V_2 - V_1}{V_{\text{shift}2} - V_{\text{CI}} + V_2} \quad (35)$$

$$\implies V_{\text{CI}} = V_B = V_2 - V_{\text{shift}1} \quad (36)$$

The transition between the buck-boost and the boost modes is obtained at a control voltage V_{CI} equal to $V_2 - V_{\text{shift}1}$.

Mathematically, it is interesting to notice that if $V_{\text{shift}1}$ and $V_{\text{shift}2}$ are taken equal, the following relation is verified:

$$M'_{\text{buck-boost}}(V_{\text{CI}}) = 1 \implies V_{\text{CI}} = \frac{V_1 + V_2}{2} \quad (37)$$

The PWM control circuit makes the DC-DC converter operating in the buck mode when the control voltage V_{CI} is below V_{A2} . Further, it makes it operating in the buck-boost mode when V_{CI} is comprised between V_{A2} and V_B . Finally, it makes it operating in the boost mode when V_{CI} is above V_B . This can be graphically observed in Fig. 13 and Fig. 16.

The values of the parameters used for designing the bi-directional DC-DC converter are listed in Tab. II. The complete transfer function M of the bi-directional DC-DC converter is shown in Fig. 16. The junction points A_2 and B between the buck, buck-boost, and boost curves were determined by the method exposed previously.

Thanks to the symmetrical triangular waveform oscillator, this newly developed PWM control circuit provides the advantage of avoiding the simultaneous turn on of the NMOS M_2 and M_3 in Fig. 5 when the special buck-boost mode is used. The logic **1** pulses provided by the BUCK and BOOST signals are automatically centered, as shown in Fig. 12. The timing separating these logic pulses are very well controlled by the design voltage parameters V_1 , V_2 and V_{shift} . No additional logic is needed in the PWM logic unit shown in Fig. 11, thus simplifying the circuit design and improving the power efficiency of the full-bridge DC-DC converter.

IV. SCHEMATIC OF THE PWM CONTROL CIRCUIT

The pulse-width modulation unit presented in the schematic in Fig. 17 is the heart of the voltage regulation. It is composed of an error amplifier with the corresponding voltage compensated feedback loop providing the control signal V_{CI} for the voltage regulation, a dual voltage shifter limiting also the duty cycle in the boost conversion mode, a triangular waveform oscillator (not shown in Fig. 17) providing the carrier V_{osc} , and finally two high speed comparators generating the PWM signals BUCK and BOOST.

The overlapping of the buck and boost regions (refer to Fig. 8) is mandatory because of the fabrication process, which introduces mismatches between transistors in the layout. These mismatches produce offset voltages in the input stages of the high speed comparators, thus adding inaccurateness to the real area value of the crossover buck-boost region. In consequence, a precisely defined buck-boost region with an area reduced to zero cannot be ensured practically (i.e., this would lead practically to either a buck, boost and a small buck-boost region, or to two disjointed buck and boost regions). This means that it must be guaranteed by design that the overlapping of the buck and the boost region still exists after the manufacturing process. Further on, since the duty cycle in this crossover buck-boost region is high for the buck comparator and low for the boost comparator (see Fig. 11, Fig. 12 and Fig. 17), the width of the generated BUCK and BOOST pulses is a problem. Actually, it is practically possible to operate a buck converter with a duty cycle D equal to 100% (i.e., with the power transistor M_1 in the buck converter in Fig. 2 always turned on). It is almost impossible, however, to operate this same buck converter with a PWM frequency of 1 MHz at a duty cycle D of 99.999%, since the duration of the turn-off pulses delivered to the gate of the power transistor M_1 would be 0.1 ns. This means that, when defining the area of the overlapping buck-boost region shown in Fig. 8, the width of the simultaneous buck and boost pulses delivered in this region must be carefully analyzed so that they can be practically generated by the power MOSFET gate drivers, and be executed by the power transistor itself. If this is not

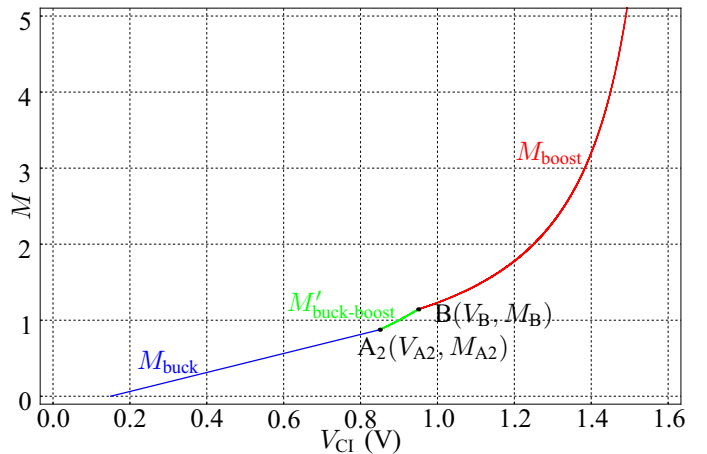


Fig. 16. Continuous transfer function of the novel proposed PWM control circuit with $V_{\text{shift1}} = V_{\text{shift2}} = 350$ mV.

TABLE II
PARAMETER VALUES OF THE DESIGNED PWM CONTROL CIRCUIT.

Parameter	Value
V_1	0.5 V
V_2	1.3 V
V_{shift}	0.350 V
V_{A2}	0.850 V
M_{A2}	0.875 V/V
V_B	0.950 V
M_B	1.143 V/V

done, the designed circuit may practically provide a buck-boost region, but its area will be too small and the width of the BUCK and BOOST pulses too narrow to make the power transistors switching.

In the PWM control scheme presented by B. Sahu *et al.* [11] and shown in Fig. 18, only one of the two control signals V_{CI1} and V_{CI2} shown in Fig. 17 is shifted. In other words, as shown in Fig. 18, the signal $V_{\text{EA(out)}}$ is directly connected to the noninverting input of the boost comparator (COMP2), while $V_{\text{EA(out)}}$ is shifted up and connected to the inverting input of the buck comparator (COMP1). The triangular waveform oscillator is therefore connected to the noninverting input of the buck comparator (COMP1) and to the inverting input of the boost comparator (COMP2). However, these high speed comparators have parasitic capacitive retroaction. Depending of their architecture, they couple the noise generated by their output to their inputs (the output noise of the VCDA architecture used as high speed comparator is mainly coupled to the noninverting input [22]). This means that when the output is switching, the inputs see a part of the generated switching noise. Thus, two major drawbacks appears in the design proposed by B. Sahu *et al.* [11] for its usage in high frequency DC-DC converters:

- The first drawback at high switching frequencies is due to the fact that the control voltage $V_{\text{EA(out)}}$ is directly provided to COMP2. When the output of COMP2 switches, it injects noise back into $V_{\text{EA(out)}}$. In the worst case, this noise is shifted up and transmitted to COMP1 through V_{CI1} . At high switching frequencies (i.e., at high dV/dt),

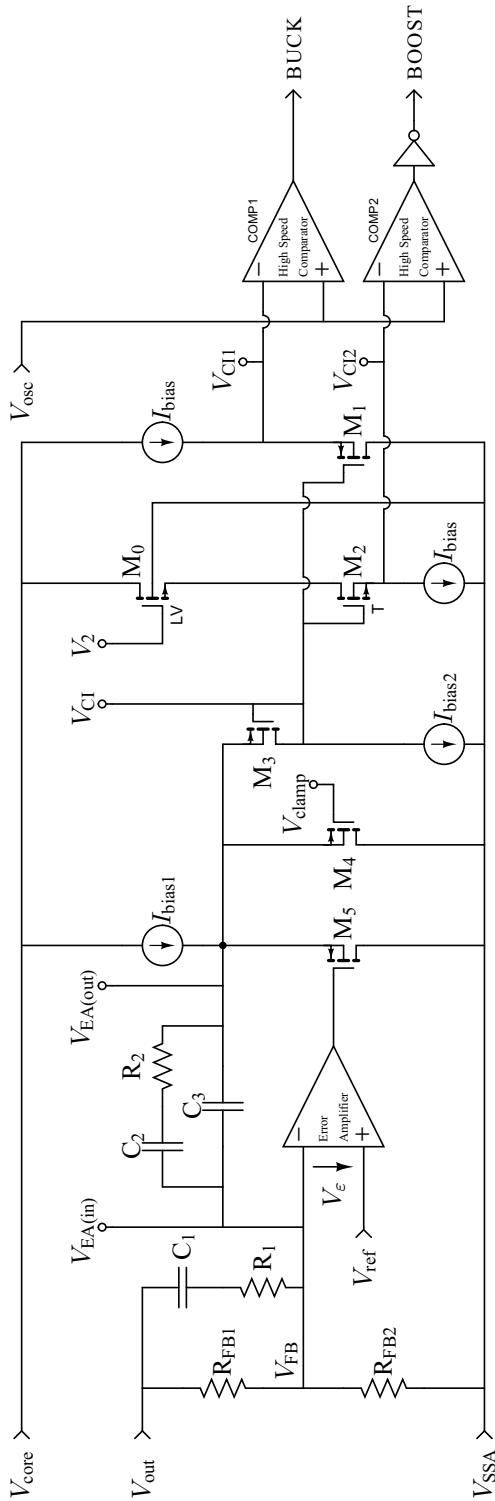


Fig. 17. Schematic of the complete PWM control circuit showing the continuous control loop. Note that the components in the feedback and compensation loop (R_{FB1} , R_{FB2} , R_1 , R_2 , C_1 , C_2 , C_3) are external discrete devices. LV stays for low- V_{th} transistors and T stays for substrate isolated NMOS transistors (i.e., NMOS in triple-well).

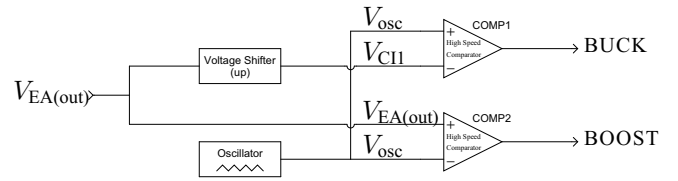


Fig. 18. Implementation of the continuous control loop by [11].

the injected noise amplitude can be sufficient to trigger the high speed comparator COMP1.

- The second drawback at high switching frequencies is that the control signals (i.e., issued from $V_{EA(out)}$) are connected to the inverting input of COMP1 and noninverting input of COMP2. Since the high speed comparators based on the VCDA architecture couple the generated output noise to the noninverting input, the design proposed by B. Sahu *et al.* [11] superposes noise to the control signal $V_{EA(out)}$ and to the oscillator waveform V_{osc} , thus increasing the inaccuracy by unmatched noise balancing.

Due to these drawbacks, the control scheme proposed by B. Sahu *et al.* [11] provides a too weak noise robustness at high switching frequencies and is therefore not well suited for an usage in high frequency PWM DC-DC converters (i.e., operating at PWM frequencies as high as 10 MHz [23]).

In the novel proposed high switching frequencies PWM control circuit, these drawbacks were avoided from the beginning. Therefore, both high speed comparators have their noisy input (i.e., noninverting input) connected to the oscillator signal V_{osc} (see Fig. 17). Hence, when one of the comparators is switching, the other comparator sees the same amount of noise at the V_{osc} side. The inverting side of the high speed comparators is nearly insensitive to the noise generated by the switching output. This configuration, however, requires an additional inverter to be connected to the output of COMP2 (see Fig. 17). Since the additional delay introduced by this inverter (i.e., 28.5 ps) is more than two orders of magnitude smaller than the comparison time (i.e., 10 ns) of the high speed comparators, it can be neglected and is, therefore, not a design issue.

Additionally, in the novel proposed PWM control circuit, two control signals V_{C11} and V_{C12} are generated by two voltage shifters (see Fig. 11 and Fig. 17). The principle of this voltage shifting is illustrated in Figure 19. There are mainly three advantages of this dual shifting method. The first advantage is that the same distortion is applied to both of the shifted control signals V_{C11} and V_{C12} , thus avoiding signal waveform mismatches (i.e., both signals have same bandwidth and same drive strength). The second advantage is that, due to the voltage shifting, the control signals V_{C11} and V_{C12} are essentially decoupled, thus avoiding noise to flow between V_{C11} and V_{C12} . In other words, no retroaction exists from V_{C11} or V_{C12} to V_{C1} , thus V_{C11} is independent of V_{C12} , and V_{C12} is independent of V_{C11} . Finally, the third advantage of this method is that the duty cycle D of the boost converter can be easily and precisely limited by using only one additional transistor.

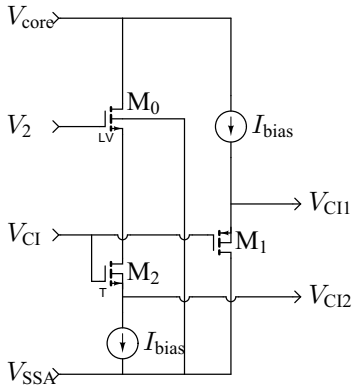


Fig. 19. Schematic of the voltage shifter and the duty cycle limiter. The transistor M_0 is a low- V_{th} (LV) NMOS and the transistor M_2 is an NMOS in a triple-well (T).

A. Error Amplifier

As shown in Fig. 17, the load voltage V_{out} is sensed and fed back through the V_{FB} voltage to the inverting input of the error amplifier. This feedback voltage V_{FB} is then compared to the internal reference voltage V_{ref} , which is connected to the noninverting input of the error amplifier. The voltage difference (i.e., the error voltage V_{ϵ}) is then amplified and integrated by the error amplifier, since its feedback loop — constituted of R_2 , C_2 , C_3 — is capacitive (i.e., there is no DC path). The transistors M_3 , M_4 , M_5 , and the current sources I_{bias1} , I_{bias2} have been implemented to allow the use of a soft-start circuit, which controls the V_{clamp} voltage. The soft-start circuit is not shown in Fig. 17, but it permits to adjust the startup speed (i.e., by limiting the amount of inrush current during startup).

The transient response of a DC-DC converter is a function of both small signal and large signal responses. The small signal response is determined by the compensation network of the error amplifier (i.e., R_2 , C_2 , C_3). The large signal response is a function of the gain, bandwidth and slew rate of the error amplifier, as well as the inductance L_1 of the power inductor and the capacity C_{out} of the output filter capacitor. The circuit of the error amplifier is a self-compensating topology based on the low-voltage complementary folded cascode operational amplifier proposed by R. Roewer *et al.* [24]. At a supply voltage of 1.8 V and with a 1 pF output load capacitor, the error amplifier provides a 50° phase margin at 6.7 MHz and consumes 45 μ W of power (i.e., 25 μ A of current).

The voltage feedback loop — constituted of R_{FB1} , R_{FB2} in Fig. 17 — must be compensated to provide stability margin, and to minimize the output voltage overshoot and undershoot response to line and load transients [25]. In the novel proposed PWM control circuit, a *Type III* error amplifier compensation network is used. It is constituted of the devices R_1 , R_2 , C_1 , C_2 , C_3 (see Fig. 17). This configuration has a pole at the origin and two zero-pole pairs, thus it can provide up to 180° of phase boost (in the literature, the used values for the phase margin ensuring the closed loop system is stable are in the interval [45°, 60°]). The method for calculating the values of the components in the compensation loop is not provided in this paper, but it can be easily found in the literature, since it

is a popular compensation scheme [3].

B. Voltage Shifter and Duty Cycle Limiter

The voltage shifting of the control voltage V_{Cl} is performed by a source follower (common drain) transistor configuration. Fig. 19 shows the schematic of the double voltage shifter used in the novel PWM control circuit. The PMOS M_1 is biased by a constant current source I_{bias} . The input voltage V_{Cl} is directly connected to the gate of M_1 (i.e., high impedance input). The output is the voltage V_{Cl1} provided at the source of M_1 . The principle of a source follower circuit consists in an output voltage provided at the source that follows the gate voltage at the input. The body effect of the transistor M_1 has been cancelled, since its bulk is directly connected to its source. This is possible since the UMC L180 technology is an n -well CMOS process. The transistor M_1 is driven in the saturation region. Therefore, when the channel-length modulation is neglected, the relation between the constant bias current I_{bias} and the input and output voltages is given by:

$$I_{bias} = \frac{1}{2} \cdot \mu_p \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_{M1} \cdot (V_{GS(M1)} - V_{th})^2 \quad (38)$$

where μ_p is the carrier mobility in p -type silicon, C_{ox} is the gate oxide capacitance per unit area, W is the channel width of the transistor, L is the channel length of the transistor, $V_{GS(M1)}$ is the gate-source voltage of the PMOS M_1 , and V_{th} is its threshold voltage. Since the bias current I_{bias} is constant, to satisfy Eq. (38), the voltage $V_{GS(M1)}$ must also remain constant because all other parameters are fixed by the technology (i.e., μ_p , C_{ox} , V_{th}) and by the design (i.e., W , L). $V_{GS(M1)}$ is defined as:

$$V_{GS(M1)} = V_{G(M1)} - V_{S(M1)} = V_{Cl} - V_{Cl1} \quad (39)$$

Thus, the voltage difference between V_{Cl} and V_{Cl1} is a constant and adjusted by the design through the $(W/L)_{M1}$ ratio. Therefore, the circuit shown in Fig. 19 provides a constant positive voltage shift for V_{Cl1} (approximately +350 mV).

The principle used to generate V_{Cl2} is the same as the one used to generate V_{Cl1} :

$$I_{bias} = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_{M2} \cdot (V_{GS(M2)} - V_{th})^2 \quad (40)$$

$$V_{GS(M2)} = V_{G(M2)} - V_{S(M2)} = V_{Cl} - V_{Cl2} \quad (41)$$

However, the voltage shift provided by the NMOS M_2 is negative. The body effect of M_2 is cancelled by connecting its bulk directly to its source. This is possible because M_2 is an NMOS transistor in triple-well, since UMC provides such an option in its L180 CMOS technology. The $(W/L)_{M2}$ ratio is also used to adjust by design the difference between V_{Cl} and V_{Cl2} (approximately -350 mV).

As explained previously, the duty cycle of the boost converter must be limited to 75%–95% to avoid unlimited energizing of the power inductor L_1 (see Fig. 6). This represents a voltage down shift between 40 mV and 200 mV of the maximum triangular oscillator voltage V_2 , since the amplitude of the waveform generated by the triangular oscillator is 800 mV. In the circuit shown in Fig. 19, the down shifting of

V_2 is accomplished by the NMOS M_0 . Since this down shift is around 100 mV, the use of a low- V_{th} transistor is mandatory for M_0 . The value of the down shift voltage is adjusted by the $(W/L)_{M_0}$ ratio.

Unfortunately, the low- V_{th} transistors do not exist with the triple-well option in the chosen UMC L180 technology. Therefore, the body effect occurring in M_0 is unavoidable. However, this is not an issue, since the voltage V_2 is fixed and constant, thus the drain-source voltage drop $V_{DS(M_0)}$ across M_0 is also constant, because M_0 is biased by a constant current source I_{bias} . Therefore, the bulk-source voltage V_{BS} is also constant. Finally, the maximum value of V_{Cl2} is given by:

$$V_{Cl2} \leq V_2 - V_{th(M_0)} - V_{DS(M_2)} \quad (42)$$

The combination of the two voltage shifters and the duty cycle limiter shown in Fig. 19 makes this implementation advantageous compared to the state-of-the-art DC-DC converter in the domains of design complexity and design size. Namely, only two transistors are needed for doing the voltage shifting (M_1 , M_2), one more for performing the duty cycle limitation (M_0), and two more for the current sources providing I_{bias} . Further, the method developed by B. Sahu *et al.* [11] was widely improved and adapted for bi-directional DC-DC converters operating with high switching frequencies. The novel proposed PWM control circuit is easy to design and to implement, and also very robust against noise.

C. Symmetrical Triangular Waveform Oscillator

The PWM oscillator providing the V_{osc} signal consists of a symmetrical triangular waveform oscillator. The schematic of the triangular oscillator is shown in Fig. 20, and the corresponding simulation results are presented in Fig. 21.

The switching frequency of the DC-DC converter is defined by the switching frequency of the oscillator that generates the triangular carrier. As shown in the schematic in Fig. 20, the principle used for generating the triangular voltage waveform carrier V_{osc} consists in charging and discharging the capacitor C_{osc} with the same constant current I_{osc} , thus generating a waveform with a constant slope:

$$V_{osc} = \frac{1}{C_{osc}} \cdot \int I_{osc} \cdot dt \quad (43)$$

In the schematic presented in Fig. 20, the transistors M_1 , M_2 , M_3 , M_4 , M_5 are used as switches, to power down the triangular oscillator through the \overline{PD} signal, and also to compensate for the drain-source voltage drop across the switching transistors M_6 and M_7 . The external resistor R_{osc} is used to setup the current flowing through the transistor M_8 , which is connected in a diode configuration. The transistor pairs (M_8, M_9), (M_{10}, M_{11}), (M_{12}, M_{13}), (M_{12}, M_{14}) are connected in a current mirror configuration. The drain currents in M_{12} , M_{13} , M_{10} are therefore identical. When M_6 is turned on (i.e., M_7 is turned off), the drain current in M_{14} is equal to the drain current in M_{12} . On the contrary, when M_7 is turned on (i.e., M_6 is turned off), the drain current in M_{11} is equal to the drain current in M_{12} . The turn-on and turn-off of M_6 and M_7 is done by the clock signal CLK, which is itself constructed

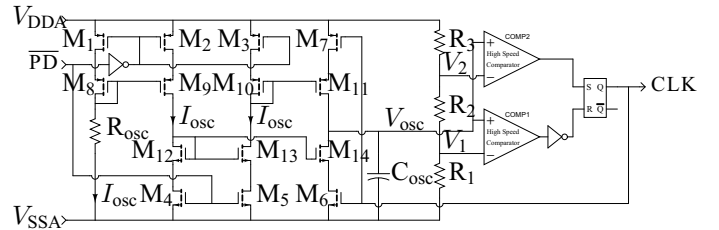


Fig. 20. Schematic of the triangular waveform oscillator. The switching frequency is adjusted by R_{osc} . The active low \overline{PD} signal is used to power down the oscillator.

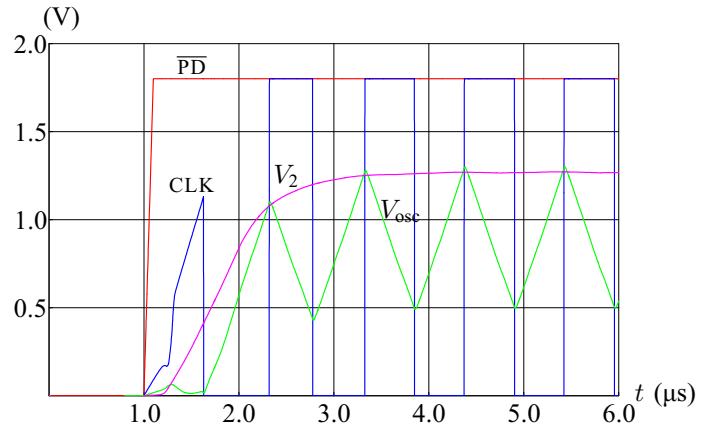


Fig. 21. Simulation results of the triangular waveform oscillator.

in the following way: when M_6 is turned off, M_7 is turned on, the constant current I_{osc} is sourced by M_{11} , thus charging C_{osc} . V_{osc} increases, and when it reaches V_2 , COMP2 outputs a logic 1 and sets the RS flip-flop output Q to 1. This turns off M_7 and turns on M_6 , so M_{14} is sinking the constant current I_{osc} , thus discharging C_{osc} . As a result, V_{osc} decreases, until it reaches V_1 . Then COMP1 resets the RS flip-flop and the next cycle begins. The configuration of the comparators COMP1 and COMP2 avoid the possibility of having both R and S signals high simultaneously.

The reference voltages V_1 and V_2 are noise sensitive. Since the high speed comparators generate noise on their noninverting inputs when their output switches, the not-noisy inverting inputs have been connected to the reference voltages V_1 and V_2 . In the designed prototype, V_1 is set to 0.5 V and V_2 to 1.3 V (see Fig. 12). The noisy noninverting inputs have been connected to the V_{osc} triangular waveform. The reason for this is that the V_{osc} voltage is less noise sensitive because of the presence of the C_{osc} capacitor. In this configuration, the triangular oscillator in Fig. 20, which is supplied by the 1.8 V V_{core} voltage, is able to generate a triangular waveform with low distortion at frequencies up to 10 MHz. When R_{osc} is adjusted so that the oscillator frequency is 1 MHz, the oscillator consumes a total power of $80 \mu\text{W}$ (i.e., $45 \mu\text{A}$ at a supply voltage of 1.8 V). The startup time is less than $2 \mu\text{s}$, as shown in Fig. 21.

D. High Speed Comparator

For the PWM regulator shown in Fig. 17 and for the triangular waveform oscillator shown in Fig. 20, the comparators COMP1 and COMP2 are two high speed comparators. These high speed comparators are based on the *very-wide common-mode-range differential amplifier* (VCDA) developed by M. Bazes [22]. The schematic of such a comparator is shown in Fig. 22 and the corresponding simulation results are provided in Fig. 23. The VCDA provides a rail-to-rail voltage input range since it uses complementary MOSFETs in the input stage (M_1, M_2, M_3, M_4). The NMOS M_1 and M_2 are isolated in triple-well so that the bulk can be shorted with the source to cancel the body effect. The output of the VCDA has been buffered to provide a rail-to-rail output swing with improved driving strength (M_{14}, M_{15}). The transistor M_{16} is used as decoupling capacitor on the power rails to absorb the important current peaks generated in the supply rails by the fast switching transients occurring in fast comparators.

Fig. 23 shows the simulation results obtained in the Cadence Spectre environment when the VCDA is supplied by a 1.8 V voltage. Because of their influence on the signal delay (approximately a factor 2), the layout parasitics were considered for the simulations. Therefore, the extracted layout of the VCDA was used to get these simulation results. A fixed 1.0 V voltage has been provided to the noninverting input and a square wave has been applied to the inverting input. The overdrive voltage of the square wave applied to V_{in}^- is about 50 mV and its frequency is 10 MHz. The output is switching from rail-to-rail with a delay of approximately 8 ns. If the parasitics are not taken into account, the observed delay is only about 5 ns. The low power VCDA developed for the PWM control circuit consumes less than $30 \mu\text{W}$ ($16 \mu\text{A}$ at 1.8 V). To our knowledge, it is the fastest low power comparator reported in the literature. Further on, when the designed VCDA is supplied with 3.3 V, the comparison time becomes less than 4 ns, but $330 \mu\text{W}$ of power are then consumed (i.e., the quiescent current is $100 \mu\text{A}$).

V. EXPERIMENTAL RESULTS

The developed PWM control circuit presented in Fig. 17 was implemented in an ASIC prototype shown in Fig. 24. The size of the silicon die of the fabricated bi-directional DC-DC converter is $3 \text{ mm} \times 1.5 \text{ mm}$ (i.e., 4.5 mm^2). The area occupied by the full-bridge containing the power transistors and the high frequency gate drivers is approximately 2.32 mm^2 . A digital part was also implemented for test purposes to get access to the different internal control signals.

A four metal layer test board shown in Fig. 25 was developed for performing the experimental measurements. For the oscillograms shown in Fig. 26, Fig. 27, and Fig. 28, a $4.7 \mu\text{H}$ SMD power inductor and a $22 \mu\text{F}$ SMD tantalum output filter capacitor were used.

The oscillograms in Fig. 26, Fig. 27, and Fig. 28 present the measurements for a 56Ω load, an output load voltage V_{out} of 1.8 V, and a decrease in the battery voltage V_{in} from 2.1 V to 1.6 V. The experimental results presented hereafter comply with the theory presented in Section III. They were

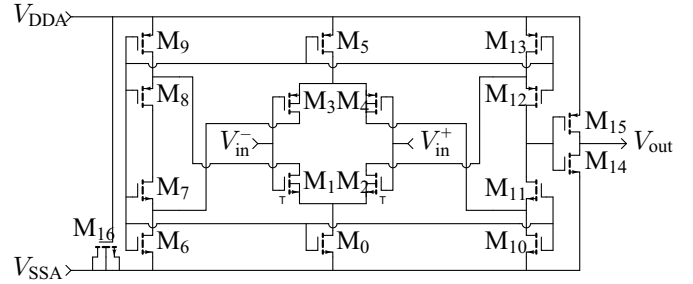


Fig. 22. Schematic of the high speed VCDA comparator [22].

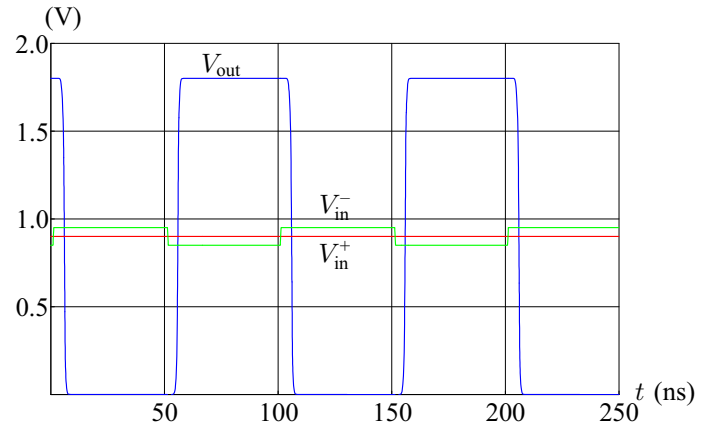


Fig. 23. Extracted layout simulation results (i.e., with parasitics) of the high speed VCDA comparator when it is supplied by a 1.8 V voltage. In this case, the comparison time is approximately 8 ns.

obtained during the discharging of the battery when the DC-DC converter is supplying a load (i.e., 56Ω resistor) with a regulated voltage (i.e., 1.8 V). Similar results can be obtained during charging of the battery, since the same PWM regulation unit is used in both energy flow directions.

The bi-directional DC-DC converter was designed to operate with a full-bridge topology using synchronous rectification at frequencies as high as 10 MHz. For the high frequencies tests, a silicon integrated $0.15 \mu\text{H}$ inductor provided by CEA-LETI (Grenoble, France) was used. The measurements shown in Fig. 29 confirms that the designed prototype is able to operate at frequencies as high as 12 MHz. With the $0.15 \mu\text{H}$ silicon inductor, however, the voltage ripple begins to become visible on V_{out} .

To achieve a high power conversion efficiency, the designed DC-DC converter uses synchronous rectification. The anti-crossconduction logic adds a dead-time between the turn-off of the rectifying transistor (M_2 and M_3 , respectively) and the turn-on of the energizing transistor (M_1 and M_4 , respectively) (see Fig. 5 and Fig. 6). This delay was set per design to 4 ns, without considering the interconnection parasitics. It is applied to the BUCK and BOOST signals and depends only on the regulated V_{core} voltage. In other words, the dead-time is independent of V_{in} and V_{out} , thus ensuring a constant delay in any operating condition. Experimentally, the measured dead-time shown in Fig. 29 is approximately 6 ns, because of the interconnection parasitics.

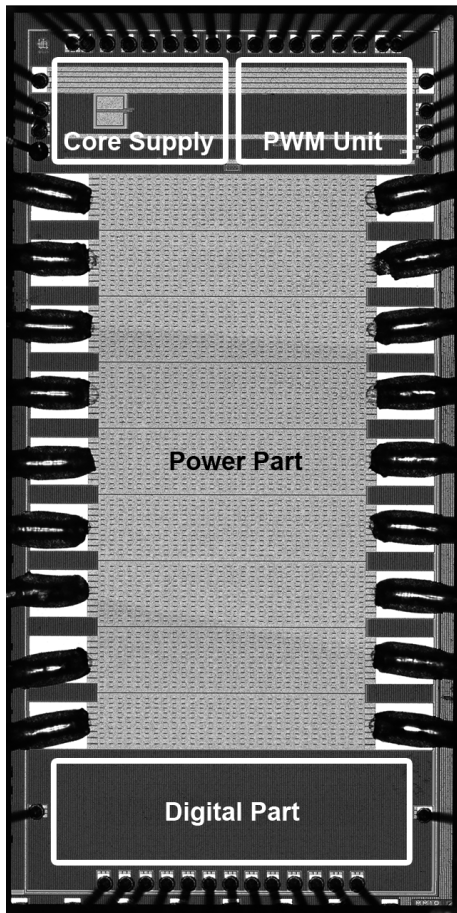


Fig. 24. Chip photograph of the prototype. The power pads with 75 μm aluminum bond wires (wedge bonds) can be clearly distinguished from the signal pads with 25 μm gold bond wires (ball bonds).

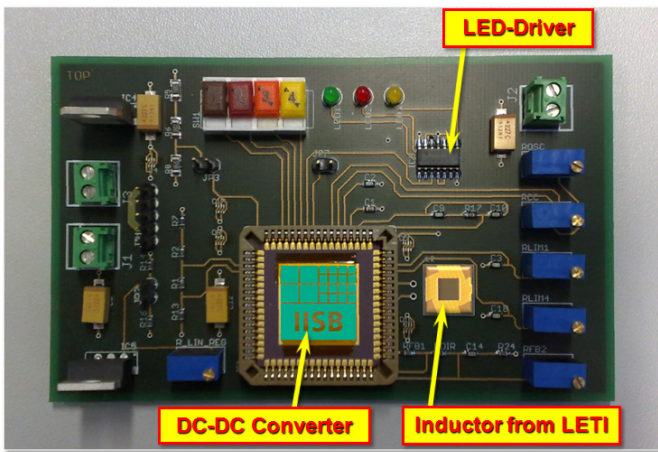


Fig. 25. Photograph of the four metal layer demonstrator board. The 0.15 μH silicon inductor was only used for the 12 MHz switching frequency test.

The bi-directional DC-DC converter was designed for battery powered mobile applications, thus the variation of the voltage provided by the battery is a slow phenomenon (i.e., the time constant is in seconds or minutes). However, since the converter is bi-directional (for allowing the battery to be recharged), the high speed VCDA comparator shown in Fig. 22 was also used to detect the connection and disconnection of

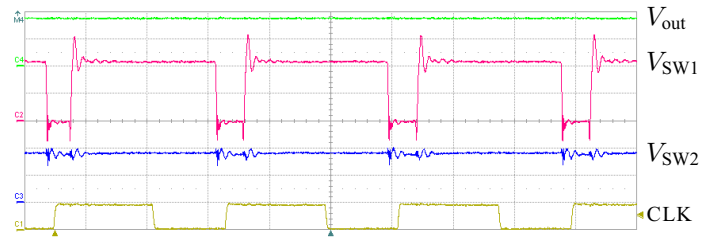


Fig. 26. Oscilloscope of the prototype in buck mode ($V_{in} = 2.1\text{ V}$, $V_{out} = 1.8\text{ V}$). Time scale: 500 ns/div ; voltage scale: 2 V/div for CLK, 1 V/div for V_{SW1} , V_{SW2} and V_{out} .

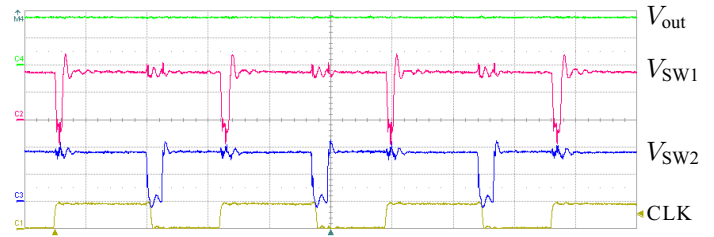


Fig. 27. Oscilloscope of the prototype in buck-boost mode ($V_{in} = 1.8\text{ V}$, $V_{out} = 1.8\text{ V}$). Time scale: 500 ns/div ; voltage scale: 2 V/div for CLK, 1 V/div for V_{SW1} , V_{SW2} and V_{out} .

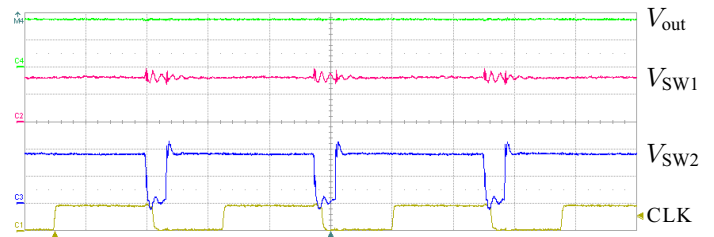


Fig. 28. Oscilloscope of the prototype in boost mode ($V_{in} = 1.6\text{ V}$, $V_{out} = 1.8\text{ V}$). Time scale: 500 ns/div ; voltage scale: 2 V/div for CLK, 1 V/div for V_{SW1} , V_{SW2} and V_{out} .

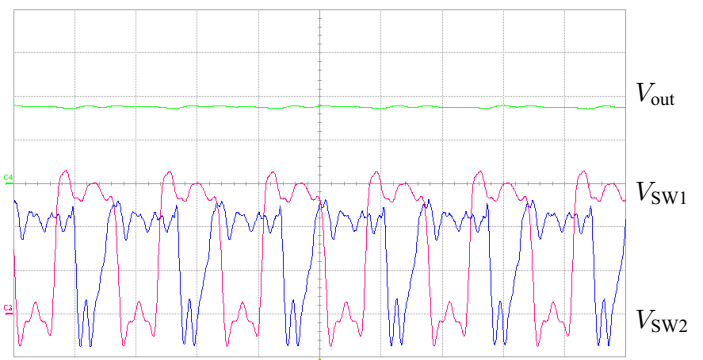


Fig. 29. Oscilloscope of the prototype in buck-boost mode at 12 MHz. Time scale: 50 ns/div ; voltage scale: 1 V/div.

a charger. The detection of the disconnection of the charger has to occur very rapidly since it connects directly in parallel to the load. A transient view of a forced charger detection, through a digital signal V_{dir} , is shown in Fig. 30. The detection is forced by tying the V_{dir} pin high so that the bi-directional DC-DC converter is told that a charger has been connected and it has to revert the direction of the energy flow to recharge the battery. After 32 clock periods, it tries to revert the energy flow (pulses shown on the CHG signal), but in less than 10 ns, a voltage drop of approximately 8% in the output voltage V_{out} is detected and the energy flow is reverted back going from the battery to the load.

Although the energy conversion efficiency of the DC-DC converter is not the focus of this paper [14], the experimental results plotted in Fig. 31 show that the integrated bi-directional buck-boost DC-DC converter with its full-bridge topology and using synchronous rectification can be operated with an efficiency as high as 77%.

VI. CONCLUSION

A novel integrated PWM control circuit allowing smooth transitions between conversion modes (i.e., buck, special buck-boost and boost mode) in full-bridge based bi-directional DC-DC converters designed for operating at switching frequencies as high as 10 MHz was fabricated in a 0.18 μm CMOS technology from UMC. The PWM control circuit was modelled, its theory was analyzed, and the method for computing the transfer function in CCM over the three operating modes were presented. The circuit of the PWM control and the designed circuit blocks were shown (i.e., error amplifier, voltage shifter, duty cycle limiter, symmetrical triangular waveform oscillator, high speed comparator). A prototype of the designed bi-directional DC-DC converter ASIC integrating the power part (i.e., full-bridge with high frequency drivers), the analog part (PWM control circuit with internal core power supply), and the digital part (i.e., test circuit) was manufactured. The experimental results have shown a very high accordance with the theoretical results and a maximum operating frequency of 12 MHz was reached in practice. The DC-DC converter was combined with a silicon integrated power inductor of 0.15 μH provided by CEA-LETI.

The proposed PWM control circuit is well suited for uni-directional and bi-directional DC-DC converters based on the full-bridge topology. It enables smooth transitions between the voltage step-up and step-down modes in both conversion directions (i.e., charging and discharging of a mobile system powered with a battery) and operates highly efficient with synchronous rectifications at high switching frequencies (i.e., experimentally as high as 12 MHz).

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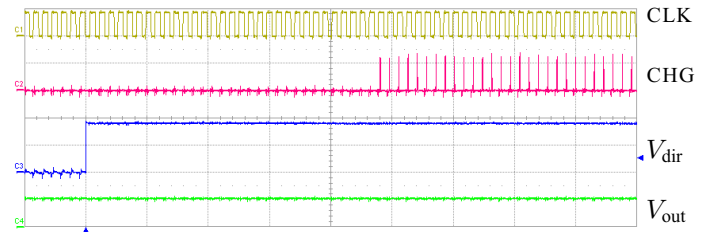


Fig. 30. Oscilloscope of a forced charger detection but without connected charger. Time scale: 10 $\mu\text{s}/\text{div}$; voltage scale: 2 V/div for CLK and V_{out} , 1 V/div for CHG and V_{dir} .

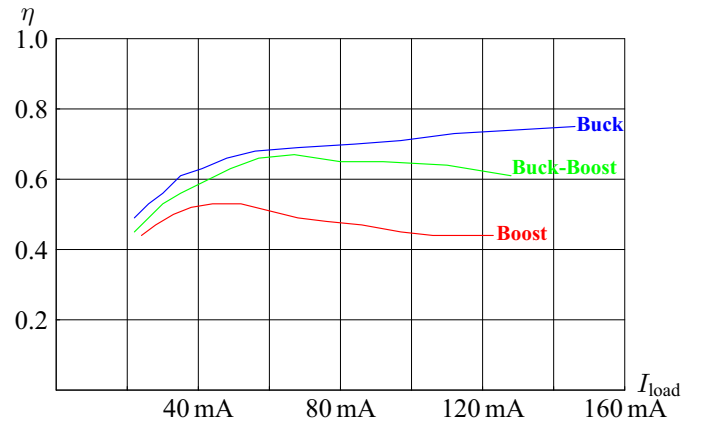


Fig. 31. Experimental efficiency of the bi-directional DC-DC converter in buck mode (3.0 V \rightarrow 1.8 V), buck-boost mode (1.8 V \rightarrow 1.8 V), and boost mode (1.4 V \rightarrow 1.8 V).

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