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FPGA-based Real Time Current Sensor Failure Diagnosis for Shunt Active Power Filters

S. Karimi*, P. Poure** and S. Saadate*

*Groupe de Recherches en Electrotechnique et Electronique de Nancy, GREEN-UHP, CNRS UMR 7037

** Laboratoire d'Instrumentation Electronique de Nancy, LIEN, EA 3440

Université Henri Poincaré de Nancy I, BP 239, 54506 Vandoeuvre les Nancy cedex France

E-mail: {[shahram.karimi](mailto:shahram.karimi@green.uhp-nancy.fr), [shahrokh.saadate](mailto:shahrokh.saadate@green.uhp-nancy.fr)}@green.uhp-nancy.fr , philippe.poure@lien.uhp-nancy.fr

*Abstract-*The performances of conventional shunt active power filters heavily depend on the accurate active filter current sensing. A sudden failure in one of the active filter current sensors decreases the filter performances. Moreover, if the fault is not detected and compensated quickly, its effect leads to disconnection or hard failure of the active filter. Hence, to reduce the failure rate and to prevent unscheduled shutdown, real-time fault detection, isolation, and compensation scheme could be adopted. This paper introduces new fast and robust current sensors fault detection and compensation method for three-phase shunt active power filters. The proposed current sensors fault detection is achieved by a predictive model associated with a logical decision. The satisfactory performances obtained by experimental “FPGA in the loop” prototyping validate the effectiveness of the proposed method.

Keywords – Current sensor failure, fault tolerant, failure diagnosis, FPGA, active power filter.

I. INTRODUCTION

Generally, harmonic currents are mostly generated by the AC/DC power conversion units and the power electronic equipments, used in domestic and industrial applications. The harmonic currents are the source of adverse effects for many types of equipments such as heating in distribution transformer, perturbation of sensitive control equipments and resonances with the grid. The recent development of power electronics components and digital control processors allowed the design of harmonic currents compensating structures, so-called active power filters. Active power filters produce a nearly sinusoidal supply current by measuring the harmonic currents and then injecting them into the power system with a 180° phase shift.

The performance of an active power filter depends on many factors, but mainly on the control strategy. To control the compensating harmonic currents generated by the active power filter, current measurement is mandatory. Therefore, the

control strategy and the filter output currents heavily depend on the accurate active filter current sensing. A sudden failure of one of the active filter current sensors decreases the filter performances. Moreover, if the fault is not detected and compensated quickly, its effect can lead to disconnection or hard failure of the active filter. These events are introduced because the active filter current sensor outputs are used in the closed-loop control system. Hence, to reduce the failure rate and to prevent unscheduled shutdown, real-time fault detection and compensation scheme could be adopted.

In the last few years, significant amounts of research studied sensor fault detection in electrical machine drive systems by analysing the residual between measured and estimated current [1]–[4]. In the papers [1]–[3], state observers have been used to estimate the phase currents. More recently, the authors of [4] have presented a Luenberger observer based current sensor fault detection for doubly fed induction generator. It is important to note that in active filter case, unlike in the case of electrical machine drive systems, state observers can not be used because the state equations of the load and of the electrical network change over time.

Furthermore, there has been significant interest in techniques for eliminating the phase current sensors at the voltage source inverter output terminal in favor of using the single dc-link current sensor to reconstruct the three phase currents [5]–[8]. The authors of [9] have proposed a current reconstruction method to estimate the phase currents and by this way they have realized a sensor fault tolerant induction motor drive. Although the previous current reconstruction methods reported good results in electrical machine application cases, they have a number of limitations [10]: since the DC link current waveforms are mostly narrow current pulses. Consequently, complex hardware circuits are required to detect the current values at specified points for currents which are usually distorted by measurement noise. Moreover, these methods are not particularly suited for active filter application, where very fast phase current variation (high di/dt) and high switching frequency introduce important errors in the reconstructed phase currents.

Because of the impossibility of using state observers and considering the difficulty to implement current reconstruction methods in active filter application case, we propose in this paper a new fast and robust current sensors fault detection and compensation method for three-phase shunt active power filters. This method is achieved by a predictive model associated with a logical decision. The satisfactory performances obtained by experimental “FPGA in the loop” prototyping validate the effectiveness of the proposed method.

II. SYSTEM CONFIGURATION

Fig. 1 shows the three-phase shunt active power filter system configuration. It is composed of the three-phase shunt active power filter, the grid, the non-linear load and the control system. The shunt active power filter consists of a three-phase voltage source inverter, three equal series inductances L_f with resistances R_f and a DC capacitor. The non-linear load is a three-phase

diode rectifier feeding (R, L) load. The active filter output currents are controlled to provide in real time the harmonic currents generated by the non-linear load to ensure filtering.

Fig. 2 shows the block diagram of the conventional control strategy. It consists in the harmonic isolator and the current controller. The harmonic isolator determines the current references which must be generated by the active filter. The current controller is used to control the switches of the voltage source inverter. There are different methods to determine the current references and control the switches [11], [12]. However, in most of the studied control strategies, two current sensors are used to measure the filter currents.

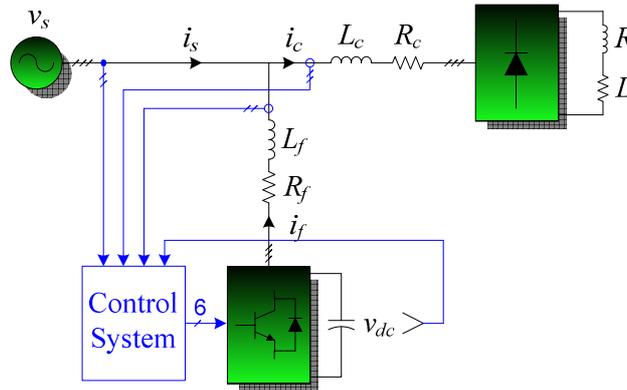


Fig. 1. System configuration.

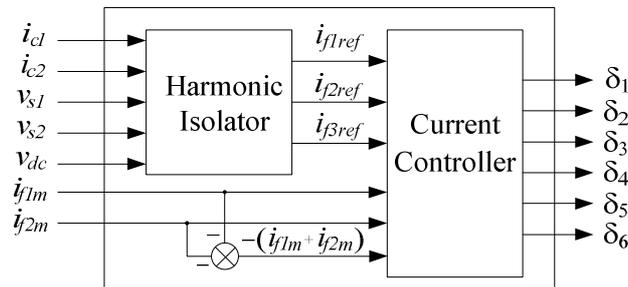


Fig. 2. Block diagram of the conventional control system.

In Fig. 2, index m denotes the measured current to clarify the difference between the measured and real active filter currents. Under normal operation, the measured active filter currents (i_{f1m} and i_{f2m}) are equal to the real ones (i_{f1} and i_{f2}). Differences arise when current sensor failure occurs.

III. FAILURE DIAGNOSIS AND COMPENSATION

Hall effect based current sensors are usually used to measure the active filter currents. They are mainly composed of a Hall element and an OP-AMP circuit. The sensor may provide erroneous measurements due to several causes, such as offset in the OP-AMP circuit. Table I shows these faults and their models for filter current sensors placed in the phase k ($k = \{1, 2, 3\}$).

TABLE I
CURRENT SENSOR FAULT CASES

Fault case	Model (i_{fkm})	Error ($i_{fkm} - i_{fk}$)
Gain change	$(1+k_g) i_{fk}$	$k_g i_{fk}$
Offset	$i_{fk} + I_{\text{offset}}$	I_{offset}
Open circuit	0	$-i_{fk}$
Intermittent disconnection	$[0, i_{fk}]$	$[-i_{fk}, 0]$

To achieve current sensor failure diagnosis and compensation, only one additional current sensor is required, placed in the third phase. Therefore, in normal operation, two conventional sensors are used and the third one will replace the faulty sensor after fault detection. With this scheme, the different active filter current sensor fault cases (see Table I) can be detected. Fig. 3 shows the block diagram of the modified control system to detect and compensate a faulty current sensor. In this figure, \hat{i}_{fkm} ($k = \{1, 2, 3\}$) are the compensated currents. The failure diagnosis and compensation shown in this figure is composed of the six following functional blocks (see Fig. 4), discussed in the following:

- Fault detection block;
- Current prediction block;
- Residual generation block;
- Faulty sensor identification block;
- Fault compensation block;
- Time to clear block.

A. Fault Detection

The fault detection block detects the occurrence of any fault and activates the time to clear block. For the detection, a three-phase current balancing test is employed. To detect the faulty sensor and replace it by another one, one additional current sensor has been added. Under normal operation, the sum of the three measured active filter output currents is near to zero. We can detect a possible fault in one of the current sensors by means of a comparator. In this case, the absolute value of the sum of the three measured active filter currents is compared with a threshold. Thus, when a fault appears in one of the current sensors, the comparator output becomes one. The threshold value depends on the accuracy of the current prediction block and must be greater than the maximum error between the measured current and the predicted

one. Fig. 5 shows the principle of the fault detection block. In this figure I_t and i_{fault} are the threshold value and the fault detection signal, respectively.

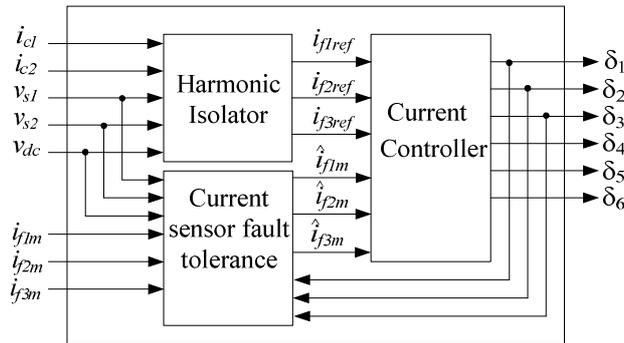


Fig. 3. Block diagram of the modified control system.

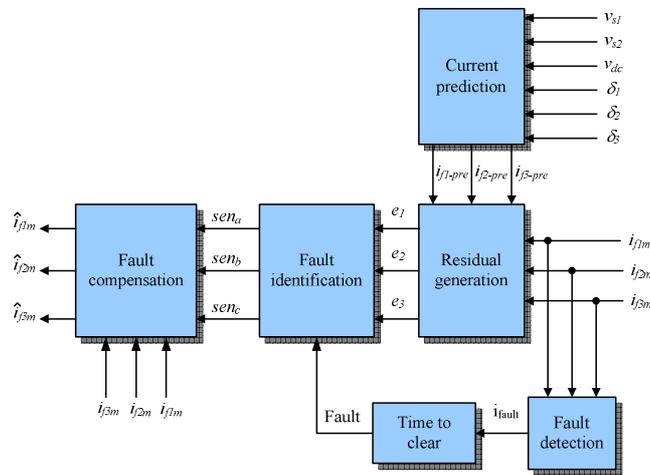


Fig. 4. Current sensor failure diagnosis and compensation.

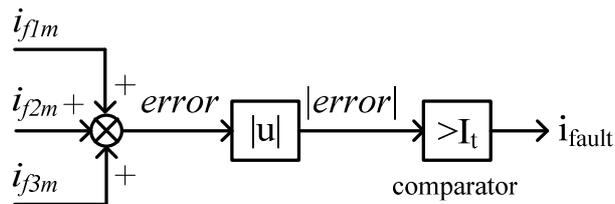


Fig. 5. Principle of the fault detection block.

B. Current Prediction

The current prediction block is used to predict the active filter currents which will be used in the residual generation block. The effectiveness and the performances of the proposed current sensor diagnosis mainly depend on the performances of this block, especially prediction accuracy.

By using the Kirchhoff laws for the active filter system configuration shown in Fig. 6, we obtain the following equation for phase k (k = 1, 2, 3):

$$L_f \frac{di_{fk}}{dt} + R_f i_{fk} + v_{sk} - v_{fk} = 0 \quad (1)$$

Where v_{sk} and v_{fk} are the phase to neutral (n) grid and filter voltages for the phase k, respectively. Because the sum of the active filter currents is null and assuming the grid voltages balanced, we deduce:

$$v_{f1} + v_{f2} + v_{f3} = 0 \quad (2)$$

The filter voltages can be expressed as:

$$v_{fk} = v_{fko} + v_{on} \quad (3)$$

Where v_{fko} is the pole voltage for the phase number k, with o the middle point of the capacitor DC bus. These pole voltages can be estimated by:

$$v_{fko} = (2 \times \delta_k - 1) \times v_{dc} / 2 \quad (4)$$

Where $\delta_k = \{0, 1\}$ is the switching pattern of the top switch S_k and v_{dc} is the dc-link voltage.

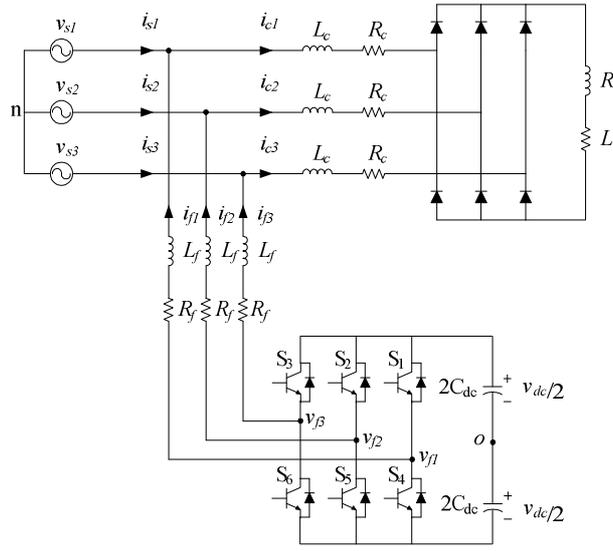


Fig.6. Three-phase shunt active power filter system.

From the expressions (2) and (3), we deduce:

$$v_{on} = -(v_{f1o} + v_{f2o} + v_{f3o}) / 3 \quad (5)$$

Then, one can replace the equation (1) by:

$$L_f \frac{di_{fk}}{dt} + R_f i_{fk} + v_{sk} - v_{fko} - v_{on} = 0 \quad (6)$$

A discrete-time form of the equation (6) for a sampling period T_s can be used to digitally predict active filter currents. By approximating the derivative by:

$$\frac{di_{fk}}{dt} \approx \frac{i_{fk}(m) - i_{fk}(m-1)}{T_s} \quad (7)$$

And replacing it in (6), the following expression is obtained for the active filter current at the m^{th} sampling instance:

$$i_{fk}(m) \approx \frac{1}{R_f T_s + L_f} [L_f i_{fk}(m-1) + T_s (v_{sk} - v_{fko} - v_{on})] \quad (8)$$

Since the active filter currents vary quickly with the time, the sampling period must be small enough to reduce the error between these predictive currents and the measured ones. The required small sampling period can be obtained by using an FPGA-based digital implementation. Thus, the term $R_f T_s$ can be neglected. So, the equation (8) becomes:

$$i_{fk}(m) \approx i_{fk}(m-1) + \frac{T_s}{L_f} v_{zk} \quad (9)$$

Where v_{zk} corresponds to the voltage across the series impedance (R_f, L_f) for the phase k . This voltage is expressed by:

$$v_{zk} = v_{sk} - v_{fko} - v_{on} \quad (10)$$

By replacing the equation (5) in (10), we deduce:

$$v_{zk} = v_{sk} - (2v_{fko} - v_{fio} - v_{fjo})/3 \quad (i \neq j \neq k \in \{1, 2, 3\}) \quad (11)$$

Considering the equations (4) and (11), the voltage v_{zk} can be estimated using the measured dc-link voltage, the grid voltage v_{sk} and the three switching pattern δ_1, δ_2 and δ_3 generated by the current controller. Fig. 7 shows the principle used to estimate the voltage v_{zk} .

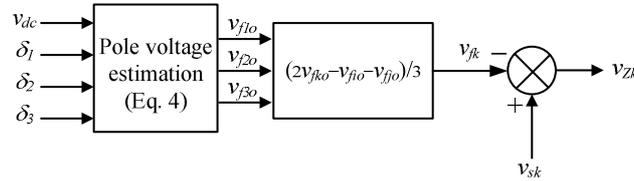
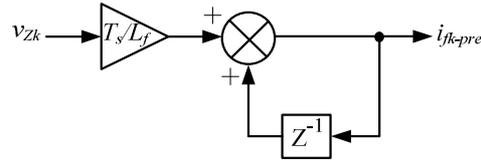
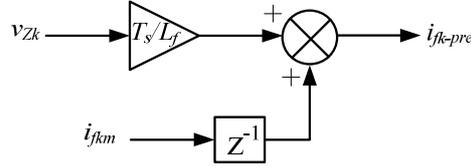


Fig.7. Estimation of the voltage v_{zk} .

By means of the equation (9), the filter current can be predicted using the estimated voltage v_{zk} and the filter current at the previous sampling time. The filter currents at the previous sampling time can either be determined by feed-backing the previous predicted current or using the previous measured current. These two solutions are illustrated in Fig. 8. Fig. 8a shows the current prediction by feed-backing and Fig. 8b shows the current prediction using the measured current. In these figures, i_{fk-pre} and i_{fk-m} are the predicted and measured current for phase k , respectively.



(a)



(b)

Fig.8. Current prediction (a) by feedbacking predicted current,
(b) by using measured current.

We point out that the first solution (Fig. 8a), which means open loop integration, leads to DC drift problem due to offset in grid voltage sensors. Moreover, in this solution the parameter mismatching (L_f) introduce the time-dependent error in the predicted current. The second solution has another disadvantage. If the current sensor failure occurred when the real filter current is small and crosses zero, the fault detection block cannot detect the fault if the absolute error is smaller than the threshold value used in the fault detection block. Therefore, the false measured current is used to predict the filter current. Then, when the fault detection block detects the fault, a false faulty sensor may be identified.

To solve the above problems, authors propose an hybrid solution which uses both solutions presented above. The principle of the proposed technique is shown in Fig. 9. In this technique, by using a comparator with the threshold value h , the filter current at the previous sampling time is determined by feed-backing the predicted current when the real current is small (first mode). Otherwise, the filter current at the previous sampling time is determined using the measured current (second mode). To ensure a correct failure diagnosis, the threshold value h must be chosen greater than the threshold value of the comparator used in the fault detection block (I_t in Fig. 5). The error introduced by even parameter mismatching (L_f) in the current i_{fk-pre} , predicted in the first mode can be suppressed by almost using the second mode. The small sampling period decreases the effect of parameter mismatch and the error between the real current and the predicted one remains very small, because there is no integration in the second mode (see Fig. 8). So that, the error introduced by even parameter mismatching is negligible in the second mode and this error remains negligible during the short time interval while the proposed hybrid method works in the first mode. Consequently, the h values near of I_t are preferred.

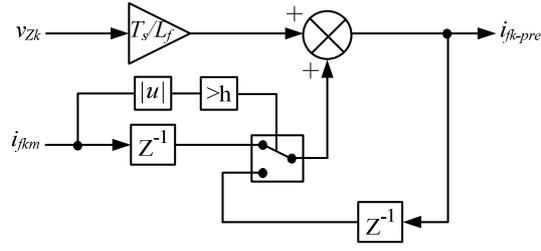


Fig.9. Proposed hybrid method for current prediction.

C. Residual Generation

The residual generation block receives the predicted and measured filter currents. It generates the residuals by comparing the predicted values with the measured ones. This block generates the three current residuals e_1 , e_2 and e_3 :

$$e_k = \left| i_{fkm} - i_{fk-pre} \right| \quad (11)$$

These three current residuals are the inputs of the faulty sensor identification block.

D. Faulty Sensor Identification

The faulty sensor identification block receives the residual values, e_k ($k = 1, 2, 3$), from the residual generation block and the fault signal, so called *Fault*, from the time to clear block. The faulty sensor identification block determines the faulty sensor only when the fault signal is one. Because of the noise measurement and the difference between the estimated currents and the real ones, the maximum of the three current residuals is considered to find out the faulty sensor. The outputs of this block are three identification signals (sen_a , sen_b and sen_c) which identify the faulty sensor. These signals will be used in the fault compensation block.

E. Fault Compensation

The fault compensation block receives the identification signals from the faulty sensor identification block and compensates the faulty sensor. The faulty sensor is easily compensated by replacing its output signal by the compensated one, calculated from the two other healthy current sensor outputs. The principle of the fault compensation block is shown in Fig. 10.

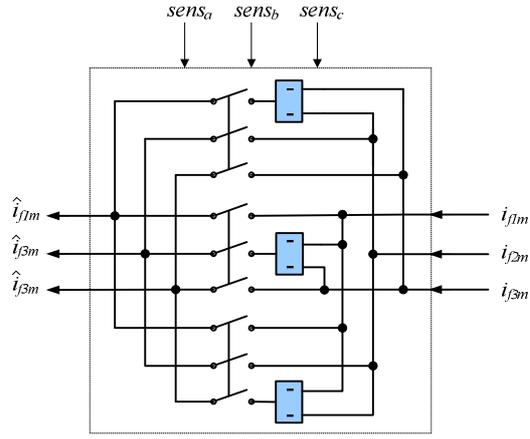


Fig. 10. Principle of the fault compensation block.

F. Time to Clear

Under faulty condition, the absolute value of the sum of the three measured active filter output currents, used in the fault detection block, is equal to the absolute value of the error mentioned in Table I. As one can notice in Table I, the error depends on the faulty sensor real current, i_{fk} , for the gain change, open circuit and intermittent disconnection fault cases. The fault can be detected only when the absolute value of the error is greater than the threshold value of the comparator used in the fault detection block (I_t in Fig. 5). However, at current zero crossing time, the absolute value of the error naturally falls below the threshold value. Therefore, the comparator output becomes zero and the faulty sensor will be used until the current increases and so on.

To get rid of this non suitable operation, i. e. false come back to healthy state, we verify, using the block called "time to clear", how long the fault is supposed to have disappeared after fault compensation. If this time is longer than 0.01 second (half a period at 50 Hz), the time to clear block considers that the fault is actually cleared and its output signal, *Fault*, becomes zero.

IV. EXPERIMENTAL VALIDATION OF THE REAL TIME DIAGNOSIS AND COMPENSATION

A. System Specification

The specifications of the power system are given in Table II. System configuration has been shown in Fig. 1.

TABLE II
SPECIFICATIONS OF THE STUDIED SYSTEM

Mains voltage	400 V
Mains frequency	50 Hz
Load ac inductor (L_c)	0.8 mH
Load ac resistance (R_c)	0.27 m Ω
Load inductor (L)	40 mH
Load resistance (R)	48.6 Ω
Filter inductor (L_f)	3 mH
Filter resistance (R_f)	5 m Ω
DC link capacitor (C_{dc})	1100 μ F
DC link voltage reference	700 V

B. Control Strategy

The control strategy consists in a harmonic isolator and a current controller. Fig. 11 shows the block diagram of the harmonic isolator. The reference currents are identified using a modified version of the instantaneous active and reactive power method, developed in our laboratory [13] and based on the work presented by H. Akagi [14]. This new strategy is based on two digital voltages and current selective band-pass filters. Thanks to the voltage band-pass filters, the active filter control completely immunises against the voltage harmonics. The current band-pass filter is employed as a high pass filter without generation of any phase delay. The DC link voltage regulator consists of a proportional controller and a first order low-pass filter, used to eliminate the ripples of the DC voltage. The current controller is used to control the switches (S_1 - S_6) of the voltage source inverter. The controller we implemented is a modulated hysteresis current controller [15]. The principle of this controller is shown in Fig. 12. In this modulated hysteresis current controller, the modulated reference signal, i_{kref-m} , is deduced from the sum of the reference current and of a triangular carrier signal whose frequency is equal to the desired switching frequency. This modulated reference signals constitute then the new references of a classical three-phase hysteresis controller.

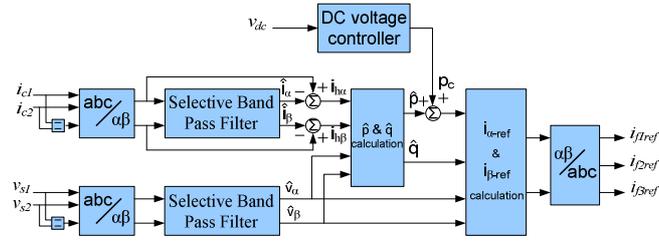


Fig. 11. Block diagram of the harmonic isolator.

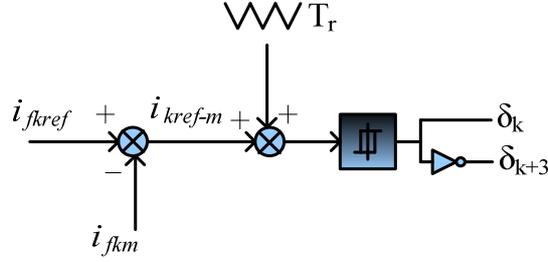


Fig. 12. Principle of the modulated-hysteresis current controller.

C. Time to clear digital design

A Moore Finite State Machine (FSM) is used to implement the control of the time to clear block. Fig. 13 presents the state diagram of the time to clear module. It is based on a control unit and a controllable decrement block. The control unit of the time to clear block is shown in Fig. 14.

D. Faulty sensor identification digital design

As for the time to clear, a Moore FSM is used to implement the control of the faulty sensor identification block. Fig. 15 presents the state diagram of this module. The control unit of this block is shown in Fig. 16. In these figures, the signals *Condition_1*, *Condition_2* and *Condition_3* are determined by:

if (*Fault* = '1') & ($e_1 = \max(e_1, e_2 \text{ and } e_3)$) then *Condition_1* = '1', *Condition_2* = '0' and *Condition_3* = '0';

if (*Fault* = '1') & ($e_2 = \max(e_1, e_2 \text{ and } e_3)$) then *Condition_1* = '0', *Condition_2* = '1' and *Condition_3* = '0';

if (*Fault* = '1') & ($e_3 = \max(e_1, e_2 \text{ and } e_3)$) then *Condition_1* = '0', *Condition_2* = '0' and *Condition_3* = '1';

For this faulty sensor identification scheme, we assume that two sensors cannot fail simultaneously.

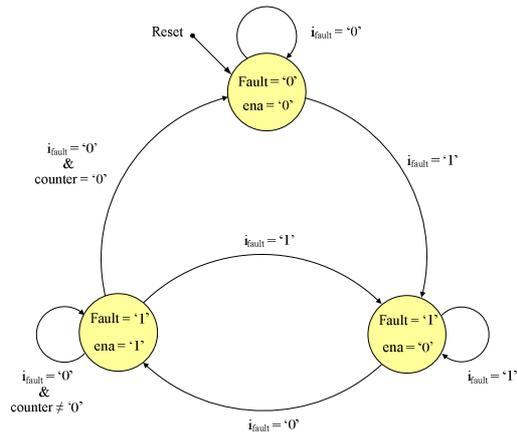


Fig. 13. State diagram of the time to clear module.

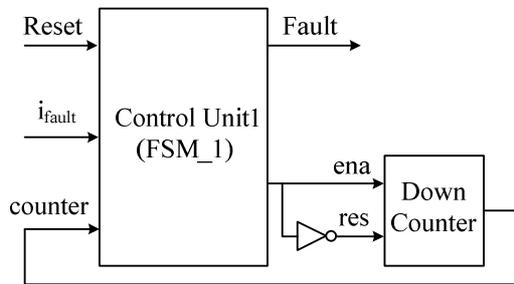


Fig. 14. Control unit of the time to clear block.

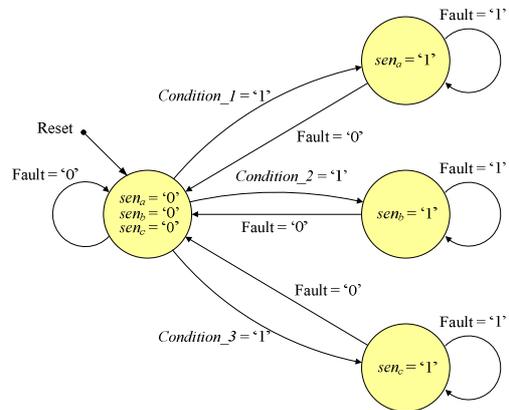


Fig. 15. State diagram of the faulty sensor identification module.

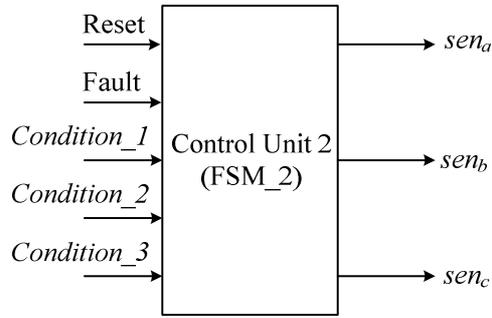


Fig. 16. Control unit of the faulty sensor identification block.

E. “FPGA in the Loop” prototyping methodology

To perform fast fault detection, a FPGA digital implementation of the real time diagnosis is used. This real time diagnosis is implemented together with the active filter control in a single FPGA chip. The active filter control implementation has ever been discussed and presented by the authors in [16]. To test the proposed diagnosis, a new “FPGA in the loop” hardware prototyping method is applied [17]. A Stratix DSP S80 development board, which comprises the Stratix EP1S80B956C6 FPGA chip, was used to implement this real time diagnosis.

Consider now the “FPGA in the loop” principle. At each time step, the power system (Fig. 6) is simulated using the Matlab/SimPower Systems toolbox in discrete-time mode. Then the Simulink output signals (i_{c1} , i_{c2} , i_{f1} , i_{f2} , i_{f3} , v_{s1} , v_{s2} and v_{dc}) are exported to the FPGA. When the FPGA receives these signals, it executes the implemented programme for one sample interval. The FPGA returns to Simulink the switching pattern for the power switches, computed during this “FPGA in the loop” step. At this point, one sample cycle of the FPGA in the loop is performed. In this prototyping method, a Joint Test Action Group interface links Simulink and the FPGA board. Fig. 17 shows the experimental setup used to evaluate the real time current sensor failure diagnosis.

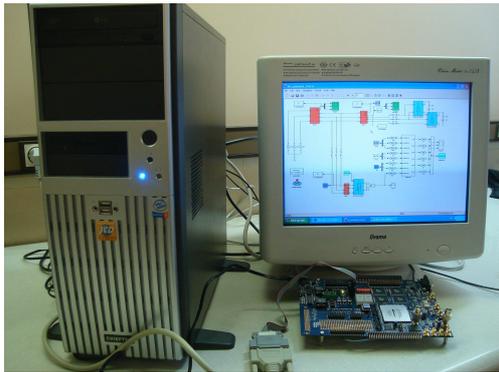


Fig.17. Experimental setup.

F. "FPGA in the Loop" results

This section presents "FPGA in the Loop" results which demonstrate the effectiveness of the fault detection, identification and reconfiguration performances of the proposed method. To attain fast fault detection and decrease the error between the real current and the predicted one, the sampling period T_s used in the proposed method is fixed equal to $0.25 \mu\text{s}$. Fig. 18 shows the active filter performances for harmonic current compensation with accurate and "healthy" current sensing. This figure illustrates the "FPGA in the Loop" results for the load, active filter and source currents. The total harmonic distortion (THD) of the load current is equal to 28.04%. The THD of the source currents is improved down to 1.27% after compensation.

Fig. 19 - 22 present "FPGA in the Loop" results for different faults occurring in the active filter current sensor connected in the phase 1. As one can see, the proposed fault tolerant algorithm preserved the main performance features after any fault occurrence, i. e. a THD value equal to 1.27%. Fig. 19 shows the results when an open circuit fault occurred at $t = 70 \text{ ms}$. One can notice that in this case the current i_{m1} measured by the phase 1 current sensor becomes equal to zero after fault occurrence. However, because of the fast fault detection and compensation, the fault effect does not appear in the active filter current i_{f1} . Fig. 20 presents the results when two intermittent disconnection faults occurred at $t = 60 \text{ ms}$ during 20 ms and at $t = 100 \text{ ms}$ during 10 ms. As one can see in this figure, the fault tolerant algorithm effectively detects the faulty sensor and reconfigures the system at the fault occurrence time. However the control system comes back to healthy state 10 ms (half a period at 50 Hz) after the time that the fault is cleared, because of the time to clear block operation. The identification signal, active filter and measured currents for the phase 1 are depicted in the Fig. 21 when an offset ($I_{\text{offset}} = 2 \text{ A}$) is applied at $t = 70 \text{ ms}$. In this case, as in other cases, the fault is identified and corrected after a very small delay time. Consequently, no significant transient over active filter current i_{f1} can be noticed. The performance of the proposed method during gain change is illustrated in Fig. 22. In this case, the current sensor gain is increased of 50% ($k_g = 0.5$) at $t = 70 \text{ ms}$. One can see that the gain change fault does not disturb the active filter current i_{f1} , when the modified control system is implemented.

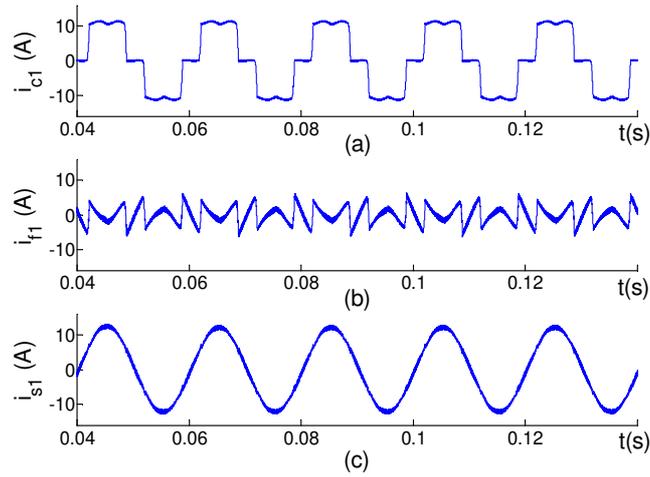


Fig.18. “FPGA in the Loop” results for the phase 1 with accurate and “healthy” current sensing

(a) load current; (b) active filter current; (c) source current.

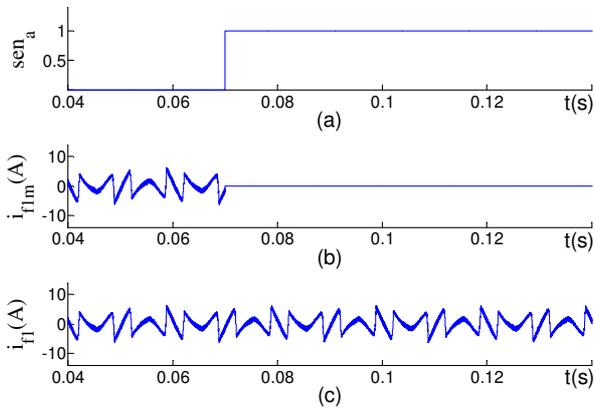


Fig.19. “FPGA in the Loop” results for i_{f1} sensor open circuit fault

(a) identification signal; (b) measured current; (c) active filter current.

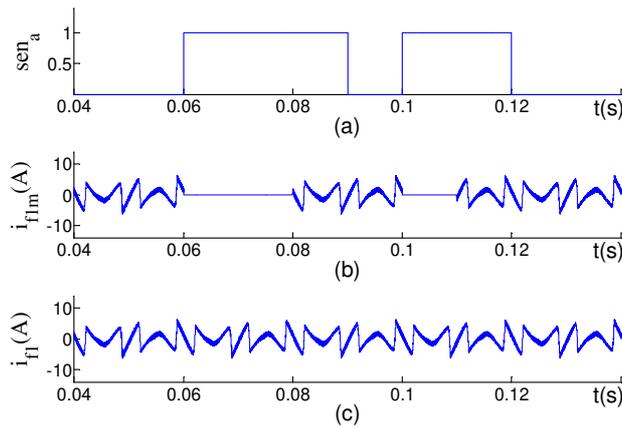


Fig.20. “FPGA in the Loop” results for i_{f1} sensor intermittent disconnection fault

(a) identification signal; (b) measured current; (c) active filter current.

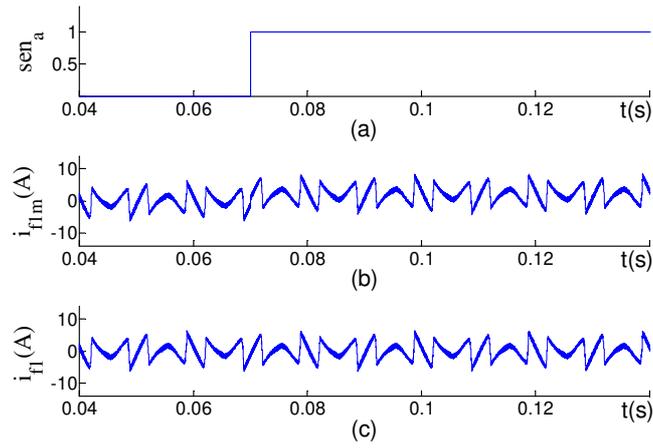


Fig.21. "FPGA in the Loop" results for i_n sensor offset fault

(a) identification signal; (b) measured current; (c) active filter current.

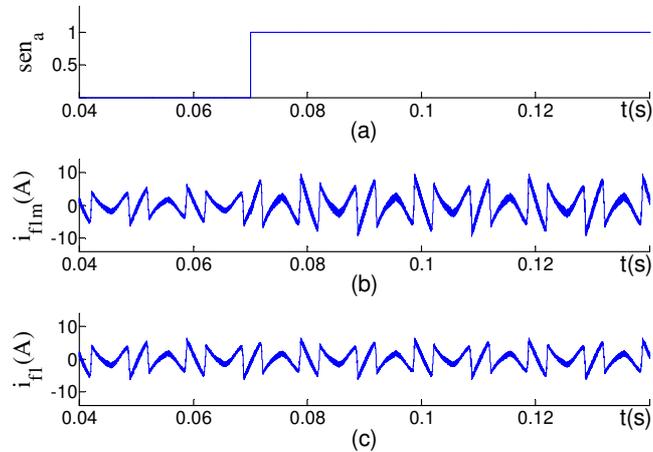


Fig.22. "FPGA in the Loop" results for i_n sensor gain change fault

(a) identification signal; (b) measured current; (c) active filter current.

V. CONCLUSION

This paper has introduced a new fast and robust active filter current sensors fault detection and compensation for three-phase shunt active power filters. The proposed current sensors fault detection is achieved by a predictive model associated with a logical decision. This method effectively detects the sensor failure even if the current crosses zero. More, the two used currents in the current controller are the measured ones even if a fault occurs. Experimental "FPGA in the loop" results have validated the effectiveness and satisfactory performances of the proposed method. This paper has shown with the proposed method, open circuit, intermittent disconnection, offset and gain change fault cases can effectively be detected. The proposed fault tolerant algorithm preserved the main performance features after fault occurrence. Even though this method has been applied to a three-phase shunt active power filter, it is adaptable for any application containing voltage source inverter.

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