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Six-Leg AC-AC Fault Tolerant Converter with Reduced Extra-Sensor Number

Mahmoud Shahbazi^{1,3}, Philippe Poure², Mohammad Reza Zolghadri³, Shahrokh Saadate¹

Abstract – In order to prevent further damage and to provide the continuity of service of six-leg converter in case of open-switch fault, it is mandatory to perform fast fault detection and converter reconfiguration schemes. Extra sensors are needed to detect the faults rapidly. In this paper, a very fast FPGA-based fault detection scheme is presented that minimizes the number of additional voltage sensors. A six-leg fault tolerant converter topology without redundancy and with bidirectional power flow is studied. First simulations are carried out to evaluate the proposed fault detection principle and the fault tolerant converter topology. The fully digital control and the fault detection are implemented on a single FPGA. Experimental tests of the digital controller and the detection scheme are performed to verify the high performance of the proposed method. **Copyright © 2011 Praise Worthy Prize S.r.l. - All rights reserved.**

Keywords: Continuity of service, Fault detection; Fault tolerant six-leg converter, Field Programmable Gate Array (FPGA)

Nomenclature

$v_{a1}^*, v_{b1}^*, v_{c1}^*$	Voltage references at source-side before ZSS
$v_{a2}^*, v_{b2}^*, v_{c2}^*$	Voltage references at load-side before ZSS
v_{a1}, v_{b1}, v_{c1}	Voltage references at source-side after ZSS
v_{a2}, v_{b2}, v_{c2}	Voltage references at load-side after ZSS
v_{zs}	Zero sequence voltage
$\left. \begin{matrix} v_{A1}, v_{B1} \\ v_C \\ v_{A2}, v_{B2} \end{matrix} \right\}$	Five-leg converter voltage references
T_i	Command of upper switch of leg i
n	DC-link middle point
V_{kn}	Voltage between leg k and dc-link middle point
$V_{ij,es}$	Estimated voltage between legs i and j
$V_{ij,m}$	Measured voltage between legs i and j
V_{dc}	DC-link voltage
h	First comparator's value
N	Second comparator's value
i_k	Output current of leg k
$\left[S_k, S_k' \right]$	Switches of leg k
$\left[D_k, D_k' \right]$	Diodes of leg k
e_k	Equivalent source-side voltage source seen from the leg k

I. Introduction

Electrical machines employed in AC motor drive systems are normally fed by Voltage-Source Inverters (VSI). VSIs use dc supplies that in turn are supplied normally by three-phase rectifiers. This type of drive system is sensitive to faults occurring in the rectifier or the inverter. A sudden failure in the power switches decreases system performances and can lead to hard failure. Therefore once a fault occurs, the drive operation has to be halted. This is not desirable in the systems where operation of the drive is of essential importance and continuous operation of the system is mandatory. Examples of such systems are some of processes in the military, aerospace and automotive industries like steering, fuel pumps, and brake-by-wire systems [1], [2].

Therefore, in order to prevent unscheduled shutdown, real-time fault detection and converter reconfiguration schemes for power converters must be implemented.

In order to make a suitable response to an open-switch fault in one of the semiconductor devices or one of the drivers, the first step consists of fast detection of fault and its location. Several papers have discussed fault detection schemes for three-phase power converters. In [3], [4] current-vector is analyzed to identify fault. The use of average motor currents park's vector is suggested in [5] for diagnosing voltage source inverter faults in AC drives. A fuzzy-based approach for the diagnosis of fault modes in a voltage-fed PWM inverter induction motor drive is presented in [6] which is based on the Concordia stator current pattern. Different schemes are proposed in [7] for faster fault detection in voltage-fed PWM motor drive systems. With these techniques the fault is detected in one fourth of the fundamental cycle. A very fast FPGA-based fault detection is presented in [8], [9] that is based on a "time and voltage criterion" and can detect and locate a fault in a few microseconds.

The methods presented in [8], [9] for a back-to-back converter use 6 additional voltage sensors to detect the fault, one per phase. Such methods are general and applicable to different types of fault-tolerant converters with or without redundancy. However, depending on the structure of the fault-tolerant converter, the number of additional sensors might be decreased. Such an approach is interesting because it is evident that using a large number of extra sensors decreases reliability and induces additional costs. A fault-tolerant six-leg converter without redundancy is studied in this paper and a modified detection scheme is presented and tested for it, which uses only 3 voltage sensors and remains as fast as the method presented in the references [8], [9]. To perform very fast fault detection, the fault detection algorithm must be implemented in a very fast digital target. Therefore in the proposed method, the detection algorithm is implemented on a FPGA chip. FPGA can execute these tasks quasi-instantaneously. This characteristic is very useful for fault detection schemes, which will be essential for the continuity of service.

After fault detection, a change in the topology is necessary. Several schemes are proposed as fault tolerant topologies for power converters. Some fault tolerant structures are provided in [10]. In [11] an additional inverter leg replaces the faulty leg by using bidirectional switches. In [1] a hardware reconfiguration is presented that is done by connecting the neutral point of the machine to the middle point of the dc-link capacitor. The proposed hardware reconfiguration presented in [12] is based on the connection of the dc bus middle point to the phase which was linked to the faulty leg before its isolation. A fault tolerant three phase ac/ac converter is proposed for machine-supply application that uses three additional bidirectional switches [13]. In this topology after a fault, the six-leg converter becomes a five-leg converter. This fault-tolerant topology is studied in this paper and, as mentioned before, a dedicated fault detection scheme is proposed for it.

In the following, first the fault tolerant converter topology without redundancy and the improved fault detection approach with reduced extra sensors number are presented. Simulations are carried out to study the effectiveness of this approach. Simulation results for fault detection are presented in part III. Then the fully digital control and the detection principle are implemented on a single FPGA chip. Experimental results are reported in part IV.

II. Fault tolerant converter

II.1. The topology

Fault tolerant six-leg converters have been proposed as fault tolerant topologies for three-phase AC machine or loads [13]. After an open-switch failure in one switch in a fault tolerant six-leg converter, the faulty leg

switching orders are stopped and the suited triac is switched on, changing the topology from six-leg to five-leg converter (See Fig. 1).

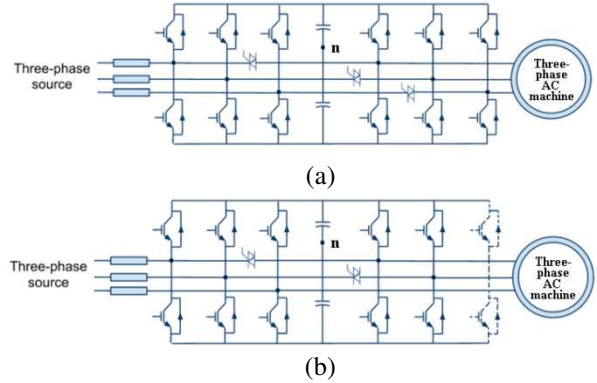


Fig. 1. Six-leg fault tolerant converter (a) before fault (b) after fault occurrence

Before the fault occurrence, when the fault tolerant converter is acting like a conventional six-leg converter, any usual PWM method can be used for its two conventional three-leg converters. After the fault detection and reconfiguration, one leg will be shared between the two sides of the converter and the faulty leg will be disconnected, so the converter will become a five-leg structure. Among the several PWM approaches for this post-fault topology, it seems that the suggested method in [14], [15] that uses all 32 possible voltage vectors of a five-leg converter, produces less voltage harmonics and is simpler and better suited for practical implementation. Therefore this approach is used in this paper. In this method a so called “double zero-sequence injection method” is performed. Fundamental voltage reference signals $v_i (i = a, b, c)$ for both sides of the converter are calculated using methods like field oriented or voltage oriented control. In this paper, reference voltages are calculated to perform the regulation of the dc-link voltage at unity input power factor in the source-side, and to have sinusoidal balanced voltages at the load-side. Then a zero sequence signal (ZSS) is added to these values to form the modulation signals (Eq. 1). In fact ZSS does not change the output line-to-line and phase voltages, therefore it is used as a degree of freedom to reduce the current harmonics and improve the dc-bus utilization [16].

$$v_i(t) = v_i^*(t) + v_{zs}(t) \quad (1)$$

Now since we have 6 voltage references and only 5 legs, a reduction in the number of voltage references is required. This is proposed in [17] using an inverse lookup table. In [15], this is done adding another ZSS in accordance to the converter configuration in five-leg mode. The new set of voltage references are calculated as:

$$\begin{aligned} v_{A1} &= v_{a1} + v_{c2}; v_{B1} = v_{b1} + v_{c2} \\ v_{A2} &= v_{a2} + v_{c1}; v_{B2} = v_{b2} + v_{c1} \\ v_C &= v_{c1} + v_{c2} \end{aligned} \quad (2)$$

Since the same signal is added to all three reference values of a converter, it does not affect the fundamental output voltage. Fig. 2 shows the principle of this method. ZSS injection is repeated for both sets of three phase reference voltages in two sides of the converter, and later using (2), new set of five voltage references are produced and sent to PWM unit, as shown in Fig.2.

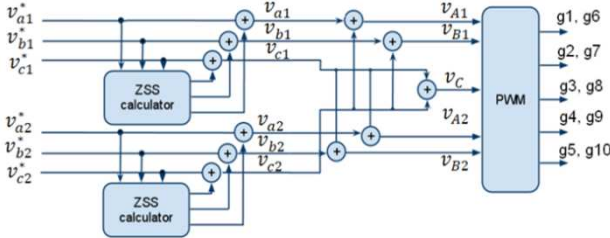


Fig. 2. Principle of the PWM module for a five-leg converter

II.2. Fault detection with reduced number of additional sensors

Very fast fault detection is possible using the aforementioned approach used in [8], [9].

But using this method, 6 additional voltage sensors are needed to measure the so called pole voltages in respect to the dc middle point 'n' [8]. In fact, this number can be reduced for fault detection in the specific case of the proposed six-leg converter case, without redundancy. This is shown in Fig. 3. The proposed detection scheme which is shown in Fig. 3 needs only 3 voltage sensors.

A fault is detected based on the difference between measured and estimated line voltages. Here, open circuit faults are studied, because it can be shown that with a proper setting of very fast acting series fuses, the converter after a short circuit fault will finally end in a situation like the open circuit fault [9]. The estimated voltages are calculated based on the switch commands and the dc-link voltage. For the fault detection scheme with reduced number of additional sensors, they are calculated as below:

$$v_{14es} = (T_1 - T_4)V_{dc} \quad (3)$$

$$v_{25es} = (T_2 - T_5)V_{dc} \quad (4)$$

$$v_{36es} = (T_3 - T_6)V_{dc} \quad (5)$$

while $[T_1 \dots T_6] \in \{0,1\}$. $T_i = 0$ indicates that the switch is commanded to be open, whilst $T_i = 1$ means that the switch is commanded to be closed. The switch commands in each leg are complementary.

Differences between measured (subscript "m") and estimated (subscript "es") values are inevitable because of the errors in measurement and the discretizing process. Also, because of non-ideal behavior of drivers and switches, there will always be delays and dead times, which means that estimated and measured voltages are not always equal, even in normal operation of the converter. Therefore two adjustments have been made: a comparator is used to determine if the difference between measured and estimated voltage is large enough to be

considered as error, and a time criterion is used to take into account delays and dead times in the converter. This is shown in Fig. 4 for the legs k and k+3 ($k=1, 2, 3$). Three detection blocks are needed for the six-leg converter.

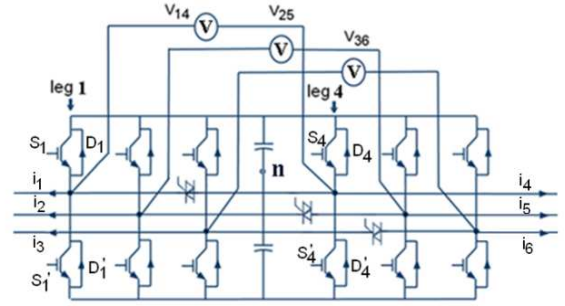


Fig. 3. Modified fault detection scheme

The error signal is observed over the time, and if it is greater than a fixed value (h) for a long enough time (N period), then we can be sure that there is a fault. This observation time should be longer than the overall delay caused by the sensors, drivers, controllers and switches.

For the converter shown in Fig. 3, for all legs, pole voltages ($V_{kn}, k=1,2,\dots,6$) will be either $-V_{dc}/2$ or $V_{dc}/2$. Therefore if the converter is not in normal operation mode, estimated and measured voltages will be different and fault detection will be possible.

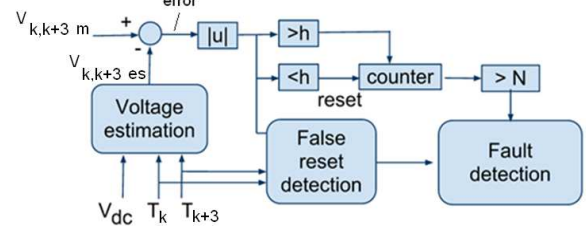


Fig. 4. Fault detection scheme

Positive direction of the currents is defined as exiting from a leg (Fig. 3). For the legs k and k+3 ($k=1, 2, 3$), there are four possible combinations of gate commands. For each case, based on the sign of the currents i_k and i_{k+3} and on the location of the faulty switch, different situations might occur. For example for $T_k T_{k+3} = '11'$, if there is an open circuit fault in S_k and $i_k < 0$, the diode D_k conducts, $v_{kn} = V_{dc}/2$, fault cannot be detected and the converter acts normally. In the contrary, if $i_k > 0$, D_k conducts and fault will be detected. In table 1, different possibilities of faults in $S_k, S_k', S_{k+3}, S_{k+3}'$ are provided. Only the cases where the converter is acting abnormally are shown, when the diode of the complementary switch is conducting instead of the faulty switch. When an output current i_k is zero when the fault occurs, 3 cases might occur, based on the other legs conditions. For example for $i_1 = 0$ and $T_2 T_3 = '00'$, it can be shown that if $e_1 > 2/3V_{dc}$, then D_1 will conduct and D_1' will be reverse biased, for $0 < e_1 < 2/3V_{dc}$ both

diodes will be off and for $e_1 \leq 0$, D_1' will conduct and D_1 will be reverse biased [8]. Similar studies can be made for other possible cases. Therefore it can be said that in all cases either the converter will continue to work normally, or a fault can be detected.

However in the contrary to the scheme of [8], [9], here different faults may result in the same measured voltage because of reduced extra-sensor number. For example for $T_k T_{k+3} = '10'$, $i_k > 0$ and $i_{k+3} < 0$, fault in S_k or S_{k+3}' will lead to $V_k V_{k+3} = 0$ as shown in Fig.5. Therefore, although detection of the fault is possible, its location will be unknown. All possible states are shown in table 1. The error signals are calculated from measured and estimated values and are summarized in table 2. One can see that for $T_k T_{k+3} \in \{00, 11\}$, there is no problem in finding the location of the fault because the “error” is different for each case. However for $T_k T_{k+3} = '01'$ (with $i_k < 0$, $i_{k+3} > 0$) or $T_k T_{k+3} = '10'$ (with $i_k > 0$, $i_{k+3} < 0$), the location of the fault cannot be detected (because of the same “error” values). Indeed, the inability to detect the fault’s location is not important. Since we have detected that one of these two legs are faulty, the corresponding triac between these two legs will be switched on. Therefore, exact knowledge of the faulty switch is not necessary. After converter reconfiguration, the legs k and $k+3$ will make a shared leg that acts as the so-called common leg of the five-leg converter.

There is one particular case compared to conventional schemes with 6 sensors that should be taken care of. The measured voltage between two corresponding legs depends on the switching pattern of both. Consequently, it should be noted that detection of a fault in one leg might be perturbed because of possible switching commands in the other leg during fault detection. For example, consider that S_k is faulty and instead of that, D_k' is conducting. S_{k+3}' is also switched on. The up-counter’s output (see Fig. 4) starts to increase, but if the command of the leg $k+3$ is changed before the fault detection, the error between measured and estimated voltages will switch to zero and a reset signal will be applied to the counter, even though the fault remains. To prevent this, a “false reset detection” a specific block is designed to check if the reset signal was applied during an increment in counter and just after the switching command. If this is the case, one can be sure that a fault has occurred. Using this modification has also another advantage, that the fault might be detected faster than the original method of [8], [9], when a switching command occurs during fault detection.

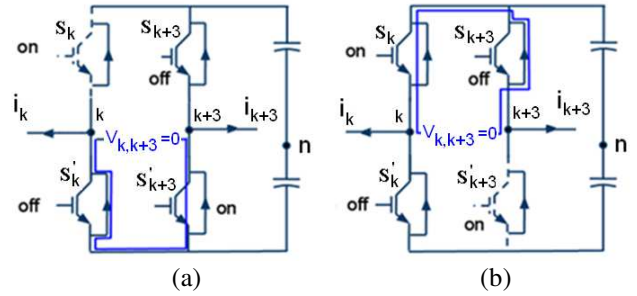


Fig. 5. Measured voltage when $T_k T_{k+3} = '10'$; (a) fault in S_k ; (b) fault in S_{k+3}'

TABLE I
MEASURED VOLTAGE IN NORMAL AND FAULTY CONDITIONS

T_k	T_{k+3}	normal	Fault in S_k	Fault in S_k'	Fault in S_{k+3}	Fault in S_{k+3}'
		estimated	measured			
0	0	0	0	V_{dc}	0	$-V_{dc}$
0	1	$-V_{dc}$	$-V_{dc}$	0	0	$-V_{dc}$
1	0	V_{dc}	0	V_{dc}	V_{dc}	0
1	1	0	$-V_{dc}$	0	V_{dc}	0

TABLE II
ERROR BETWEEN MEASURED AND ESTIMATED VOLTAGES IN FAULTY CONDITIONS

T_k	T_{k+3}	Fault in S_k	Fault in S_k'	Fault in S_{k+3}	Fault in S_{k+3}'
		Error ($V_{k,k+3} - V_{k,k+3}^{es}$)			
0	0	0	V_{dc}	0	$-V_{dc}$
0	1	0	V_{dc}	V_{dc}	0
1	0	$-V_{dc}$	0	0	$-V_{dc}$
1	1	$-V_{dc}$	0	V_{dc}	0

III. Simulation results

Simulations are performed in order to validate the high performance of the proposed fault detection scheme and fault tolerant converter. MATLAB/ Simulink is used for simulation. For control of the converter, as stated earlier, three-phase voltages at the source side are controlled to provide the ability of dc-link voltage regulation at unity input power factor. This is done using a well known source-voltage oriented control method for three phase controlled rectifiers [16]. Voltage references at the load-side are balanced sinusoidal values. Two sets of voltage references obtained from these control schemes are sent to the appropriate six-leg or five-leg PWM block, based on the state of the converter. PWM block for a five leg converter has a preprocessing unit as stated in (1), (2).

Input inductance of 3 mH is used between the converter and the source. A 2200 μ F capacitor is used in the dc-link. Switching frequency is equal to 8 KHz. An open-circuit fault is introduced in one of the semiconductor switches in order to evaluate the response of fault detection scheme and to validate the

effectiveness of fault tolerant converter.

Fault is occurred at time $t = 0.5s$ in the leg ‘6’ in the inverter side. The goal is mainly to evaluate the fault detection capability, but also to test the performance of the fault tolerant converter, and the implementation of control schemes on the FPGA. Fig. 6 shows the moment of fault occurrence and detection, and also the output of the counter in the corresponding detection unit. A large detection time of $30\mu s$ is selected in order to take into account all delays in the system. Fig. 7 and Fig. 8 show the load currents and dc-link voltage respectively. It is clear that the fault is detected very fast. Therefore, it is evident that the proposed fault detection method performs well.

Simulation results show that the fault detection and control is in fact very effective. The fault detection is fast and robust, and the control of the converters before and after fault occurrence is well performed. Now the next step will be the fully-experimental verification of these results.

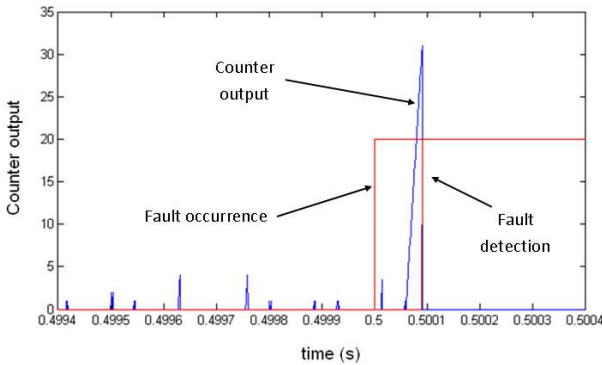


Fig. 6. Fault occurrence (at 0.5s) , and detection

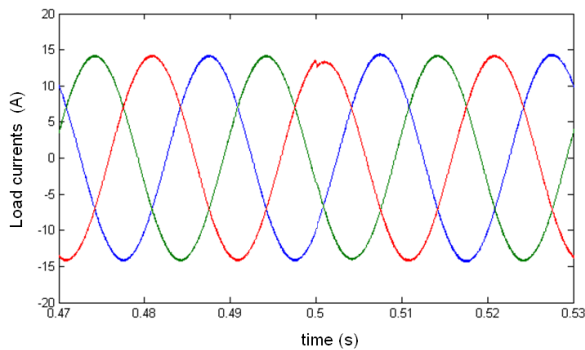


Fig. 7. Load currents (fault at 0.5s)

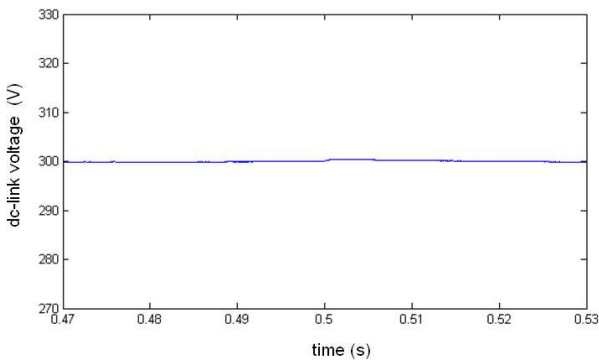


Fig. 8. dc-link voltage (fault at 0.5s)

IV. Experimental results

For experimental test, a setup is built in our laboratory. Two three-phase converters and three triacs form the fault-tolerant converter. Parameter values are the same as reported in part III. A three-phase RL load is supplied via this fault-tolerant converter. The experimental setup is shown in Fig. 9.

For very fast detection, the fault detection algorithm must be implemented in a very fast digital target. Therefore in the proposed method, like the methods of [8], [9] the detection algorithm is implemented on a FPGA. FPGA can execute the tasks quasi-instantaneously. This characteristic is very useful for fault detection schemes, which will be essential for fault tolerant operation. In order to minimize the cost and to increase the efficiency, control schemes are also implemented on this FPGA. Effectiveness of FPGA for control of power-electronic converters has been demonstrated in [18]-[21].

In our experiments, a Stratix DSP S80 development board is used, which includes the Stratix EP1S80B956C6 FPGA chip. This chip contains 79,040 programmable logic elements. The development board has an on-board 80-MHz oscillator.

An open circuit fault is introduced in the leg “6” in the inverter side. Fig. 10 shows the currents of the phase “c” of the load and the phase “a” of the source. It is clear that even after a fault in one of the semiconductors, the load is still supplied with the desired currents.

Fig. 11 shows the moment of fault detection, the detection counter’s output and the dc-link voltage waveform before and after the fault occurrence. It is clear that the fault is detected very fast, and the effect of fault on the dc-link voltage is negligible. Note the low-amplitude changes in the counter’s output that are due to delays in the control and measurement. Having defined a sufficiently large band (N) in the detection unit, these spikes are not considered as a fault, and therefore robustness of the fault detection method against false-alarms is achieved.

Clearly fault detection and reconfiguration is done in a very suitable manner. Fault detection was very fast, so the effect of fault on drive’s operation is negligible. In this way, one can be sure that a semiconductor fault will not harm other mechanical or electrical parts of the drive. Also the number of additional voltage sensors for fault detection is reduced, therefore the cost is decreased and the reliability is improved in comparison with the original scheme.

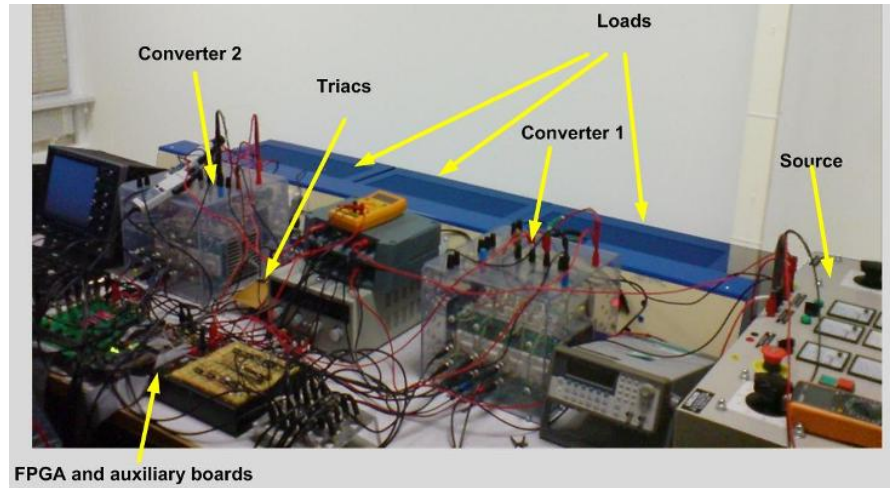


Fig. 9. Experimental setup

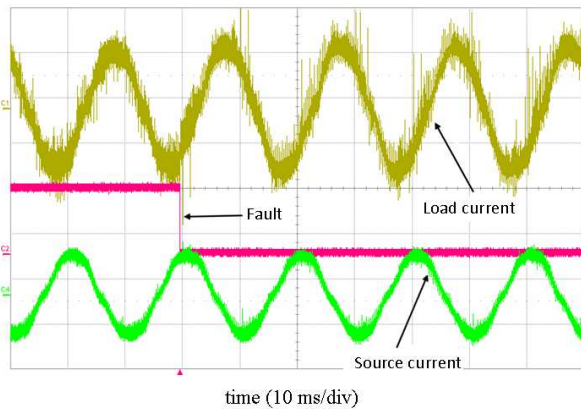


Fig. 10. From top to bottom: load current (2 A/div), fault, source current (5 A/div)

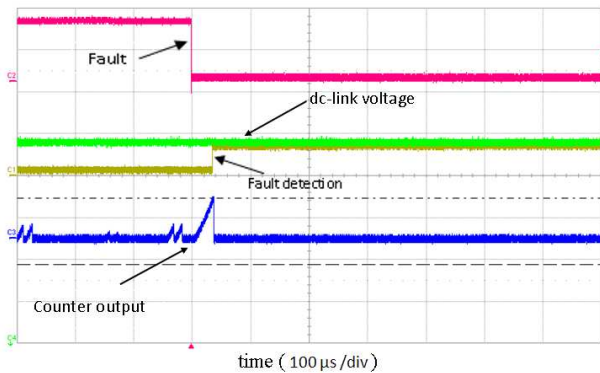


Fig. 11. From top to bottom: fault, dc-link voltage (50 V/div), fault detection, counter output

V. Conclusion

In this paper a modified fault detection for a six-leg fault tolerant converter without redundancy is proposed that minimizes additional voltage sensors. This fully digital robust and fast detection scheme uses only three voltage sensors instead of six. Detection unit is modified in respect to the original method to be able to detect faults effectively.

Simulations are performed to evaluate the effectiveness of the detection scheme and fault tolerant

structure. Then fully experimental tests are carried out and the high performance of the detection scheme and fault tolerant structure is validated. Both Fault detection and control units are implemented on a single FPGA chip to verify the effectiveness of the detection scheme and fault tolerant structure. It is shown that very fast detection is possible. Also after reconfiguration, desirable control of the source-side, load-side and dc-link voltages is achieved.

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