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► **To cite this version:**

Shahram Karimi, Philippe Poure, Shahrokh Saadate. FPGA in the Loop Prototyping Methodology for Fully Digital Power Electronics System Control Design. *International Review of Electrical Engineering*, 2008, 3 (2), pp.281-288. hal-03568520

HAL Id: hal-03568520

<https://hal.univ-lorraine.fr/hal-03568520>

Submitted on 13 Feb 2022

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FPGA in the Loop Prototyping Methodology for Fully Digital Power Electronics System Control Design

S. Karimi¹, P. Poure², S. Saadate¹

Abstract – This paper presents a methodology to design and prototype FPGA-based fully digital controller for power electronics systems. A Top-down design methodology is used to study step by step the digital adaptation and the fully digital implementation of the control algorithm. Finally, “FPGA in the loop” prototyping is achieved, based on MATLAB/SimPower Systems and Altera DSP Builder computer aided design tools. Modeling, simulation and FPGA in the loop prototyping are achieved in a unique design environment. An application using the proposed methodology is studied: a fully digital controller for a three-phase parallel active power filter. The fully digital controller implementation is described and the hardware digital controller experimentally validated by FPGA in the loop prototyping.

Keywords: Field Programmable Gate Array (FPGA), Design methodology, fully digital controller, industrial power control system

Nomenclature

i_c	Load current
v_s	Supply voltage
v_{dc}	DC voltage
L_s	Mains inductance
R_s	Mains resistance
L_c	Load AC inductance
R_c	Load AC resistance
L	Load inductance
R	Load resistance
L_f	Active filter inductance
R_f	Active filter resistance
ω_c	Cut-off frequency of the multi variable filter
T_s	Sampling period
x_α, x_β	Multi variable filter input signals (current/voltage) in $\alpha\beta$ axis
$\hat{x}_\alpha, \hat{x}_\beta$	Multi variable filter output signals (fundamental components of the x_α and x_β)
$i_{h\alpha}, i_{h\beta}$	Harmonic components of the load currents in $\alpha\beta$ axis

I. Introduction

The amount and complexity of digital controller for power electronic systems is continually increasing. Consequently, more and more efforts are dedicated to the digital controller design, verification and simulation with the controlled power system. More, fast recent progress of integration technology and electronic design automation techniques allow the development of

complex and compact high performance integrated controllers for industrial electronic systems. For example, with the advance of Field Programmable Gate Array (FPGA) devices and Integrated Circuits (IC) technology, fully digital controllers can be implemented in only one digital circuit [1], [2]. Consequently the number of control system components is reduced and thus the control circuit is very compact. Also, the use of FPGA components for hardware prototyping allows faster design and changes can be made without penalty [3]. However, a suited methodology must be used to perform a reliable design and realize satisfactory time to market. Traditional software based simulation has the disadvantage of being unable to exactly replicate real operating conditions. It does not take into account the limitations of the digital controller, like saturation of values in fixed point during the intermediate calculations and the finite resolution of registers. Also, in virtual prototyping of digital controllers based on mixed simulation tools using VHDL-AMS language [4] and/or ModelSim tool [5], the real controller is not experimentally tested.

One way to bridge the gap between the simulation and real conditions is Hardware-In-the-Loop simulation (HIL or HILS) [6]. This solution increases the realism of the simulation while eliminating the risk of damaging the actual drive or plant. However, the digital controller remains still simulated. Recently, many papers have been published on Real-Time Hardware-In-The Loop (RT-HIL) simulation used for the design and testing of electric drives and power electronic systems [7]. In RT-HIL simulation, a real-time simulator simulates the drive or plant. However, real-time simulators are usually not fast enough to simulate Insulated Gate Bipolar

Transistor (IGBT) power electronic systems and if they are, their cost is prohibitive [8].

This paper presents a new design methodology based on FPGA rapid prototyping for controllers of power electronics systems; in this method, the fully digital controller is implemented in only one FPGA. A new “FPGA in the loop” prototyping method is introduced to test experimentally the hardware digital controller. The FPGA target (implementing the fully digital controller) communicates with the simulated power plant. By this way, we take into account the limitations of the FPGA-based controller and the additional cost is null.

First, this paper describes the design methodology and detail the required software. Then, a power application case illustrates the proposed methodology.

II. Power Electronics System

Conventional power electronics systems consist of a complex assemblage of individual components with a variety of different functionalities. They mostly consist in power elements (plant), controller, sensors and interfaces (see Fig. 1). Source, converter and load are the major power elements. Sensors mostly consist in electrical (voltage or current) or mechanical sensors. Plant and controller are usually connected in closed loop by sensors sending feedback signals from the plant to the controller.

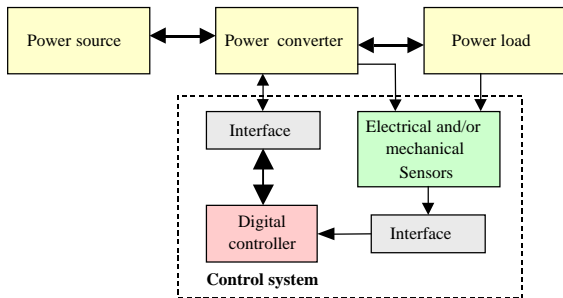


Fig. 1. Components of conventional power electronics systems.

III. Required Software

Digital signal processing (DSP) system design in Programmable Logic Devices (PLDs) as FPGA requires both high-level algorithm and hardware description language (HDL) development tools. The Altera DSP Builder is a software which integrates these tools by combining the algorithm development, simulation and verification capabilities of the Matlab/Simulink system-level design tools with VHDL (Very high speed integrated circuits Hardware Description Language) design flow, including the Altera Quartus II software. The Quartus II software provides a comprehensive design, synthesis, and analysis environment for PLDs applications. DSP Builder allows creating the hardware representation of the required digital signal processing

functions using Matlab/Simulink user-friendly algorithm-development environments, for shorter design and implementation cycles. Matlab functions and native Simulink blocks can be combined with Altera DSP Builder library blocks to create FPGA designs which can be simulated under Simulink. For automated design flow, the “Signal Compiler” block, which is at the core of DSP Builder, can generate VHDL code and scripts for Quartus II-based synthesis and fitting from within Simulink.

Furthermore, the DSP Builder “FPGA in the Loop” block enables chip programming for experimental hardware–software validation.

IV. Top-Down Design Flow

The designer can proceed using Top-Down methodology, first performing conceptual studies using conventional simulation, and then continually refining the digital controller design using simulation and finally testing the design by “FPGA in the loop” prototyping. Fig. 2 shows the proposed system-level design flow.

IV.1. Conventional Simulation

To define the system specifications and validate the functionality of the control system, conventional simulation tools can be used.

The power circuit (plant) can be modelled using the MATLAB/SimPower Systems toolbox. The sensors, the interfaces and the control system can be modelled using Simulink. At this step of the design flow, the system is first modelled in continuous-time mode. Then it can be modified and converted in discrete-time mode.

Non-linear switching topologies such as IGBT inverter model with switching frequency of several kHz, need very tiny time-steps to attain acceptable accuracy [6]. Thus to attain acceptable simulation accuracy, time-step for the plant model must be usually selected equal or smaller than 1 μ s.

IV.2. Mixed Simulation

In mixed simulation, the power plant, the sensors and the interfaces models remain the same as the ones used in the conventional simulation, described in previous section. However, the control system blocks (Simulink models) must be removed and replaced by Altera DSP Builder library blocks, in the same Simulink environment. In this case, Simulink signals must be converted to fixed-point binary signals. The fixed-point binary format, noted $[s, m_i, m_d]$, is defined with s the bit sign, m_i the bit numbers of the integer part, and m_d the bit numbers of the decimal part. The bit number of the input signals is limited by Analog to Digital (A/D) specifications. However, the bit number for the intermediate blocks must be chosen lower than 51 bits because of the Altera DSP Builder limitation. The small

value increases the calculation errors and can lead to the saturation, furthermore the big value increases execution time and uses high FPGA chip resources. Fig. 3 shows the general mixed simulation environment for conventional power electronics systems.

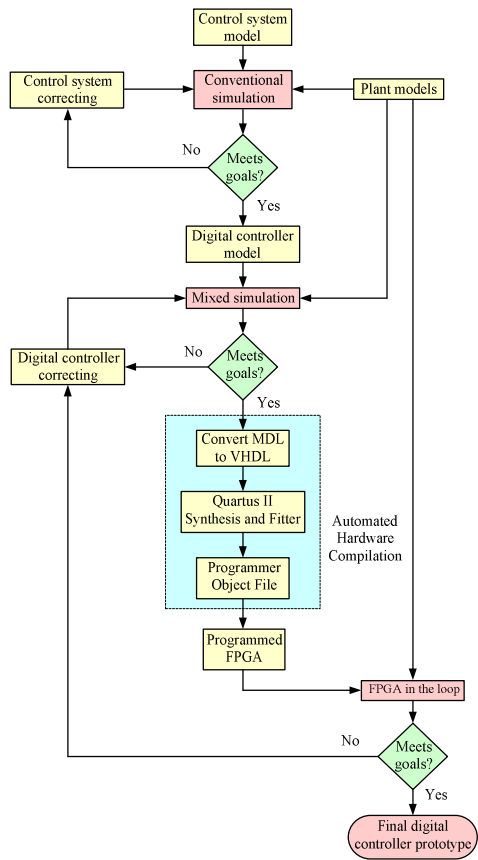


Fig. 2. System-level design flow.

The sampling period of the control system depends on the system requirements and specifications. However in “FPGA in the loop” prototyping, the sampling period must be selected equal to the minimum time-step used in Simulink models for synchronisation of signals between Simulink and DSP Builder models.

At this step of procedure, the designed system can be evaluated by mixed simulation.

IV.3. “FPGA in the Loop” Prototyping

The VHDL code of the control system can be generated from the Altera DSP Builder library blocks by the DSP Builder “Signal Compiler” tool. Then the VHDL code is synthesised and fitted automatically with Altera Quartus II software. At this step of the procedure, the reports files must be checked for any error or warning. After debugging if necessary, we can put the DSP Builder HIL block into the design environment and remove all control system blocks. Since, the VHDL code is implemented into FPGA. After connection of the Simulink input and output signals to the DSP Builder HIL block, the “FPGA in the loop” prototyping can be

run. In this step, if the “FPGA in the loop” prototyping results are not correct or the goals don’t meet, the control system design must be modified.

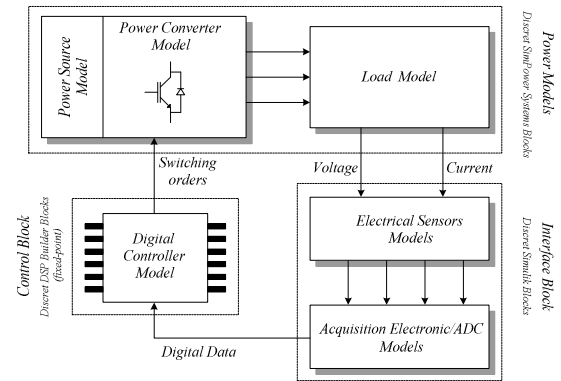


Fig. 3. Mixed simulation environment.

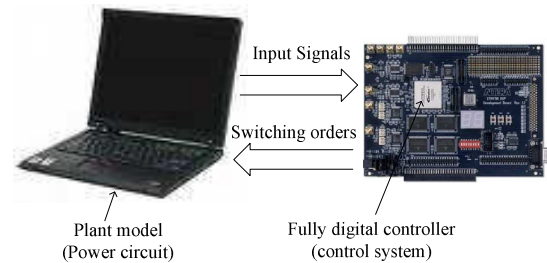


Fig. 4. “FPGA in the loop” principle.

In “FPGA in the loop” prototyping (see Fig. 4), at each time step, the plant model is simulated using Matlab/SimPower Systems and then the Simulink output signals are exported to the FPGA. When the FPGA receives the signals from Simulink, it executes the implemented program for one sample interval. The FPGA returns the switching orders, computed during this step, to Simulink. At this point one sample cycle is performed. In this case, the FPGA prototyping board is connected to a PC via a Joint Test Action Group (JTAG). This interface performs communication between the digital control system (implemented into the FPGA prototype) and the plant (emulated by Matlab/SimPower Systems).

V. Application Example

An example of FPGA-based fully digital controller experimentally validated using “FPGA in the loop” prototyping is described in this section. A power application, three-phase parallel active power filter, was chosen to be designed. Active power filters are proposed as means of removing the current harmonics. Current harmonics produced by non-linear loads are effectively prevalent in today’s power systems. They interfere with sensitive electronics equipment and cause additional power losses. Active power filters produce a nearly sinusoidal supply current by measuring the harmonic

currents and then injecting them into the power system with a 180° phase shift.

V.1. System Configuration

Fig. 5 shows the studied three-phase parallel active power filter system configuration [9]. It is composed of a three-phase parallel active power filter, a grid and a non-linear load. The parallel active power filter consists of a three-phase voltage source inverter, three equal series inductances L_f with resistances R_f and a DC capacitor. The non-linear load is a three-phase diode rectifier feeding (R, L) load. The grid is balanced with equal series resistances R_s and inductances L_s for each phase. The specifications of the power system are given in the Table I. The output currents of the active filter are controlled to provide in real time harmonic currents generated by the non-linear load to ensure filtering. The control system of the active filter is depicted in the Fig. 6. The control system consists in an Analogue/Digital unit and a FPGA-based fully digital controller.

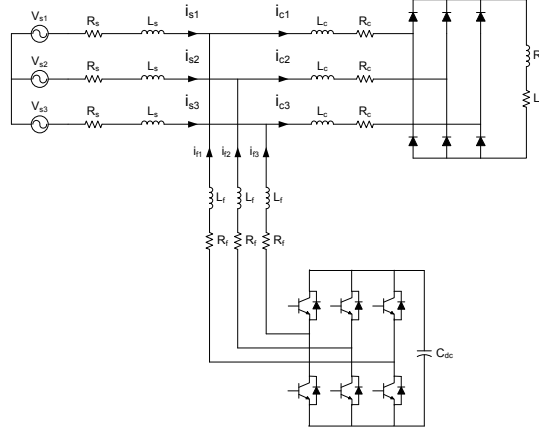


Fig. 5. System configuration with active filter.

TABLE I
SPECIFICATIONS OF THE STUDIED SYSTEM

Load power	6 kW
Mains voltage	400 V
Mains frequency	50 Hz
Mains inductance (Ls)	0.1 mH
Mains resistance (Rs)	0.2 mΩ
Load AC inductance (Lc)	0.8 mH
Load AC resistance (Rc)	0.27 mΩ
Load inductance (L)	40 mH
Load resistance (R)	48.6 Ω
Filter inductance (Lf)	3 mH
Filter resistance (Rf)	5 mΩ
DC capacitor (Cdc)	1100 μF
DC voltage reference	700 V

V.2. Control Strategy

Fig. 7 shows the block diagram of the digital controller. This controller consists in a harmonic isolator and a current controller. Both are programmed in only one FPGA. The harmonic isolator determines the current references which must be generated by the active filter. The current references are identified using a modified version of instantaneous active and reactive power method [9], associated with two digital voltage and current multi variable filters [10]. The current controller is used to control the switches (S_1 - S_6) of the voltage source inverter. This controller is a modulated hysteresis current controller [11]. It allows the operation of the voltage source inverter at fixed frequency with the robustness properties of an hysteresis controller.

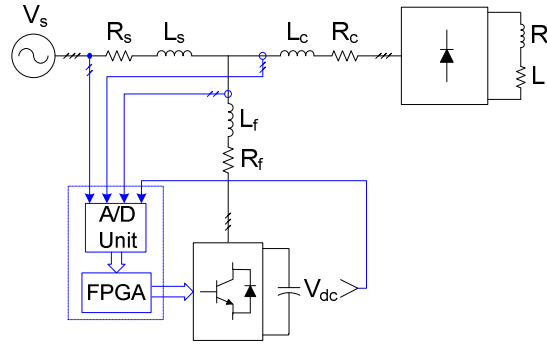


Fig. 6. FPGA-based digital controller.

A) Harmonic Isolator

The harmonic isolator separates the harmonic currents from the fundamental component of the load current so the current references can be calculated.

Fig. 8 shows the principle of the harmonic isolator. In this part, the classical Concordia transformation is used to transform the three-phase load currents (i_{c1} , i_{c2} and i_{c3}) and supply voltages (v_{s1} , v_{s2} and v_{s3}) to the two-phase load currents ($i_{c\alpha}$ and $i_{c\beta}$) and the supply voltages ($v_{s\alpha}$ and $v_{s\beta}$).

The harmonic components directly extract from the $\alpha\beta$ axis by using multi-variable filters, as given by the following expressions:

$$\hat{x}_\alpha = \frac{k}{s} [x_\alpha(s) - \hat{x}_\alpha(s)] - \frac{\omega_c}{s} \hat{x}_\beta(s) \quad (1)$$

$$\hat{x}_\beta = \frac{k}{s} [x_\beta(s) - \hat{x}_\beta(s)] + \frac{\omega_c}{s} \hat{x}_\alpha(s) \quad (2)$$

Thanks to the voltage multi-variable filter, the active filter control completely immunises against the voltage harmonics. The current multi-variable filter is employed as a high pass filter without generation of phase delay [10].

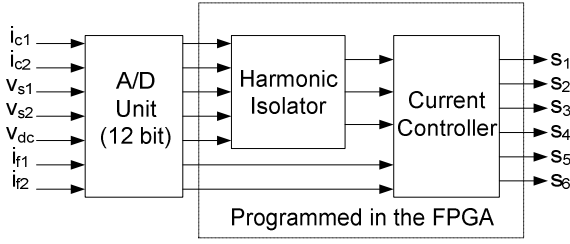


Fig. 7. Block diagram of the digital controller.

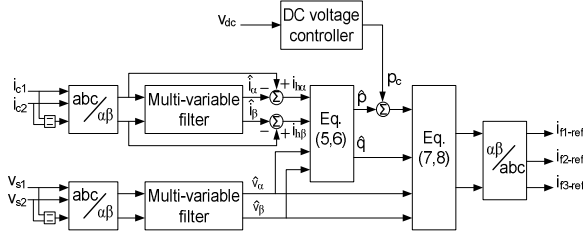


Fig. 8. Principle of the harmonic isolator.

By applying the zero-order hold transformation, the equations (1) and (2) can be transformed into the following discrete time format:

$$\hat{x}_\alpha = (1 - kT_s)Z^{-1}\hat{x}_\alpha + kT_sZ^{-1}x_\alpha - \omega_c T_s Z^{-1}\hat{x}_\beta \quad (3)$$

$$\hat{x}_\beta = (1 - kT_s)Z^{-1}\hat{x}_\beta + kT_sZ^{-1}x_\beta + \omega_c T_s Z^{-1}\hat{x}_\alpha \quad (4)$$

In the Fig. 9 the digital multi-variable filter is presented. Alternative component of the instantaneous real and imaginary power are identified by:

$$\hat{p} = \hat{v}_\alpha i_{h\alpha} + \hat{v}_\beta i_{h\beta} \quad (5)$$

$$\hat{q} = -\hat{v}_\beta i_{h\alpha} + \hat{v}_\alpha i_{h\beta} \quad (6)$$

After adding the active power required for regulating DC bus voltage, p_c , to the alternative component of the instantaneous real power, \hat{p} , the current references in the $\alpha\beta$ axis are calculated as follow:

$$i_{f\alpha}^{ref} = \frac{v_\alpha}{v_\alpha^2 + v_\beta^2} \hat{p}_c - \frac{v_\beta}{v_\alpha^2 + v_\beta^2} \hat{q} \quad (7)$$

$$i_{f\beta}^{ref} = \frac{v_\beta}{v_\alpha^2 + v_\beta^2} \hat{p}_c + \frac{v_\alpha}{v_\alpha^2 + v_\beta^2} \hat{q} \quad (8)$$

The three-phase current references are finally computed by transforming the equations (7) and (8) into three-phase reference frame by using the inverse Concordia transformation.

B) DC Voltage Control

The active filter does not require any external DC power supply, because it can build up the DC voltage across the capacitor by itself. The DC voltage controller consists of a proportional controller and a first order low-pass filter used to eliminate the DC voltage ripples. The transfer function of this controller is given as follows:

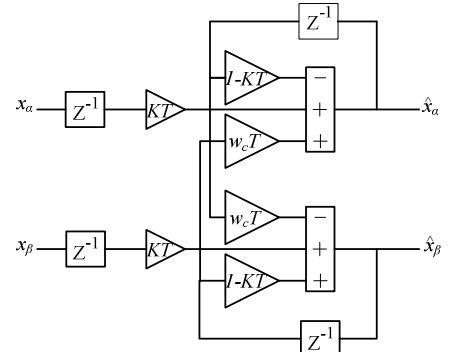


Fig. 9. Block diagram of the digital multi-variable filter.

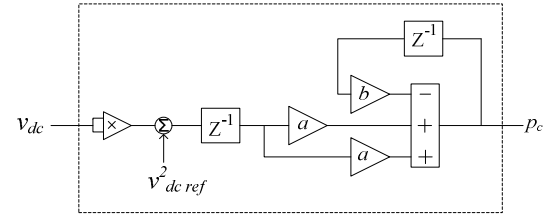


Fig. 10. Digital DC voltage controller.

$$H(s) = \frac{k_c}{1 + \tau_c s} \quad (9)$$

Where k_c and τ_c respectively represent the proportional gain of the controller and the time-constant of the first order filter.

By applying the bilinear “transformation of Tustin”, the transfer function of the DC voltage controller is transformed into the following discrete time format:

$$H(Z) = \frac{a + aZ^{-1}}{1 + bZ^{-1}} \quad (10)$$

$$\text{Whit } a = \frac{T_s k_c}{T_s + 2\tau_c} \quad \text{and} \quad b = \frac{T_s - 2\tau_c}{T_s + 2\tau_c}$$

In the Fig. 10, the digital DC voltage controller is presented.

C) Modulated Hysteresis Current Controller

The conventional hysteresis controllers are generally used for their robustness and simplicity. In fact, these controllers ensure the current control of the static converters without any necessity of the knowledge of the load model and its parameters. Its disadvantage is that the converter switching frequency is variable. Modulated hysteresis current controller allows the operation of the voltage source inverter at fixed frequency with the robustness properties of a hysteresis controller [11]. In this current controller, the modulated reference signal, $i_{ref.ms}$, is deduced from the sum of the reference current and a triangular carrier signal whose frequency is equal to the desired switching frequency. This modulated reference signal constitutes then the new reference of a classical hysteresis controller. The principle of this controller is shown in Fig. 11.

The triangular carrier is generated in digitally form by a n-bit up-counter as is shown in Fig. 12. The up-counter is clocked by a clock with T_s sampling time. Thus, the n-bit up-counter with signed binary fractional format (1 bit for the integer part and n-1 bits for the fractional part) generates a periodic ramp signal with amplitude of 1 and period time of $2^n \times T_s$. For the generation of the triangular carrier signal with an amplitude A_{tr} the absolute value of the up-counter output is multiplied by $-2 A_{tr}$ and then the result is added to A_{tr} .

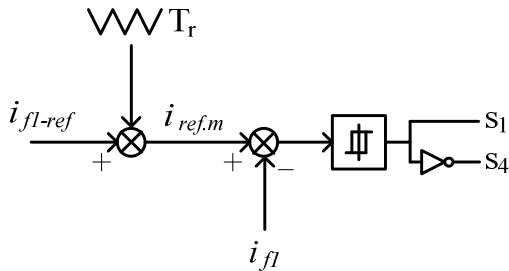


Fig. 11. Scheme of the modulated-hysteresis controller.

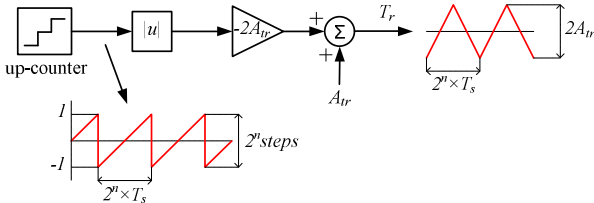


Fig. 12. Principle of the triangular carrier signal generator.

V.3. "FPGA in the Loop" Prototyping

The active power filter and its digital controller were designed and modeled using the proposed methodology. However, only the final "FPGA in the loop" results are presented. Fig. 13 shows the experimental setup.

A Stratix DSP S80 development board, which comprises the Stratix EP1S80B956C6 FPGA chip, has been used to implement the digital controller. This FPGA contains 79,040 programmable logic elements, 679 user I/O pins, 12 reconfigurable fast PLLs and approximately 7.4 Mb RAM. Also, this development board has an on-board 80-MHz oscillator. The three-phase digital implementation of the harmonic isolator and the current controller in the FPGA chip uses 26% of its resources.

The sampling frequency and time-step have been selected equal to $0.25 \mu s$. With this sampling period and selecting of a 8-bit up-counter, high resolution triangular carrier signal is produced with the frequency of 15.625 kHz. Furthermore, this high sampling frequency reduces the level of current overshoot from the hysteresis limits used in the current controller.

The plot shown in Fig. 14 represents the source current for the phase 1 without active filter. In this case, the Total Harmonic Distortion (THD) is 28.04 %. Fig. 15-17 illustrate the "FPGA in the loop" prototyping

results for the active filter and source currents and the DC voltage across the capacitor after the active filter connection. In this case, THD is improved down to 1.27 %.



Fig. 13. Experimental setup.

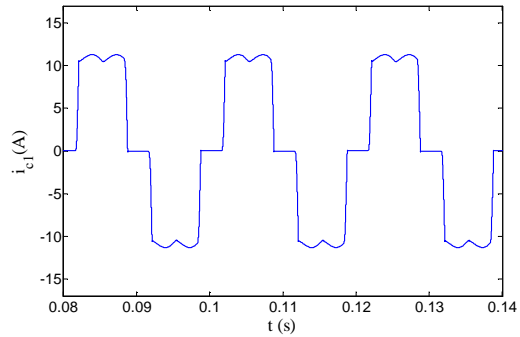


Fig. 14. Phase 1 source current without active filter.

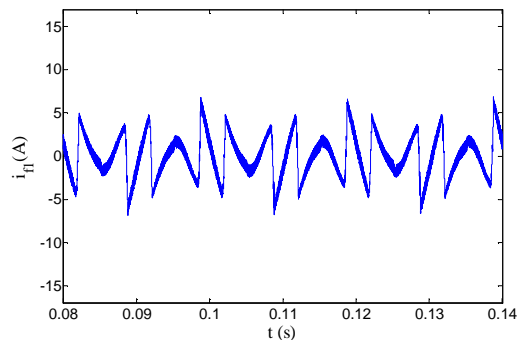


Fig. 15. Phase 1 filter current.

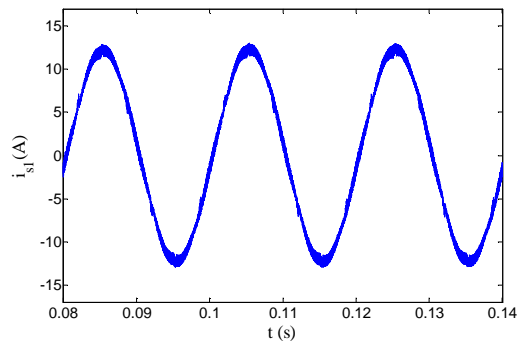


Fig. 16. Phase 1 source current with active filter.

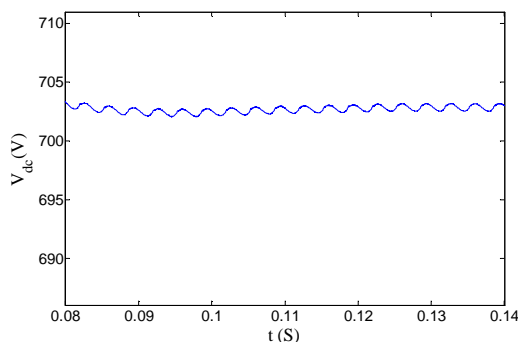


Fig. 17. DC bus voltage.

VI. Conclusion

In this paper, we have presented a Top-down methodology to design FPGA-based fully digital controller for power electronics systems. This methodology uses “FPGA in the loop” prototyping experimental setup. We either used an unique environment for modelling, simulation, experimental validation and design of the digital controller for power electronics systems. The proposed methodology allows fast design development time and short time to market. More it takes into account the limitations of the FPGA-based digital controller, like saturation of values in fixed point during the intermediate calculations and the finite resolution of registers. The design of a digital controller for a three-phase active power filter has been used to illustrate and validate our methodology design flow. “FPGA in the loop” prototyping can be very effective to evaluate the control design especially when the sampling period is very small.

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Authors’ information

¹Groupe de Recherches en Electrotechnique et Electronique de Nancy UMR 7037, Nancy-Université, CNRS - Faculté des Sciences et Techniques - BP 239 - 54506 Vandoeuvre Cedex - France

²Laboratoire d’Instrumentation Electronique de Nancy EA 3440, Nancy-Université- CNRS - Faculté des Sciences et Techniques – BP 239 - 54506 Vandoeuvre Cedex - France



Shahram KARIMI was born in Kermanshah, Iran, in 1972. He received the B.S. degree in electrical engineering from Tabriz university, Tabriz, Iran, in 1995, the M.S. degree in electrical engineering from Sharif university, Tehran, Iran, in 1997. He joined the Gharb High Education and Research Institute, Kermanshah, Iran, in 1999, and is currently pursuing the Ph.D. degree in the GREEN-UHP, Nancy, France. His research interests are active power filters, power quality and fault tolerant converters.



Philippe POURE was born in 1968. He received the Engineer Degree and Ph.D. Degree in Electrical Engineering from INPL-ENSEM-GREEN, France, in 1991 and 1995 respectively. Since 1995, he is an Associate Professor and worked first at the University Louis Pasteur of Strasbourg, France, in the field of mixed-signal System-On-Chip for control and measurement in Electrical Engineering. Since September 2004, he joined the University Henri Poincaré – Nancy I, France and works on power quality, more particularly on active filtering and wind energy conversion systems.



Shahrokh SAADATE was born in Teheran/IRAN on May 6th, 1958, received his engineer degree in 1982, his Master of research in 1982, his PHD thesis in 1986 and his “Habilitation à diriger des recherches” in 1995 from INPL-ENSEM Nancy, FRANCE. Currently, he is Professor in Electrical Engineering in the University Henri Poincaré – Nancy I, France, GREEN laboratory. His main research domains are power electronics and systems, power quality and wind energy conversion.