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Symmetric Wide-Input-Voltage Range Boost Z-Source DC-DC Converter with Reduced Current of Source and Active Components

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Abstract—This study proposes a new enhanced boost DC/DC converter with high voltage boost ability. The proposed converter takes advantage of a continuous source current with negligible ripple, and the start-up inrush current is limited as well. Compared with the traditional extended switched boost DC-DC converter, this converter generates higher output voltage while the numbers of components in the Z-source network of both converters are the same. Moreover, the peak values of the currents provided by the input source and crossing the active-devices are reduced. In addition, the ripples of the previously mentioned currents are noticeably decreased in this topology; thus, the losses are reduced. In this research, the operation principles in continuous conduction mode and discontinuous conduction mode, the voltage gain, and the parameters design of the proposed converter are analyzed. Finally, by presenting the simulation and experimental results, the performance of the proposed converter is assessed.

Keywords— DC-DC converters, Z- source, current stress, voltage stress, boost converter.

I. INTRODUCTION

It is common practice to use a DC-DC converter to regulate and magnify the un-regulated low voltage output of some renewable energy sources like photovoltaics (PV). Thanks to the higher boost factor of the impedance source converters, these circuits can be utilized as an alternative to the conventional boost converters. In this regard, various structures of impedance source converters have been proposed by authors. The structures can be classified in three distinct categories, as proposed in [1]: using magnetically coupled inductors/transformers [2-5], improving and expanding the impedance network [6-18], and using extra active switches in the impedance network [19]. All these structures aim to achieve some of the following benefits: higher voltage gain, less inrush current, less stress on devices, higher efficiency and higher power density. Using coupled inductors, which leads to some particular structures like A-source, Γ -source, Δ -source, Y-source converters, is a fine method for increasing the voltage gain [2-4]. Another appropriate method that provides high voltage gain is utilizing the isolated high step-up DC-DC converters [5]. However, the energy stored in the leakage inductance of their transformers results in electromagnetic interference problems, high voltage stress and high switching losses.

In the literature, it has been proposed to use switched-inductor cells [6]-[12] or add extra components to the Z-source

network [13]-[17] to achieve a higher voltage gain. The switched-inductor/capacitor topologies [6]-[12] have numerous passive components; consequently, the size and losses of the system are substantial. The Z-source converter presented in [11] has an improved boost ability, but the current crossing the switch is high due to the presence of a current path among the capacitors. By taking the number of Z-source components into account, the boost factor of the quasi-Z-source (qZS) DC-DC converter with switched capacitor presented in [12] is not considerable. Although the qZS DC-DC converter in [17] has high voltage gain, the input current ripple is considerable, and a high number of passive elements is penalizing. Reducing the number of additional passive components to the Z-source network can play an important role in decreasing the size, cost, and losses of systems.

The boost factor of the converter can also be increased by using an extra switch in the impedance network, which leads to a reduction of the passive components [19]. Generally, the structures that do not have extra switch have more passive parts in their networks. For example, the number of elements added to the Z-source network of Hybrid Z-Source Boost DC-DC converters (HZS-BC) [20] to achieve high boosting ability ($B = \frac{1}{1-4D}$) is relatively high in comparison with some classical switched boost converters.

Current spikes, high current stress, separate grounds between DC source and load, high duty ratio, and discontinuous current are the other concerns which are discussed in literature. The structure of the switched-capacitor switched-boost converter (SC-SBC) [21] is shown in Fig. 1(a). The boost factor of this converter is $B = 2 \frac{1-D}{1-2D}$. In this converter, C_1 , C_2 and C_0 capacitors make an current path when the switches S_1 and S_2 are on. Because of this drawback, the discontinuous currents crossing the switches as well as the input source have high peak values and ripples. Moreover, as in the Z-source converter (ZSC) [22], the DC source and the load in SC-SBC also have separated grounds. Generating high voltage gain is the advantage of switched-capacitor-based active-network converter (SC-ANC) [23], but the source current ripple is noticeable. Complexity and large value of input current ripple can be mentioned as disadvantages of the presented converter in [24] (DIESC-SC). The proposed interleaved boost converter (IBC) in [25] has an additional switch in its impedance network, but it does not provide high voltage gain in high duty ratio. One of the proposed converters in [26] (S-SCZSC) has a high boosting ability ($B = \frac{1}{3-2D}$), however, it suffers from the high peak current crossing the switches.

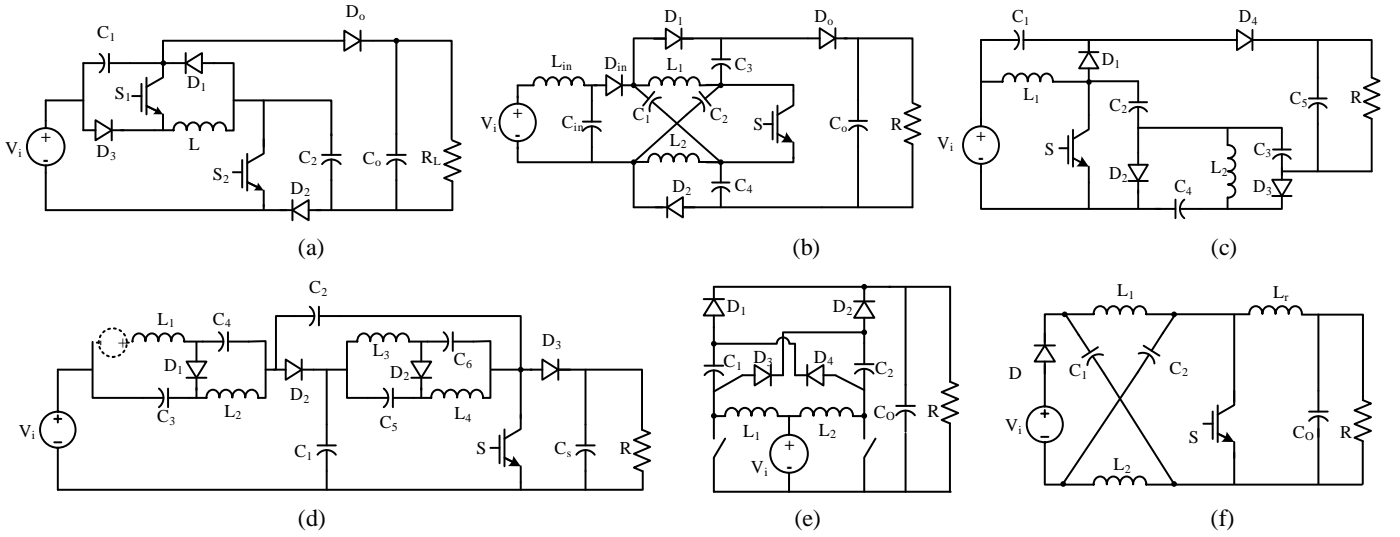


Fig. 1 Conventional converters; (a) SC-SBC [21], (b) S-SCZSC [26], (c) DIESC-SC [24], (d) HZS-BC [20], (e) IBC [25], (f) ZSC [22].

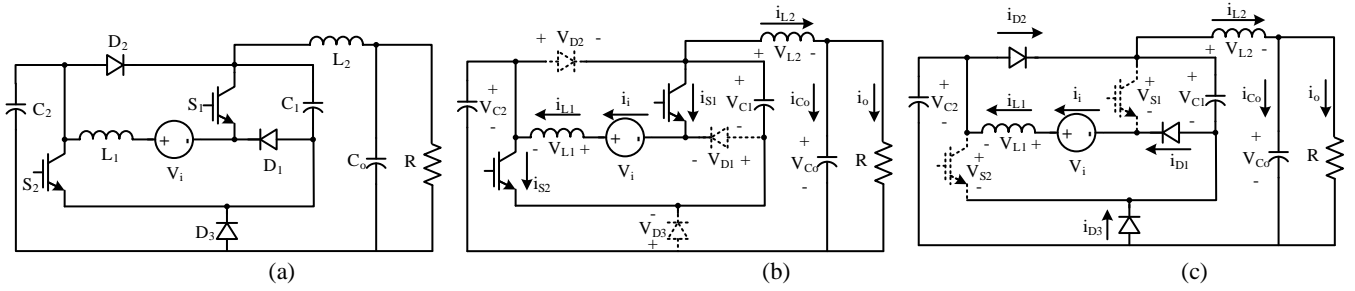


Fig. 2. Proposed ESC-ZSC topology and equivalent circuits in CCM; (a) Circuit of the ESC-ZSC, (b) Switches are on, (c) Switches are off.

In this paper, a new extended-boost DC-DC structure, namely symmetric embedded switched capacitor Z-source converter (ESC-ZSC), is proposed. This original circuit has the following features. It operates at continuous source current and at increased output voltage, with symmetric voltage on the main capacitors of the Z-source network (C_1 and C_2), diodes and switches. Moreover, the inrush current problem is tackled and the ripple of the output voltage is limited and independent of the output power as long as the converter operates in the continuous-conduction mode (CCM). Lastly, it has separate grounds.

The other parts of the paper are organized as follows. In section II, the principles of operation are presented and focus is made on the boost factor. Section III presents a comparison with the other topologies. Section IV provides some selected simulation results by considering conduction losses. Then experimental results are given and discussed in section V. Finally, section VI concludes the paper.

II. PROPOSED CONVERTER

The proposed ESC-ZSC topology is shown in Fig. 2. The operation is analyzed in detail in the following subsections.

A. Principle of Operation

The equivalent circuit of the proposed ESC-ZSC in CCM is shown in Fig. 2. When S_1 and S_2 are on, all diodes are blocked, and when S_1 and S_2 are off, these diodes are on. Looking at Figs. 2 and 3(a) the voltages across the inductors during CCM can be

obtained by applying Kirchhoff Voltage Law (KVL) to the circuits shown in Figs. 2(b) and 2(c):

$$\begin{cases} v_{L1,on} = V_i + V_{C1} \\ v_{L2,on} = V_{C1} + V_{C2} - V_{Co} \end{cases} \quad (1)$$

$$\begin{cases} v_{L1,off} = V_i - V_{C1} \\ v_{L2,off} = V_{C1} - V_{Co} \end{cases}, \quad V_{C1} = V_{C2} \quad (2)$$

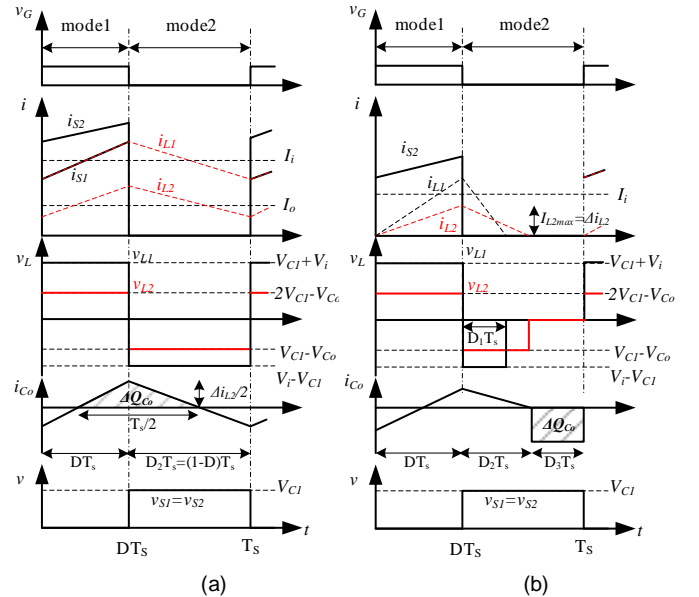


Fig. 3. Key waveforms in a) CCM, b) DCM.

In the steady state, the average value of voltage across the inductors is equal to zero. In mode 1, the switches are on and they are conducting during DT_s , and in mode 2 the current of L_1 and L_2 is flowing for D_1T_s and D_2T_s second (general expressions of the conduction times, whatever the considered conduction mode, CCM or discontinuous-conduction mode (DCM)). Therefore, we can obtain the following expressions for the mean values:

$$\begin{cases} V_{C1} = V_{C2} = \frac{D_1+D}{D_1-D} V_i \\ V_{S1} = V_{S2} = \frac{D_1+D}{D_1-D} V_i \\ V_{D1} = V_{D2} = V_{D3} = \frac{D_1+D}{D_1-D} V_i \\ V_{Co} = \left(\frac{D_2+2D}{D_2+D}\right) \left(\frac{D_1+D}{D_1-D}\right) V_i \end{cases} \quad (3)$$

In CCM case, $D_1 = D_2 = 1 - D$; therefore, the voltage across the capacitors, the output voltage gain, the voltage on the switches and diodes are expressed as follows (diodes and switches are considered as ideal, as well as the inductors):

$$\begin{cases} V_{C1} = V_{C2} = \frac{1}{1-2D} V_i \\ V_{S1} = V_{S2} = \frac{1}{1-2D} V_i \\ V_{D1} = V_{D2} = V_{D3} = \frac{1}{1-2D} V_i \\ G = G_{CCM} = \frac{V_{Co}}{V_i} = \frac{1+D}{1-2D} \end{cases} \quad (4)$$

According to (4), the voltages of capacitors C_1 and C_2 in the Z-source network are the same. Thus, the voltages across the main capacitors, switches and diodes of the proposed ESC-ZSC are symmetric. In addition, the voltages on the two switches are less than the output voltage.

The source and inductor (L_1) have a series connection so that the source current is the same as the inductor current (L_1). Assuming the lossless condition for the circuits shown in Fig. 2 and as $I_i V_i = I_o V_o$ and $I_o = \frac{V_o}{R}$, the following equation can be written:

$$I_i V_i = I_{L1} V_i = V_o \left(\frac{V_o}{R}\right) = \frac{(GV_i)^2}{R} \Rightarrow \quad (5-1)$$

$$I_{L1} = I_i = \frac{GV_i}{R} = \frac{(1+D)^2}{R(1-2D)^2} V_i \quad (5-2)$$

where R is the load resistance. The ripple of the inductor current L_1 for ESC-ZSC by using (1) is calculated as follows,

$$\frac{di_{L1,on}}{dt} = \frac{V_{C1}+V_i}{L_1} = \frac{2(1-D)}{L_1(1-2D)} V_i \quad (6-1)$$

$$\Delta i_{L1} = \frac{2(1-D)DT_s}{L_1(1-2D)} V_i = \frac{2(1-D)D}{f_s L_1 (1+D)} V_o \quad (6-2)$$

where $f_s = \frac{1}{T_s}$ is the switching frequency. For inductor L_2 following equation can be obtained,

$$I_{L2} = \frac{V_{Co}}{R} = \frac{1+D}{R(1-2D)} V_i \quad (7)$$

The ripple of the inductor current L_2 by considering (1) can be obtained,

$$\frac{di_{L2,on}}{dt} = \frac{2V_{C1}-V_{Co}}{L_2} = \frac{(1-D)}{L_2(1-2D)} V_i \quad (8-1)$$

$$\Delta i_{L2} = \frac{(1-D)DT_s}{L_2(1-2D)} V_i = \frac{(1-D)D}{f_s L_2 (1+D)} V_o \quad (8-2)$$

The proposed ESC-ZSC operates in CCM mode under the following condition, otherwise it operates in DCM:

$$I_L - \frac{\Delta i_L}{2} \geq 0 \quad (9)$$

The key waveforms of the proposed ESC-ZSC are shown in Fig. 3. The average (DC value) and current ripple of the inductors are presented in (5) to (8). By considering these relations and substituting into (9), we have the following relation while V_o is constant.

$$\begin{cases} K_1 = \frac{L_1}{RT_s} \\ K_{crit,1} = \frac{D(1-D)(1-2D)}{(1+D)^2} \end{cases} \text{ for } L_1 \quad (10)$$

As long as $K_1 > K_{crit,1}$, the proposed converter operates in CCM and the proposed ESC-ZSC enters DCM while $K_1 < K_{crit,1}$. The criteria for the L_2 inductance can be found in a similar way which is $K_{crit,2} = \frac{(1-D)D}{2(1+D)}$ and $K_2 = \frac{L_2}{RT_s}$. The boundary between CCM and DCM as a function of duty ratio is shown in Fig. 4.

The output voltage gain in DCM can be obtained from utilizing the fact of volt-second balance and capacitor charge balance laws and in DCM, and substituting in (3) yields:

$$G_{DCM} = \left(\frac{D_2+2D}{D_2+D}\right) \left(\frac{D_1+D}{D_1-D}\right) \quad (11)$$

It is supposed that $K_{1,2} < K_{crit1,2}$. The DCM leads to an overboost impact on voltage gain and capacitor voltage (Fig. 5).

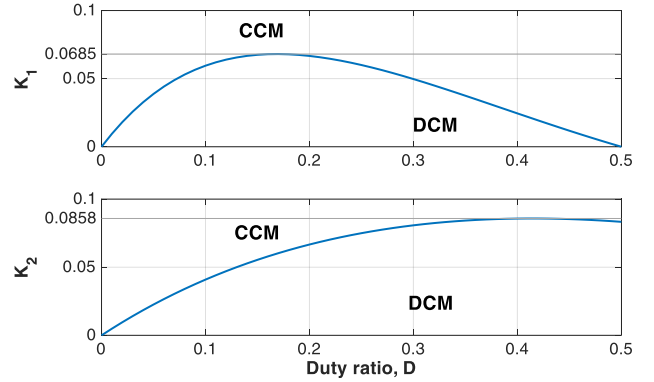


Fig. 4. Boundary of continuous-discontinuous conduction.

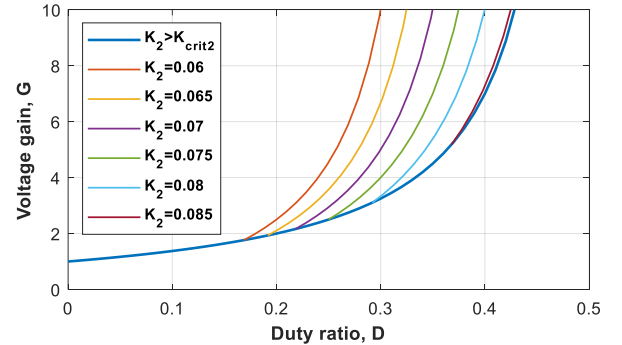


Fig. 5. Output voltage in DCM and its variation with duty ratio.

Let's now consider that the power losses of L_1 and L_2 are modelled by r_1 and r_2 , respectively, and the load resistance is R ; therefore, the nonideal voltage gain is:

$$G_{ideal} = \frac{R(1+D)(1-2D)}{-(4R+r_1+4r_2)D^2 + 2(2R+2r_2-r_1)D - (R+r_1+r_2)} \quad (12)$$

The nonideal voltage gain (G_{ideal}) is plotted in Fig. 6 as a function of duty ratio. Here r_1 , r_2 and R are supposed to be 0.2Ω , 0.2Ω and 200Ω , respectively.

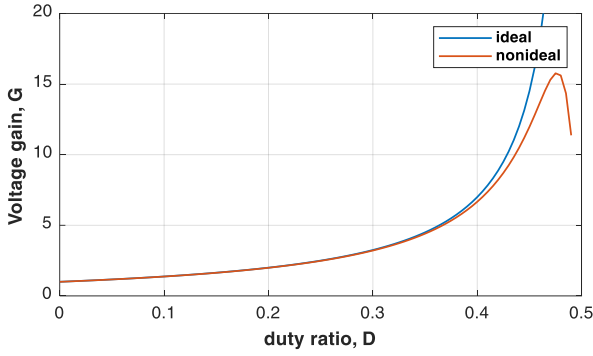


Fig. 6. Comparison of ideal and nonideal voltage gains, considering the losses of inductors.

B. Parameters Design

In this section, the parameters design of passive components is presented. The voltage across the inductor and capacitor current can be written as follow:

$$\begin{cases} v_L = L \frac{di_L}{dt} = \frac{L \cdot \Delta i_L}{\Delta t} = \frac{L \cdot \Delta i_L \cdot f_s}{D} & \text{and } \frac{\Delta i_L}{i_L} = \%i_L \\ i_C = C \frac{dV_C}{dt} = \frac{C \cdot \Delta V_C}{\Delta t} = \frac{C \cdot \Delta V_C \cdot f_s}{D} & \text{and } \frac{\Delta V_C}{V_C} = \%V_C \end{cases} \quad (13)$$

The voltage across the inductors in mode 1 and mode 2 and the average value of inductors current are presented in (1), (2), (5) and (7). By considering these relations as well as (13), for a given current ripple ($\%i_L$) and duty ratio (D), the inductors can be designed as follow:

$$\begin{cases} L_1 = \frac{2D(1-D)(1-2D)}{f_s \%i_{L1}(D+1)^2} R \\ L_2 = \frac{D(1-D)}{f_s \%i_{L2}(D+1)} R \end{cases} \quad (14)$$

To operate in CCM and for the constant V_o the condition of $K > K_{crit}$ should be satisfied, so that a minimum inductance is necessary.

$$K \geq K_{crit} \Rightarrow \begin{cases} L_{1,min} = \frac{D(1-D)(1-2D)}{f_s(1+D)^2} \cdot R \\ L_{2,min} = \frac{D(1-D)}{f_s(1+D)} \cdot R \end{cases} \quad (15)$$

To guarantee to be in CCM it is better to choose the inductance at least 25% bigger than $L_{1/2,min}$, so:

$$L_1 > 1.25 \times \frac{D(1-D)(1-2D)}{f_s(1+D)^2} \cdot R, L_2 > 1.25 \times \frac{D(1-D)}{f_s(1+D)} \cdot R \quad (16)$$

The voltage across the capacitors for ESC-ZSC is presented in equation (4). For given voltage ripple ($\%V_C$) and duty ratio, the capacitance of the capacitors by taking relations (4) and (13) into account can be designed as follow:

$$\begin{cases} C_1 = \frac{D(-D^2+D+2)}{f_s R \%V_{C1}(1-2D)} \\ C_2 = \frac{D \cdot (D+1)}{f_s R \%V_{C2}} \\ C_o = \frac{D^2(1-D)}{4f_s L_2 \%V_{Co}(D+1)} \end{cases} \quad (17)$$

III. COMPARISON WITH THE OTHER CONVERTERS

In this section a comparison with some of the other topologies is presented.

A. Voltage Gain Comparison (CCM)

With regard to relation (4) in the proposed ESC-ZSC, the duty ratio can be selected between 0 and 0.5. Therefore, the

output voltage of ESC-ZSC can be regulated over a wide range of input voltage.

Fig. 7 presents the comparison of the voltage gain of the proposed ESC-ZSC and other ZSC topologies, namely ZSC [22], SC-SBC [21], DIESC-SC [24], IBC [25], and S-SCZSC [26]. From Fig. 7, it can be deduced that the voltage gain of the proposed topology is more than its counterparts other than S-SCZSC, and it is almost ahead of the others for a range of duty cycles, in particular for $D > 0.33$. It is worth mentioning that ESC-ZSC has the same voltage gain as SC-qZSC [12], which is not shown in Fig. 7 for the sake of simplicity.

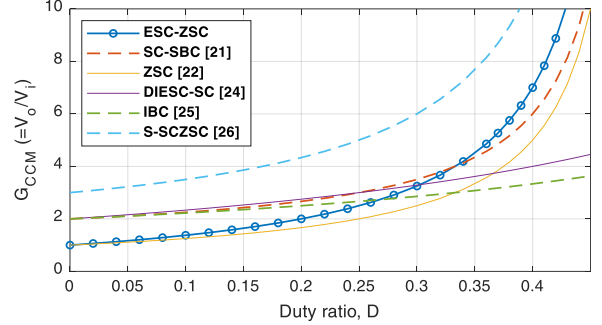


Fig. 7. Variation of G versus D of ESC-ZSC and conventional topologies in CCM.

TABLE I
COMPARISON OF COMPONENT QUANTITIES IN DIFFERENT TOPOLOGIES

Topology	inductor	capacitor	diode	switch
SC-qZSC [12]	3	5	3	1
HZS-BC [20]	4	7	4	1
SC-SBC [21]	1	3	4	2
ZSC [22]	3	3	1	1
DIESC-SC [24]	2	5	4	1
IBC [25]	2	3	4	2
S-SCZSC [26]	3	5	4	1
ESC-ZSC (This paper)	2	3	3	2

B. Number of Component Comparison

Table I compares the proposed ESC-ZSC and the other topologies; by considering this table and Fig. 7, it can be concluded that:

- The proposed ESC-ZSC has the same voltage gain as SC-qZSC [12] while having fewer elements.
- The proposed ESC-ZSC provides a high boost factor with the exact components count in the Z-source network compared with conventional SC-SBC [21] topology.
- Although the proposed ESC-ZSC has fewer elements than DIESC-SC [24], it has better voltage gain.
- The proposed ESC-ZSC has one fewer diode and higher voltage gain than IBC [25].
- By implementing more components, S-SCZSC [26] performs higher voltage gain than ESC-ZSC.

C. Current Stress Comparison

According to Fig. 2, for the proposed ESC-ZSC, the average switches current (I_{S1}, I_{S2}) can be calculated as below,

$$I_{S1} = I_{L1} = \frac{(1+D)^2}{R(1-2D)^2} V_i = \frac{1+D}{1-2D} \cdot \frac{V_o}{R} \quad (18)$$

$$I_{S2} = I_{L1} + I_{L2} = \left(\frac{1+D}{1-2D} + 1 \right) \cdot \frac{V_o}{R} \quad (19)$$

The comparison of the normalized average current stresses in the proposed topology and conventional SC-SBC [21] and S-SCZSC [26] topologies is shown in Fig. 8 for the constant output voltage and constant load. Tables II and III compare the normalized average current stress and the normalized voltage stress in counterpart topologies. Moreover, in table III some of the current stresses are presented in both term of duty cycle and term of voltage gain, for example, in last column for ESC-ZSC the current stress of L_1 is $\frac{1+D}{1-2D}$ which can be represented as G . In other words, we have $\bar{I}_{L1} = \frac{1+D}{1-2D} = G$.

As shown in Fig. 8 and equations (18) and (19), the average switches currents in the proposed topology are noticeably decreased in comparison with the conventional topologies.

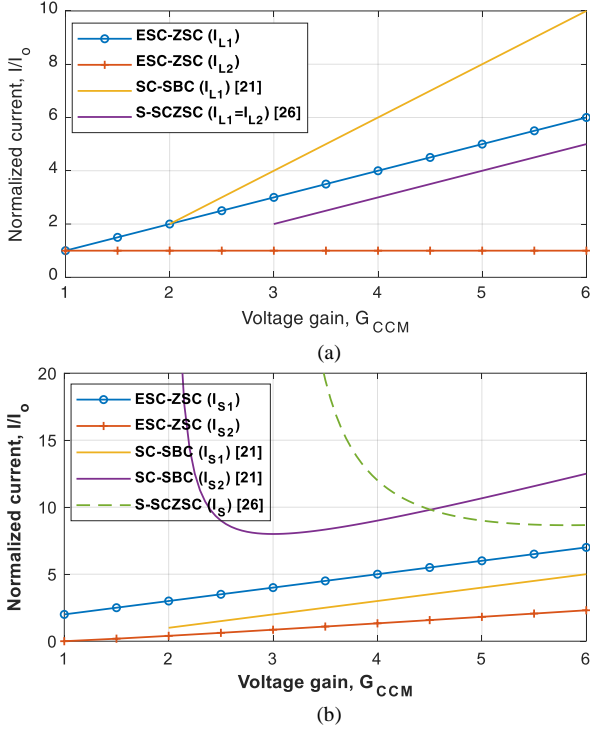


Fig. 8. Variation of components' average current stresses in various topologies, (a) average current stresses of inductors, (b) average current stresses of switches.

The peak current stress of the switches in ESC-ZSC is as below:

$$\hat{I}_{S1} = I_{L1,max} = I_{S1} + \frac{\Delta i_{L1}}{2} \quad (20)$$

$$\hat{I}_{S2} = I_{L1,max} + I_{L2,max} = I_{S2} + \frac{\Delta i_{L1}}{2} + \frac{\Delta i_{L2}}{2} \quad (21)$$

Looking at Fig. 9(a) one can deduce that in SC-SBC when the switches are on, the source, C_1 , C_o and C_2 are placed in a loop. If V_i and $V_{C1} + V_{C2} - V_{Co}$ are not equal then their difference drops on the parasitic parameters like the loop impedance, R_{don} of the semiconductors and etc. Due to the fact that the impedances of the parasitic parameters are not big enough to prevent the current from being high, a small amount of unbalanced voltage causes a spike current pass through the switch at the very beginning of each duty ratio of the switches. Supposing that the total amount of current produced by similar effects is ξ the peak value of switch current in SC-SBC becomes:

$$\hat{I}_{S2} \approx I_{S2} + \xi \quad (22)$$

$$\hat{I}_{S1} = I_{S1} + \frac{\Delta i_L}{2} \quad (23)$$

S-SCZSC acts up in a similar way and:

$$\hat{I}_S \approx I_S + \zeta \quad (24)$$

Where ζ is the total amount of current produced by capacitors' loops.

D. Output Voltage Ripple

For SC-SBC the output diode does not conduct during mode 1 and in S-SCZSC the output diode is off in mode 2 (Fig. 9 (b,c)). The output diode current is $i_o = i_{Co} + I_o$ supposing that the load current does not ripple and the average of i_o supplies the load and its ripple flows through C_o ; therefore:

$$i_{Co} = i_o - I_o = i_o - \frac{V_o}{R} \quad (25)$$

When D_o is off i_{Co} is $-I_o$ and we have:

$$\Delta Q_{Co} = (1-D)T_s \cdot \frac{V_o}{R} \quad \text{for SC-SBC} \quad (26)$$

$$\Delta Q_{Co} = DT_s \cdot \frac{V_o}{R} \quad \text{for S-SCZSC} \quad (27)$$

TABLE II
COMPARISON OF THE VOLTAGE STRESS (NORMALIZED TO V_i) IN DIFFERENT TOPOLOGIES.

component	Voltage stress	SC-SBC [21]	S-SCZSC [26]	ESC-ZSC
Capacitors	C_1	$V_{C1} \frac{D}{1-2D}$		$\frac{1}{1-2D}$
	C_2	$V_{C2} \frac{1-D}{1-2D}$	$\frac{1-D}{1-2D}$	
	C_3	V_{C3}	-	-
	C_4	V_{C4}	-	-
Diodes	D_1	$\hat{V}_{D1} \frac{1-D}{1-2D}$		$\frac{1}{1-2D}$
	D_2	$\hat{V}_{D2} \frac{1-D}{1-2D}$	$\frac{1}{1-2D}$	
	D_3	$\hat{V}_{D3} \frac{D}{1-2D}$		
	D_o	$\hat{V}_{Do} \frac{1-D}{1-2D}$		-
Power switches	S_1	$\hat{V}_{S1} \frac{D}{1-2D}$	$\frac{1}{1-2D}$	$\frac{1}{1-2D}$
	S_2	$\hat{V}_{S2} \frac{1-D}{1-2D}$	$\frac{1}{1-2D}$	$\frac{1}{1-2D}$

TABLE III
COMPARISON OF THE AVERAGE CURRENT STRESS (NORMALIZED TO I_o) IN DIFFERENT TOPOLOGIES, SOME OF THEM ARE PRESENTED IN TERM OF VOLTAGE GAIN, TOO.

component	current stress	SC-SBC [21]	S-SCZSC [26]	ESC-ZSC
Inductors	L_1	$\bar{I}_{L1} \frac{2}{1-2D}$	$\frac{2}{2(G-1)}$	$\frac{1+D}{G}$
	L_2	\bar{I}_{L2}	$\frac{2}{2(G-1)}$	$\frac{1}{1}$
Diodes	D_1	$\bar{I}_{D1} \frac{1}{2D^2-3D+1}$	$\frac{2-3D}{1-2D}$	$\frac{(1-D)(1+D)}{1-2D}$
	D_2	$\bar{I}_{D2} \frac{1}{1-D}$	1	$1-D$
	D_3	$\bar{I}_{D3} \frac{2}{1-2D}$	1	$1-D$
	D_o	$\bar{I}_{Do} \frac{1}{D}$	1	-
Power switches	S_1	$\bar{I}_{S1} \frac{2}{1-2D}$	$\frac{4D^2-2D+2}{D(1-2D)}$	$\frac{D(1+D)}{1-2D}$
	S_2	$\bar{I}_{S2} \frac{1}{2(G-1)^2}$	$\frac{G^2-3G+8}{G-3}$	$\frac{6(G-1)}{2G+1}$
		$\frac{1}{G-2}$	-	$1 + \frac{1+D}{1-2D}$
			-	$1+G$

TABLE IV
COMPARISON OF DIFFERENT TOPOLOGIES

Topology	SC-qZSC [12]	SC-SBC [21]	ZSC [22]	DIESC-SC [24]	IBC [25]	S-SCZSC [26]	Proposed ESC-ZSC
The voltage gain	$\frac{1+D}{1-2D}$	$\frac{2(1-D)}{1-2D}$	$\frac{1}{1-2D}$	$\frac{2+D}{1-D}$	$\frac{2}{1-D}$	$\frac{3-2D}{1-2D}$	$\frac{1+D}{1-2D}$
Number of components	✓	✓✓✓	✓✓✓	✓	✓✓	✓	✓✓✓
Start-up current inrushing	✓✓✓	×	×	×	✓✓✓	✓✓✓	✓✓✓
The switch current	✓✓✓	×	✓✓✓	×	✓✓✓	×	✓✓✓
The input current ripple	×	×	×	×	✓✓✓	✓✓✓	✓✓✓
The input current	Cont.*	Discont.*	Discont.	Cont.	Cont.	Cont.	Cont.
Output voltage ripple (CCM)	Dep.*	Dep.	Indep.*	Dep.	Dep.	Dep.	Indep.

* the abbreviations stand for as following: *Cont.*=continuous, *Discont.*=discontinuous, *Dep.*=dependent on the load, and *Indep.*=independent of the load.

Knowing that $\Delta V_{C_o} = \frac{\Delta Q_{C_o}}{C_o}$, the normalized voltage ripple of the output capacitor is as following and they are dependent to the load:

$$\frac{\Delta V_{C_o}}{V_o} = \frac{1-D}{f_s R C_o} \quad \text{for SC-SBC} \quad (28-1)$$

$$\frac{\Delta V_{C_o}}{V_o} = \frac{D}{f_s R C_o} \quad \text{for S-SCZSC} \quad (28-2)$$

For ESC-ZSC the current ripple of L_2 flows through C_o and:

$$\Delta Q_{C_o} = \frac{T_s}{2} \cdot \frac{\Delta i_{L_2}}{2} = \frac{1}{4} \cdot \frac{D(1-D)T_s^2}{L_2(1-2D)} \cdot V_i = \frac{T_s^2 D}{4L_2} \cdot \frac{1-D}{1+D} V_o \quad (29)$$

and then:

$$\frac{\Delta V_{C_o}}{V_o} = \frac{D(1-D)}{4f_s^2 L_2 C_o (1+D)} \quad (30)$$

In addition, the voltage ripple due to equivalent series resistance (ESR) of output capacitor is:

$$\frac{\Delta V_{ESR}}{V_o} = \frac{\Delta i_{L_2}}{V_o} \cdot r_c = \frac{D(1-D)}{f_s L_2 (1+D)} \cdot r_c \quad (31)$$

where r_c is the ESR value. Relation (30) shows that at CCM the output voltage ripple in ESC-ZSC is independent of load. Moreover, comparing (28) and (30) declares that the output voltage ripple in ESC-ZSC is much better than S-SCZSC and SC-SBC.

Without a substantial increase in the parts count just by using a single additional switch in the impedance network, the boost factor is significantly increased. Based on the used components, a comparison between the proposed converter and some competitors shown in Fig. 1 is summarized in Table I. In the proposed ESC-ZSC, the inductor L_1 is connected in series with the source; therefore, the source has continuous current in CCM, and a proper design of L_1 can limit the ripple of the source current. In addition, the inductor L_2 is placed at the output stage and contributes to filter the output. Moreover, thanks to the presence of L_2 , the current that supplies the output stage ($C_o R$) is kept continuous which also helps reduce the output voltage ripple. In the proposed ESC-ZSC, when the switches are on, the diodes D_1 and D_2 prevent the capacitors from being placed in a loop and the C_1 , C_2 and C_o capacitors have no inherent current path. Thus, the peak value of the currents that pass through the switches and the source are very low compared with conventional SC-SBC and S-SCZSC. Unfortunately, the load and the source do not have a common ground which may limit the applications of the converter and causes more complicated gate drive circuits for the switches. In comparison with SC-SBC and S-SCZSC, the voltage stress on power switches is higher in ESC-ZSC. Table IV presents a

comparative overview of proposed and conventional topologies to reveal the merits and demerits.

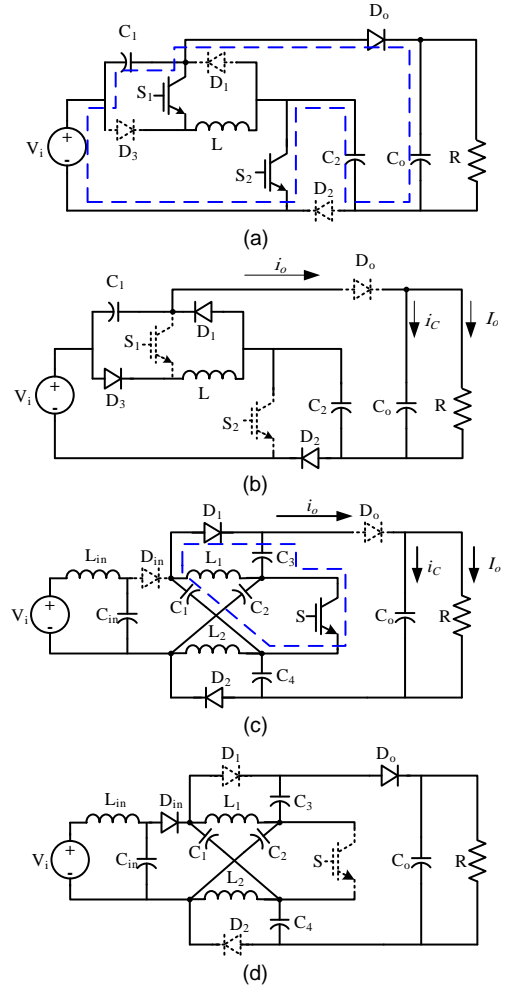


Fig. 9. The equivalent circuits of: (a,b) SC-SBC in modes 1 and 2, (c, d) S-SCZSC in modes 1 and 2.

IV. SIMULATION RESULTS

In this section, the proposed converter is compared with the conventional SC-SBC and S-SCZSC by means of simulations carried out in MATLAB software. The parameters used in the simulations are presented in Table V. The comparison between conventional and proposed topologies in the same condition (with the presented parameters in Table V) is illustrated in Fig. 10.

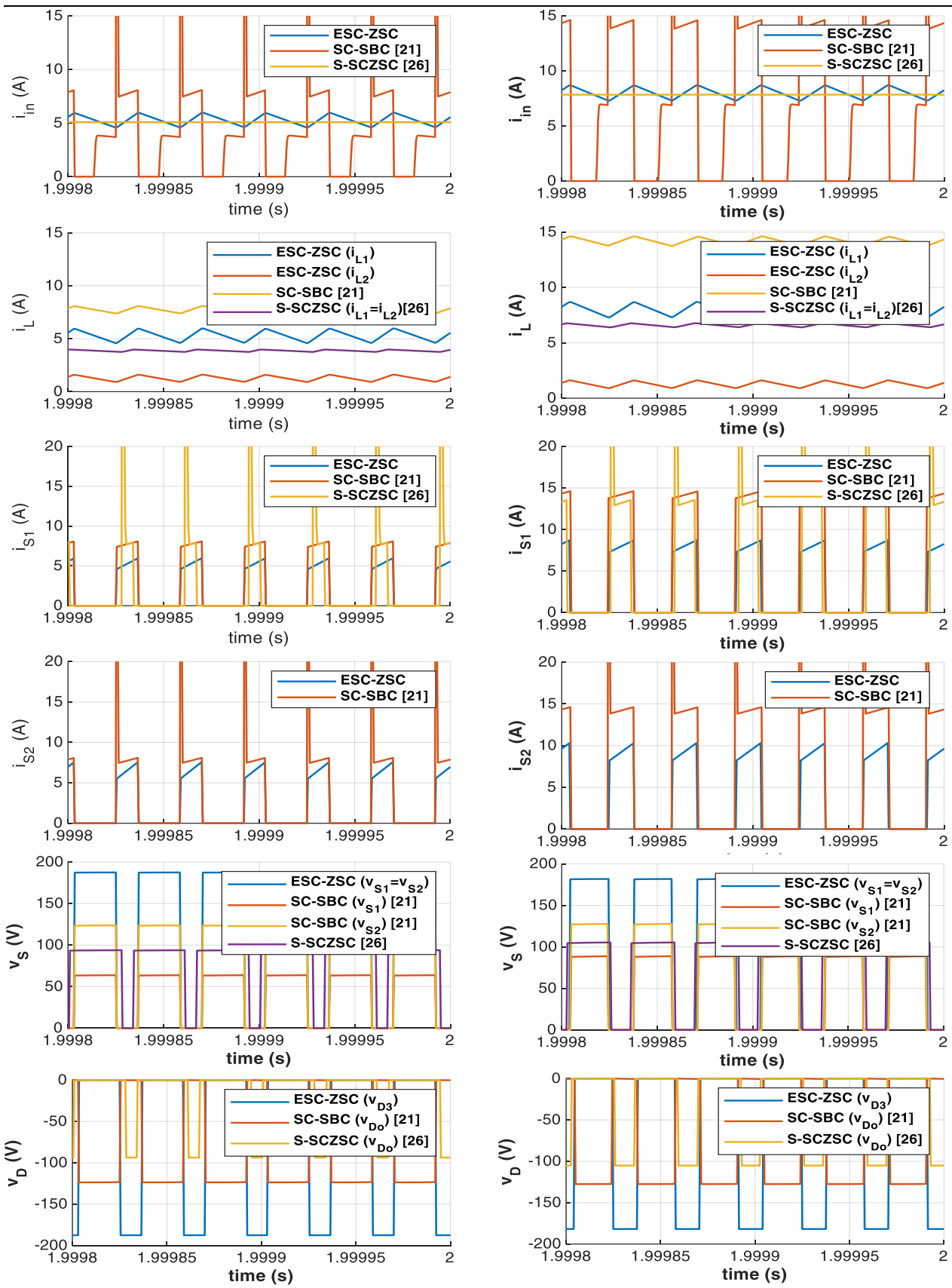


Fig. 10 Simulation results of ESC-ZSC, SC-SBC, and S-SCZSC under the fixed output voltage and fixed load; (a) $V_i = 60\text{ V}$, (b) $V_i = 40\text{ V}$. From up to down, source current (i_{in}), inductors' currents (i_L), switches current ($i_{s1,2}$), switches voltage (v_s), and diode voltage (v_D).

We consider two input voltage levels, 40 V and 60 V and the duty ratio is tuned to have a fixed output voltage about 251 V. The parameters for SC-SBC and S-SCZSC are same as Table V except for duty ratio. In Fig. 10 first column (Fig. 10(a)) is for $V_i = 60 V$ and second column (Fig. 10(b)) is for $V_i = 40 V$. As the output power is fixed, the source current (i_{in}) increases when $V_i = 40 V$.

It can be also seen that the source current is discontinuous for SC-SBC, and due to presence of an input filter in S-SCZSC, its source current does not have large ripple. Because the parasitic effects are not simulated precisely the peak value of current spike for SC-SBC is not shown and the curves are clipped at 15 – 20 A. However, because of the capacitors' loop, the source current of SC-SBC jumps at the beginning of duty ratio. The current stress of inductor is the highest for SC-SBC, but it has only one inductor. S-SCZSC has two inductors and the summation of their current stress is higher than that of the ESC-ZSC. For the same inductance value and the same output power, the current ripple of L_1 in ESC-ZSC is higher than the others. The current stress of power switches (i_{S1} and i_{S2}) is the best for ESC-ZSC; moreover, it does not have any spike while the switches' current in SC-SBC and S-SCZSC has a big peak value. From the voltage stress point of view ESC-ZSC is not better than the other topologies.

All in all, ESC-ZSC has the superior performance from the current stress and continuous current points of view and it performs the inferior status from the voltage stress point of view. Therefore, it can be concluded that the proposed converter is suitable for the applications concerning the higher current and it does not suit the needs for low voltage applications.

Taking the losses of the power switches and diodes into account, the efficiency of the converter under the approximately fixed output voltage condition can be estimated using the simulations. The obtained efficiencies are plotted in Fig. 11. In these simulations R_{Don} is 0.23Ω and $V_F = 1 V$ and the resistance of inductors is 0.2Ω .

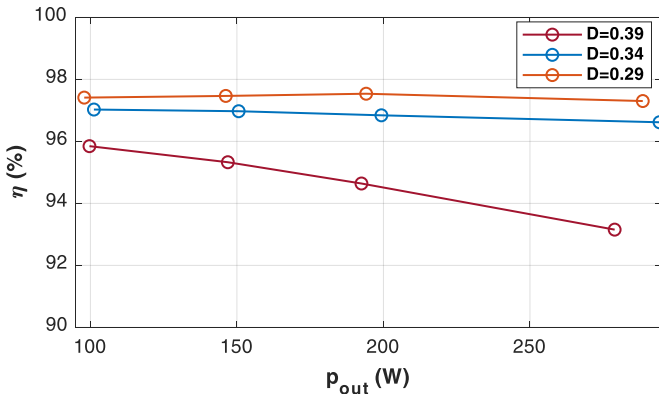
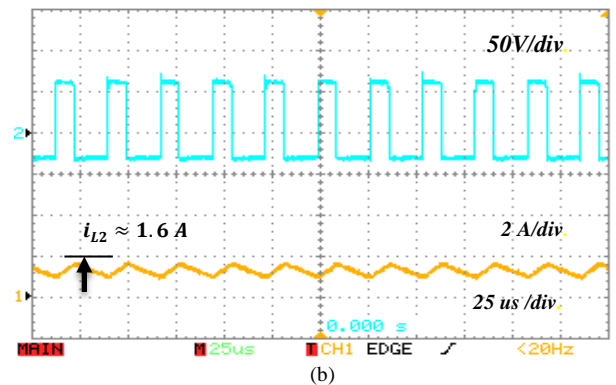
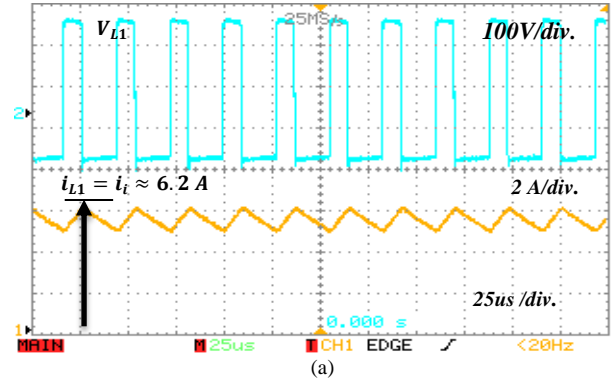


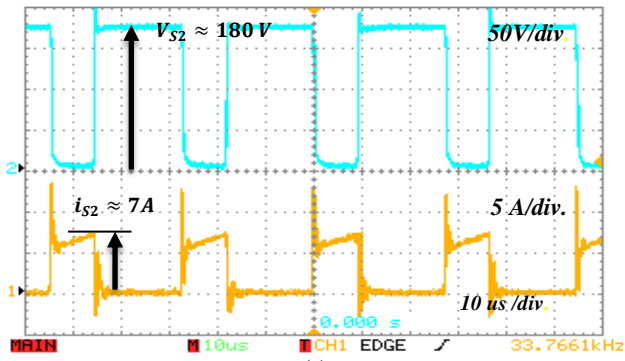
Fig. 11. Estimated efficiency obtained by simulations.

	simulation	experiment
Switching frequency (f_s)	30 kHz	30 kHz
Output voltage (V_{Co})	252 V	242 V
Duty ratio (D)	0.39-0.34	0.34
Load resistance (R)	200 Ω	200 Ω
Capacitors of ZSI (C)	330 μF	330 μF
Inductance of ZSI (L)	2 mH	2 mH
Input voltage (V_i)	40-60 Vdc	60 Vdc

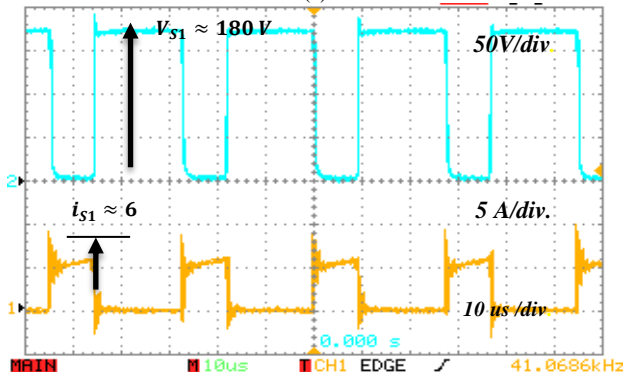
V. EXPERIMENTAL RESULTS

This section presents the results of the prototype test. The parameters used in experiments are presented in Table V. By taking Fig. 12 into account, there is a positive and close correlation between simulation (Fig. 10) and experimental results. The source ($i_{in} = i_{L1}$) and inductor current (i_{L2}) are shown in Figs. 12(a) and 12(b), respectively. According to relations (5) and (7), the ripple of inductor L_2 is half of the ripple of inductor L_1 . The switches current is demonstrated in Figs. 12(c) and 12(d). By comparing Figs. 10(a), 12(c) and 12(d), it can be concluded that the average value of switch current in experimental results are almost equal to the simulation results. The voltage and current of diodes are shown in Fig. 12(e-g). In Fig. 12(h), the output voltage ($V_{Co} = V_{Co}$) of ESC-ZSC is shown. It can be seen that the boost factor is equal to 4.03, which is close to the ideal boost factor, about 4.18.

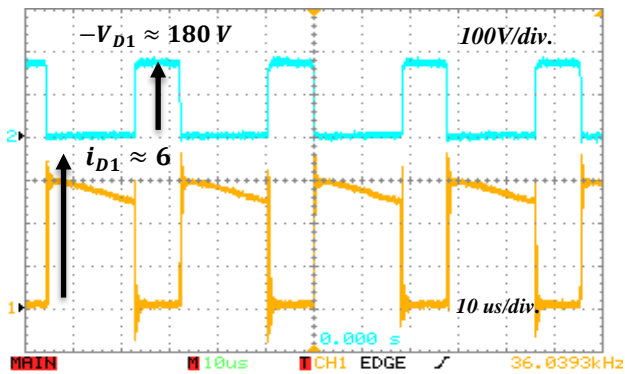




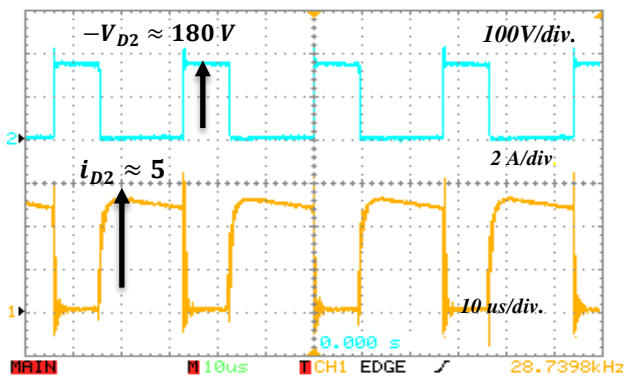
(c)



(d)



(e)



(f)

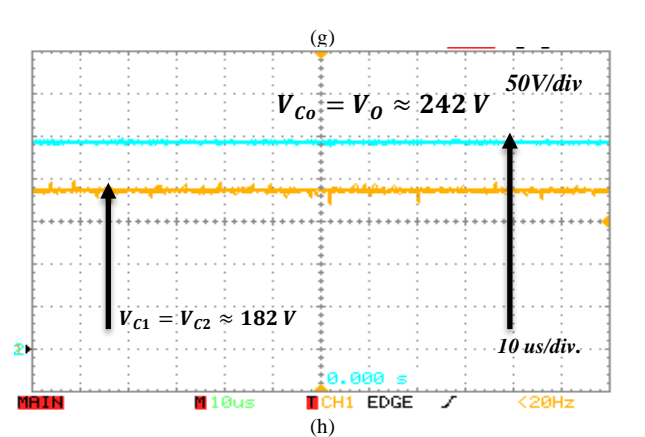
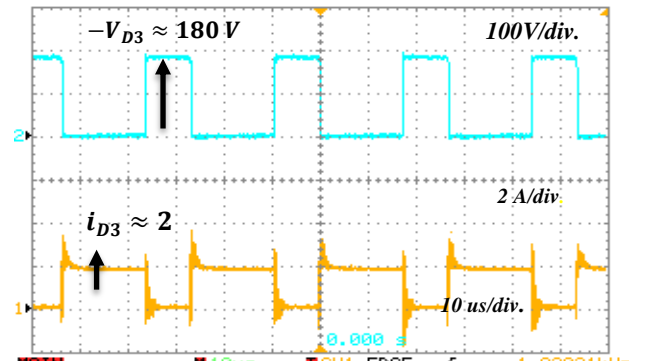


Fig. 12. The experimental results of ESC-ZSC.

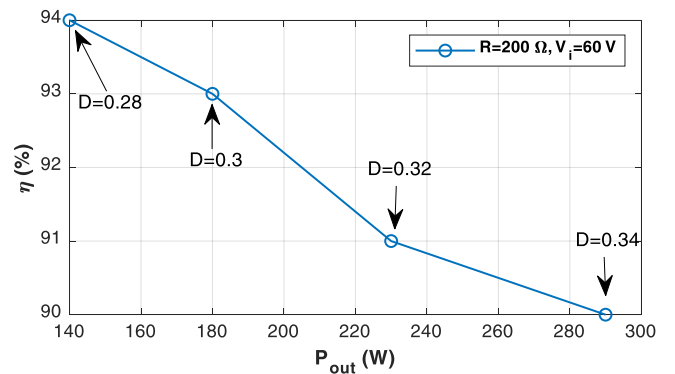


Fig. 13. Measured efficiency of the proposed ESC-ZSC.

The measured efficiency of the proposed ESC-ZSC under fixed load resistance ($R = 200\Omega$) and different duty ratios is plotted in Fig. 13. Increasing the duty ratio causes the average converter currents value to rise (diode, inductor, capacitor and switch) and consequently decreases the efficiency. This matter is shown in Fig. 13. However, in large output power, the efficiency of the system is still high.

VI. CONCLUSION

This study has introduced a new structure based on DC-DC Z-source converter. Thanks to the high voltage gain the proposed converter can be used in renewable energy systems in DC or hybrid microgrids. The source current is continuous with a negligible ripple, and the proposed ESC-ZSC has a high boost factor with a wide duty cycle range and also, this converter takes the advantage of a symmetric voltage on active and

passive components. The superiority of the proposed converter over the conventional SC-SBC and S-SCZSC is that the switches and source current are significantly decreased, which results in a reduction of losses and the nominal rating of the device (more than 50%) while maintaining a high boost factor and possessing the same number of components. Compared with the conventional IBC, the proposed ESC-ZSC structure has one fewer diode. However, the boost factor of ESC-ZSC is higher than that of conventional IBC. The proposed ESC-ZSC has the same voltage gain as SC-qZSC. In contrast, the ESC-ZSC has fewer components in the Z-source network. The comprehensive analysis of the proposed converter, such as voltage stress on the capacitor, the voltage gain of the converter, and parameters design were presented. Also, the merits of the proposed topology were investigated by simulation results in MATLAB software by considering the conduction losses. Finally, experiments were conducted to validate the approaches and analyses.

It is concluded that due to lower current stress, the proposed converter is suitable for the applications that require high current, and because of the higher voltage stress it does not suit the needs for low voltage applications.

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