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Optimization of an SSHC-Based Full Active Rectifier for Piezoelectric Energy Harvesting

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Abstract

This paper presents a compact and efficient integrated interface circuit for piezoelectric energy harvesting. While the state-of-the-art interface circuits require the use of either an external inductor or a significant number of additional capacitors to achieve high voltage flip and improve power efficiency, the proposed Full Active Rectifier on Flipping Capacitor (FAR-FC) is based on a reduced set of flipping capacitors and an active rectifier to efficiently flip the voltage across the piezoelectric transducer. In addition, this optimized SSHC circuit reaches better power efficiency when the piezoelectric transducer is operating under low mechanical excitation, i.e. when the open-circuit voltage of the piezoelectric transducer is $V_{oc} = 1V$, while this value is usually $V_{oc} \geq 2V$ in literature. Furthermore, the FAR-FC supports piezoelectric transducers with higher inherent capacitance values compared to those usually reported in literature, which makes the circuit potentially suitable for a larger variety of MEMS applications. The interface circuit was designed and fabricated in a 0.35- μm CMOS process. Measurement results show that the voltage flip efficiency goes up to **90%**. It also reveals that the proposed FAR-FC circuit achieves power performance up to **5.64** \times higher than a conventional full-bridge rectifier.

Keywords: Index Terms— piezoelectric transducer, integrated active rectifier, energy harvesting, synchronized switch harvesting on capacitors (SSHC).

1 Introduction

In the recent decade, ultra-low power wireless sensors have become of increase interest in a variety of applications [1–8]. For such sensors, batteries are the main energy sources despite of its finite lifetime. However, for certain applications such as aeronautics and rail transport, significant operation time of sensors is required. This makes the battery usage impractical and adds maintenance cost due to the periodic re-charging or replacement. In order to address this challenge and extend the operational lifetime of wireless sensors, there has been an emerging research interest in harvesting ambient energy. Many different kinds of energy harvesters have been proposed over the past decade such as solar, kinetic, thermal, wind. . . [9–16]. In the case of kinetic energy, the most popular type is the vibration-based energy harvesters. These are often used where mechanical vibration permanently or frequently occurs, such as the passing of vehicles, engines, or human movements [11, 17–19]. Among all vibration-based energy harvesting implementations, piezoelectric energy harvesting (PEH) is widely employed due to its high power density, scalability and compatibility with conventional integrated circuit technologies compared to other implementations, such as electromagnetic and electrostatic harvesters [20, 21]. The direct effect of the piezoelectric material causes the generating of an electrical charge when a mechanical strain is applied to it. Owing to its vibrational nature, the raw energy of this kind of harvester is unsuitable to directly power an electronic device. Therefore, an interface circuit is necessary to rectify the voltage across the piezoelectric transducer and provide stable power supply. Figure 1 shows a piezoelectric energy harvesting system. It consists of a piezoelectric transducer (PT), an interface circuit, storage and load elements. When the piezoelectric harvester vibrates at or near resonance, it can be modeled as an equivalent sinusoidal current source I_{peh} in parallel with the inherent piezoelectric capacitor C_{peh} . The need to discharge and recharge C_{peh} every cycle of I_{peh} significantly reduces the output voltage amplitude and thus the output power. This makes the use of the conventional diode-based full bridge rectifier FBR unsuitable for low PT voltage (i.e. around 1V or below) because of the threshold voltage of the rectifying diodes.

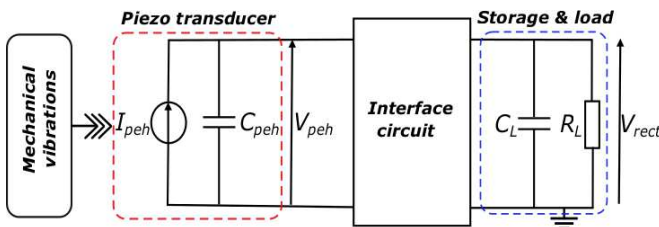


Fig. 1 Piezoelectric harvesting system.

To address this problem and improve the extracted power, many approaches have been proposed in literature. In the switch-only [22] approach,

a single switch is connected in parallel with the PT to instantly discharge C_{peh} every time the PT output voltage reaches its maximum. This eliminates the time required to discharge C_{peh} and leads to double the PT output voltage and thus the extracted power. However, there is still a charge loss due to the need to recharge C_{peh} every time I_{peh} changes direction.

To reduce this charge loss, different typologies have been implemented such as Synchronized Switch Harvesting on Inductor (SSHI) [22–25] and Synchronous Electric Charge Extraction (SECE) [26–31]. In these typologies, an inductor is employed to flip the voltage across the PT at each zero crossing of I_{peh} . Although SSHI and SECE can extract most of energy generated by the PT, they require a large inductor in range of (mH) with a high quality factor to reach satisfactory extracted power. This significantly increases the overall volume of the harvesting system and makes them not suitable for ultra-compact applications. Moreover, accurate RCL tuning is also needed to achieve acceptable power efficiency in SSHI [22], while in SECE, the PT should be weakly coupled to extract more power than that extracted by the FBR [30]. These limitations are overcome by replacing the inductor with one or more capacitors in Synchronized Switch Harvesting on Capacitor (SSHC) interface circuits [19, 32–35]. In SSHC, switched capacitors are used to flip the voltage across the PT. However, to reach high power efficiency, a significant number of flipping capacitors or flipping phases is needed [32–34]. This increases the system's volume and its control complexity. Furthermore, the large number of flipping capacitor/phases leads to increase the PT voltage flipping time i.e. decrease the power conduction time and thus the harvested power. This sets a significant constraint on the C_{peh} capacitance value, which should be in this case as low as possible to reduce the RC constant time required to discharging and recharging it i.e. the PT voltage flipping time [19, 32–34].

In addition, in the majority of research works proposed in the literature, in order to extract an acceptable power from the PT, the latter should operate under relatively high mechanical excitation level with an open circuit voltage greater than 1V [19, 22, 25, 26, 31, 32, 36]. However, in the real operation conditions of the PT, the mechanical excitation can be decreased leading to reduce both the PT open circuit voltage and generated power, and hence the extracted power by the interface circuit [37].

This paper presents an optimized version of the SSHC topology, named Full Active Rectifier on Flipping Capacitor (FAR-FC) [32, 34]. The proposed compact and efficient interface SSHC circuit uses a reduced set of capacitors to efficiently flip the voltage across the PT in only nine phases. This enables the use of PTs with higher C_{peh} capacitance value than the ones used in literature [32, 34]. The paper is organized as follows: section 2 recalls the principles of a the conventional capacitor-based interface SSHC [32]. The design of the FAR-FC with the detailed analysis of each building block is presented in section 3. Section 4 provides and discusses the measurement results. Finally, section 5 summarizes and concludes this paper.

2 Conventional Capacitor-Based SSH Interface

Figure 2 shows a one-capacitor SSHC interface circuit and the associated current, voltage and control signals waveforms [32]. This circuit consists of a diode-based full bridge rectifier (FBR) with only one switched flipping capacitor C_0 used to flip the voltage V_{peh} across the PT. The V_{peh} inversion is achieved using five analog switches. The V_{peh} inversion operation takes three phases: 1) the sharing phase (Φ_p) when the charge in C_{peh} is shared with C_0 , 2) the shorting phase (Φ_0) when C_{peh} is completely discharged and finally 3) the building phase when C_{peh} is recharged from C_0 in the reverse direction.

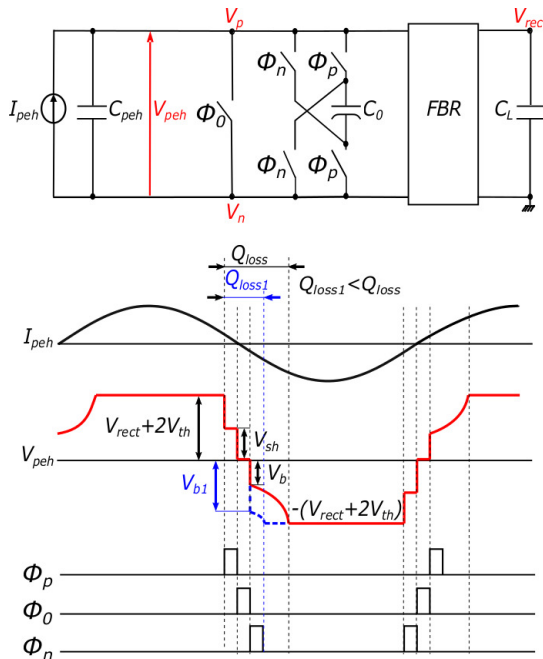


Fig. 2 One-capacitor SSHC interface circuit and associated waveforms.

As shown in Figure 2 (bottom), the voltage across PT before the flipping moment is $V_{peh} = V_{rect} + 2V_{th}$. Where V_{rect} is the voltage across the storage capacitor and V_{th} is the threshold voltage across the FBR diode. Assuming that the voltages across PT at the end of the sharing and the building phases are V_{sh} and V_b , respectively. In steady state V_b becomes constant and C_{peh} needs to further charge from V_b to $V_{rect} + 2V_{th}$. In order to evaluate the performance of this interface, the charge conservation equations are applied during both sharing and building phases, respectively:

$$V_{sh}(C_{peh} + C_0) = C_{peh}(V_{rect} + 2V_{th}) + C_0 V_b \quad (1)$$

$$V_b(C_{peh} + C_0) = V_{sh}C_0 \quad (2)$$

Assuming the voltage drop across the rectifying diodes of the FBR in addition to the parasitic loss related to all switches and capacitors are negligible, the ratio between the voltage across the PT after the building phases and the rectified voltage as expressed in [19] is:

$$K_{FCR} = \frac{V_b}{V_{rect}} = \frac{1}{2 + \frac{C_{peh}}{C_0}} \quad (3)$$

This ratio is highly related to the voltage flip efficiency $\eta_F = \frac{V_{rect} + V_b}{2V_{rect}}$ defined in [23] when the voltage drop across the FBR rectifying diodes is neglected. This relation can be given as:

$$\eta_F = \frac{K_{FCR} + 1}{2} \quad (4)$$

Hence, increasing K_{FCR} leads to increase the voltage flip efficiency. Also, in [19], Chen et. al. demonstrated that the maximum output power of this interface depends on K_{FCR} , expressed as:

$$P_{SSHCM_{max}} = \frac{2C_{peh}V_{oc}^2f_{ex}}{1 - K_{FCR}} \quad (5)$$

Therefore, the maximum output power improvement ratio of the one-capacitor SSHC interface as expressed in [19] is:

$$MOPIR_{SSHC} = \frac{P_{SSHCM_{max}}}{P_{FBR(ideal)_{max}}} = \frac{2}{1 - K_{FCR}} \quad (6)$$

where $P_{FBR(ideal)_{max}}$ is the maximum output power extracted by an ideal FBR [22] with zero voltage drop across its diodes expressed as:

$$P_{FBR(ideal)_{max}} = C_{peh}V_{oc}^2f_{ex} \quad (7)$$

From (3), one can notice that K_{FCR} is related to both C_{peh} and C_0 . When $C_0 \gg C_{peh}$, K_{FCR} converges to $\frac{1}{2}$, which yields $MOPIR = 4$. In order to improve the K_{FCR} of the one-capacitor SSHC interface circuit, several implementations have been proposed in the state of the art. In [32], using eight parallel flipping capacitors, improves the K_{FCR} to $4/5$ leading to $MOPIR = 9.7$. Recently, it was proved in [35], that using $C_0 = 100C_{peh}$ increases the output power by 35.7%. In another implementation, proposed in [19], the use of four re-configurable capacitors led to 0.85 voltage flip efficiency and $MOPIR = 4.83$. This topology requires a seven-phases voltage flip scheme. Increasing the number of switching phases to 21 phases [34] improves the $MOPIR$ to 9.3. However, the use of a large number of parallel flipping capacitors [32] increases the number of switching phases and hence the flipping time. This in turn reduces the conduction time and thus the extracted power.

Also, using the re-configurable flipping capacitors [19, 34] increases the number of required switches, which increases the ON resistance during one flipping phase and thus the flipping time. As a result, increasing the number of flipping capacitors or phases to improve the flipping efficiency implies fast voltage flip operation. This can be achieved only when C_{peh} is low. Otherwise, the use of large C_{peh} in such implementations significantly increases the charge loss and hampers the voltage flip and power efficiencies.

From (5), we can notice that the maximum output power is also related to the PT properties and more pointedly to the V_{oc} , the open circuit voltage of the PT. This voltage is induced by the mechanical excitation applied to the PT. The high mechanical excitation applied to the PT, the high V_{oc} value across the PT. We can also point out, from (5), that a small increase in V_{oc} significantly boosts the output power. Thus a low excitation level, i.e. $V_{oc} \leq 1V$, extremely limits the SSHC extracted power.

To overcome the limitations mentioned above, the following sections propose an optimized SSHC interface circuit. While the employed PT with a high parasitic capacitor C_{peh} is operating under low excitation conditions, the proposed circuit achieves high voltage flip efficiency using a reduced set of flipping capacitors.

3 FAR-FC interface circuit topology and design analysis

As we can see in Figure 2 (bottom), increasing the building voltage from V_b (red curve) to V_{b1} (blue curve) contributes to minimize the charge loss Q_{loss} . This increases the conduction time and thus the extracted power. Based on this observation, our proposed interface performs an efficient voltage flip thanks to an optimized implementation of SSHC circuit. Figure 3 shows the architecture of the proposed FAR-FC interface circuit. It mainly consists of: a Damping/Building capacitors array (D/B), an active AC/DC rectifier, a voltage regulator (VR) and a control block (CTRL). These blocks and their corresponding signals are detailed in the subsections below. Note that the circuit also features additional blocks, namely a ring oscillator (RO) [38], another voltage regulator (VR12) [32], a charge pump (CP) [39] and level shifters (LS) [32]. The VR12 is needed to provide the low power supply ($V_{DDL} = 1.2V$) mainly to the digital parts of the circuit (CTRL, RO), while the high power supply ($V_{DDH} = 3V$) is provided by the CP block to the rectifier and the LS. These latter are employed to ensure proper control and operation of the switches.

3.1 Damping/Building Capacitors Array (D/B)

This block is used to efficiently flip V_{peh} at each zero crossing moment of I_{peh} . The voltage flip operation is performed in nine phases using three re-configurable capacitors and eleven switches (Figure 3). As in the one-capacitor SSHC interface, V_{peh} inversion operation can be subdivided into: 1) damping

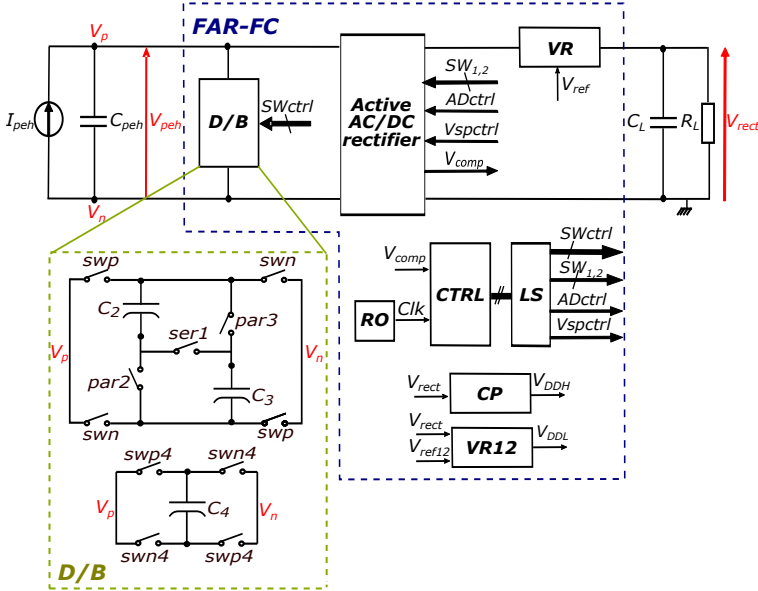


Fig. 3 FAR-FC interface circuit architecture.

phases (Φ_{-1} , Φ_{-2} , Φ_{-3} , Φ_{-4}) where C_{peh} is discharged through the flipping capacitors, 2) a shorting phase (Φ_0) to get rid of the remaining charge in C_{peh} , 3) building phases (Φ_4 , Φ_3 , Φ_2 , Φ_1) where C_{peh} is recharged from the flipping capacitors. Figure 4 shows the optimized 9-phase reconfiguration cycle at each V_{peh} inversion operation. In this configuration, a trade-off between the capacitors/phases numbers, power extraction efficiency and control complexity is made. This trade-off limits the maximum number of the switches connected in series to three during the D/B phases, which enables the use of PTs with large C_{peh} as explained further in this section.

Let's define n as the phase number and m as the voltage flip cycle number. After m voltage flip cycles, V_{peh} can be defined as $V_{d(n,m)}$ and $V_{b(n,m)}$ at the end of the damping Φ_{-n} and building Φ_n phases, respectively. Applying the conservative equations, these voltages can be expressed as follows:

$$V_{d(n,m)} = \frac{V_{d(n-1,m)}C_{peh} + V_{b(n,m-1)}C_n}{C_{peh} + C_n} \quad (8)$$

$$V_{b(n,m)} = \frac{C_{peh}V_{b(n+1,m)} + V_{d(n,m)}C_n}{C_{peh} + C_n} \quad (9)$$

In steady state, $V_{b(1,m)} = V_{b(1,m-1)}$. As a consequence, the voltage flip efficiency can be expressed by:

$$\eta_F = \frac{V_{rect} + V_{b(1,m)}}{2V_{rect}} \quad (10)$$

From (10), it is clear that increasing $V_{b(1,m)}$ leads to increase η_F . For such a configuration, fulfilling the condition $C_n \gg C_{peh}$ is not sufficient to reach

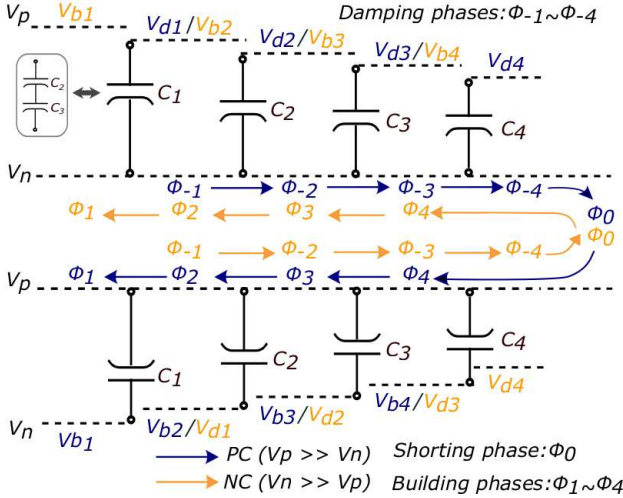


Fig. 4 Optimized 9-phase flipping capacitors configuration for PC and NC cycles.

the maximum $V_{b(1,m)}$ as in the one-capacitor SSHC interface. The choice of the capacitance values for this configuration is the key to optimize the voltage flip operation. The simplified calculation of $V_{d(n,m)}$ and $V_{b(n,m)}$ when $m = 1$ using (8) and (9) allows to find the condition to have $V_{b(1,1)}$ maximal. As a result $V_{b(1,1)}$ can be expressed as:

$$V_{b(1,1)} = \frac{C_{peh}C_1(C_{peh} + C_2)^2(C_{peh} + C_3)^2(C_{peh} + C_4)^2}{K} + \frac{C_{peh}^3C_2(C_{peh} + C_3)^2(C_{peh} + C_4)^2 + C_{peh}^5(C_{peh} + C_4)^2 + C_{peh}^7C_4}{K} \quad (11)$$

where $K = (C_{peh} + C_1)^2(C_{peh} + C_2)^2(C_{peh} + C_3)^2(C_{peh} + C_4)^2$. The previous equation (11) shows that maximum $V_{b(1,1)}$ is achieved when $C_1 < C_{2,3} < C_4$. This also applies to maximum $V_{b(1,m)}$. To fulfill this condition, we set $C_2 = C_3 = \frac{C_4}{2}$ and thus $C_1 = \frac{C_2C_3}{C_2+C_3} = \frac{C_{2,3}}{2}$. Based on the characteristics of the PT device (S118-J12S-1808YB) employed in our experiments, the parasitic capacitor C_{peh} is estimated to be $100nF$. To choose the capacitance values, theoretical simulation of the voltage flip efficiency η_F versus different $\frac{C_1}{C_{peh}}$ ratios was performed (Figure 5). Simulation results show that increasing $\frac{C_1}{C_{peh}}$ leads to increase η_F . However, for $\frac{C_1}{C_{peh}} > 5$, the improvement on η_F becomes negligible. Therefore, the value of C_1 is set to $5 \times C_{peh}$, i.e. $C_1 = 500nF$, $C_{2,3} = 1\mu F$ and $C_4 = 2\mu F$ in our case.

As mentioned above, this configuration requires eleven transmission gate switches (TG), represented in the D/B inset of Figure 3. Note that there are at most three TGs in series during the damping/building operation, i.e. when the D/B array is configured as C_1 . This helps containing the total series

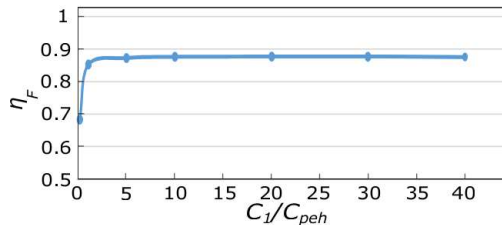


Fig. 5 Voltage flip efficiency η_F as a function of $\frac{C_1}{C_{peh}}$.

resistance at a low value during the charge transfer between C_{peh} and the flipping capacitors, and thus limits the total time (RC) required to accomplish the voltage flip operation. This is an important point because it allows to efficiently apply the SSHC voltage-flip technique even on PTs with C_{peh} as high as $100nF$ or above, and represents an improvement compared to the state-of-the-art works that report PTs with $C_{peh} = 45nF$ [32] or much less [37, 40].

Table 1 Summary of Control Signal Combination.

SWctrl	Control phase								
	Φ_{-1}	Φ_{-2}	Φ_{-3}	Φ_{-4}	Φ_0	Φ_4	Φ_3	Φ_2	Φ_1
swp	On/Off	On/Off	On/Off	Off	On	Off	Off/On	Off/On	Off/On
swn	Off/On	Off/On	Off/On	Off	On	Off	On/Off	On/Off	On/Off
ser1	On	Off	Off	Off	Off	Off	Off	Off	On
par2	Off	On	Off	Off	Off	Off	Off	On	Off
par3	Off	Off	On	Off	Off	Off	On	Off	Off
swp4	Off	Off	Off	On/Off	Off	Off/On	Off	Off	Off
swn4	Off	Off	Off	Off/On	Off	On/Off	Off	Off	Off

Table 1 shows the control sequence of each switch when V_{peh} is inverted from positive to negative ($V_p \rightarrow V_n$). The whole set of control signals is named $SWctrl$ in Figure 3. Individually, the switches are named after their control signals. That explains why some switches bare the same name in Figure 3. Note that when V_{peh} is inverted from negative to positive ($V_n \rightarrow V_p$), the control sequence for swp , swn , $swp4$ and $swn4$ switches is changed during certain phases as mentioned in red in Table 1.

3.2 Active AC/DC Rectifier

Figure 6 (left) shows the circuit diagram of this block. It consists of five switches named after their control signals and an active diode (AD) controlled by the CTRL block as shown in the following sub-sections. The rectification switches (SW_1, SW_2) are used to rectify the voltage across the PT. During the positive phase of V_{peh} , the switches controlled by SW_1 and SW_2 signals are ON and OFF, respectively and vice versa during the negative phase. As a

result, the node V_{sp} is permanently connected to the positive terminal of the PT, i.e. V_{peh} is rectified.

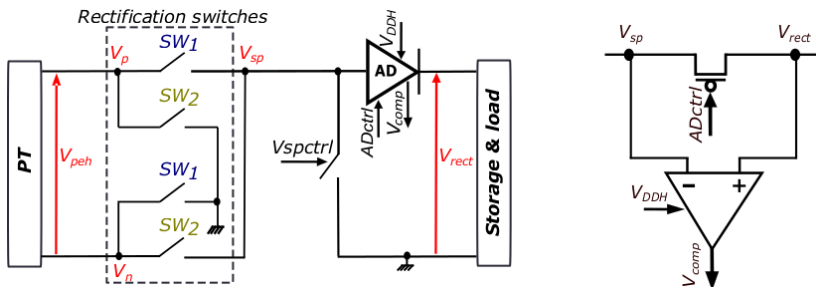


Fig. 6 Circuit diagram of active AC/DC rectifier (left), and the active diode (AD) (right).

The AD, shown in Figure 6 (right), is used to both prevent the current backflow from C_L to PT and detect the zero crossing moment of the PT current. It consists of an ultra-low power comparator [32] and a PMOS switch. When V_{rect} , the voltage across C_L , becomes larger than the voltage at node V_{sp} , i.e. the current changes its direction, the comparator output V_{comp} goes high. This signal is used by the CTRL block to both turn off the PMOS switch, thus preventing the discharging of C_L , and trigger the inversion of V_{peh} . Note that, during the damping phase, the AD is disconnected from the PT in order to ensure proper charge transfer from C_{peh} to the flipping capacitors. This disconnection sets the node V_{sp} in high impedance state, which leads to the false $I_{peh} = 0$ detection. To prevent this phenomenon, a switch controlled by signal V_{spctrl} is added to connect V_{sp} node to the ground during the damping phases.

3.3 Voltage Regulator (VR)

Figure 7 presents the circuit diagram of the on-chip voltage regulator VR. This block is used for both the overload protection and maximum power extraction requirements. In this voltage regulator, a common gate comparator presented in [23] is used to limit V_{rect} to a constant voltage V_{ref} which allows maximum output power extraction.

To evaluate the maximum output power extracted by FAR-FC circuit, the total charge that actually flows into C_L every cycle Q_{rect} is calculated. This amount of charge can be defined as the difference between the available charge from PT and the amount of charge lost every cycle to charge C_{peh} from V_b to V_{rect} :

$$Q_{rect} = Q_{peh} - Q_{loss} \quad (12)$$

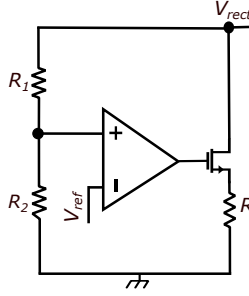


Fig. 7 Circuit diagram of the voltage regulator (VR).

The available charge from PT every cycle can be given by:

$$Q_{peh} = 4C_{peh} \hat{V}_{oc} = \int_0^{1/f_{ex}} I_{peh}(t) dt \quad (13)$$

where \hat{V}_{oc} is the amplitude of V_{oc} , and f_{ex} is the PT's excitation frequency. As the charge lost every cycle Q_{loss} can be calculated by:

$$Q_{loss} = 2C_{peh}(V_{rect} - V_b) \quad (14)$$

Therefore, Q_{rect} can be expressed as:

$$Q_{rect} = 2C_{peh} [2\hat{V}_{oc} - (V_{rect} - V_b)] \quad (15)$$

The extracted output power is given as:

$$P_{rect} = Q_{rect} V_{rect} f_{ex} \quad (16)$$

From (16) and (15), P_{rect} can be expressed as:

$$P_{rect} = 2C_{peh} V_{rect} f_{ex} [2\hat{V}_{oc} - (V_{rect} - V_b)] \quad (17)$$

The derivative of (17) shows that maximum output power is achieved when:

$$V_{rect} = \hat{V}_{oc} + \frac{V_b}{2} \quad (18)$$

This value is used as a voltage reference of the voltage regulator VR in order to extract the maximum of power. From (17) and (18), the maximum power extracted by the FAR-FC circuit can be expressed as:

$$P_{rectmax} = 2C_{peh} f_{ex} (\hat{V}_{oc} + \frac{V_b}{2})^2 \quad (19)$$

Therefore, the maximum output power improvement ratio of the FAR-FC circuit can be expressed as:

$$MOPIR_{FAR-FC} = \frac{P_{rectmax(FAR-FC)}}{P_{FBR(ideal)max}} = 2(\hat{V}_{oc} + \frac{V_b}{2})^2 \quad (20)$$

3.4 Control Block (CTRL)

The control block CTRL shown in Figure 8 generates the voltage flip control signals mentioned in Table 1, and the control signals of the rectifier block (Figure 6, left).

The AD's comparator output signal V_{comp} is used to trigger CTRL. Upon rising edge of V_{comp} , a lock signal ($Lock$) is generated to trigger the 9-phase sequence and lock the PMOS switch of AD in open state for the whole duration of the flipping process.

A counter 4bit, a decoder and a sequence generator are employed to generate the nine voltage flip phases. The counter is clocked by signal Clk generated by the a ring oscillator RO, previously mentioned. At the end of the voltage flip operation, an internal reset signal $RST-int$ prepares CTRL for the next voltage flip operation.

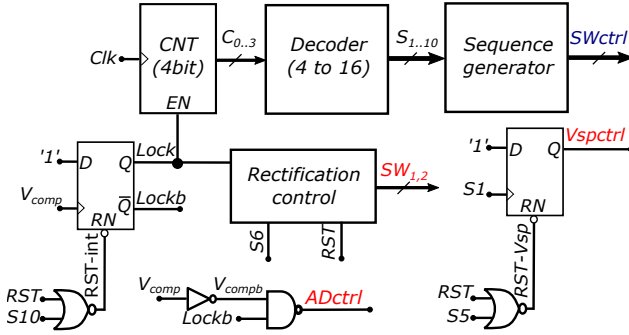


Fig. 8 Control block circuit (CTRL).

Figure 9 (top) details the structure of the sequence generator block. It generates the vector of non-overlapping signals $SWctrl$ presented in Table 1, that control de D/B array (see 3.1). Figure 10 shows the timing diagram of the signals generated by both the sequence generator and the rectification control circuits.

In normal operation mode and during the first and the last phases Φ_{-1} , Φ_1 , signal $ser1$ is set high to connect C_2 and C_3 in series, thus forming the equivalent capacitance C_1 . When the D flip flop is enabled by $S1$, signal $ser1$ goes low at the end of Φ_1 , and returns again to high when the D flip flop is reset by an internal signal when the last phase Φ_1 starts ($S_9 \cdot \overline{S_8}$). Signal $par2$ is generated when $S2$ or $S8$ is high, i.e during Φ_{-2} and Φ_2 . Signal $par3$ is generated when $S3$ or $S7$ is high i.e during Φ_{-3} and Φ_3 . To control the polarity of C_1 , C_2 and C_3 while connecting with C_{peh} , either swp or swn is set high depending on whether V_{peh} is positive or negative, respectively. Furthermore, both swp and swn are set high during Φ_0 , which corresponds to the shorting of C_{peh} . Signals swp and swn are generated by three internal signal $swpb0$, $swnb0$ and $sw0b$ determined by the phase combinations (Φ_{-1} , Φ_{-2} , Φ_{-3}), (Φ_1 , Φ_2 , Φ_3) and Φ_0 , respectively. Since C_4 is independent from C_1 , C_2 and C_3

it only requires signals $swp4$ or $swn4$, which are set high during Φ_{-4} or Φ_4 depending on whether V_{peh} is positive or negative.

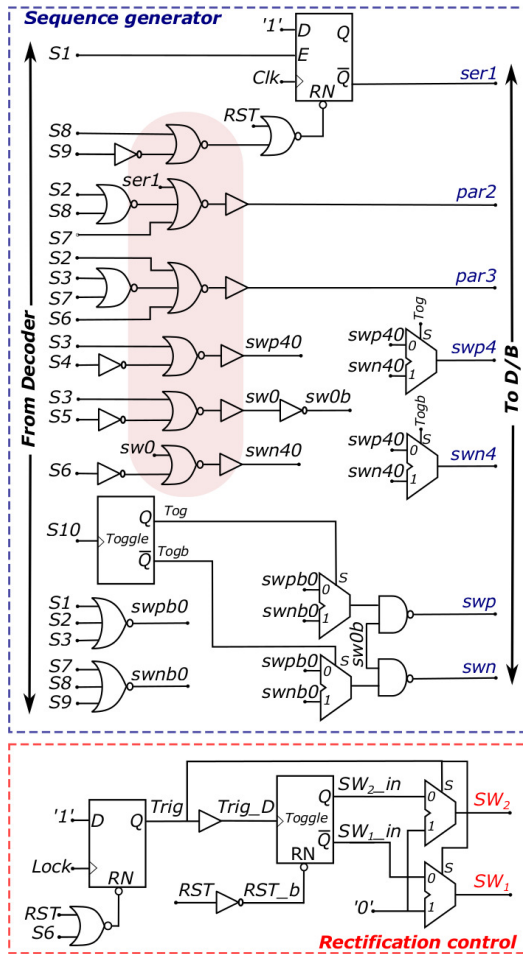


Fig. 9 Sequence generator circuit (top), Rectification control circuit (bottom).

Finally, a toggle is triggered at the end of each 9-phase generation process to swap states between swp and swn so the polarities of C_1 , C_2 and C_3 match the polarity of C_{peh} on the next voltage flip. Also, in order to match the polarities of C_4 and C_{peh} , the same toggle used in this block is employed to swap states between $swp4$ and $swn4$.

The duration PW (Figure 10) of each phase depends on the time required to ensure proper charge transfer between C_{peh} and the flipping capacitors. PW is set using a clock divider of the clock generator RO and can be tuned externally. It should be noted here that to avoid overlap between two successive

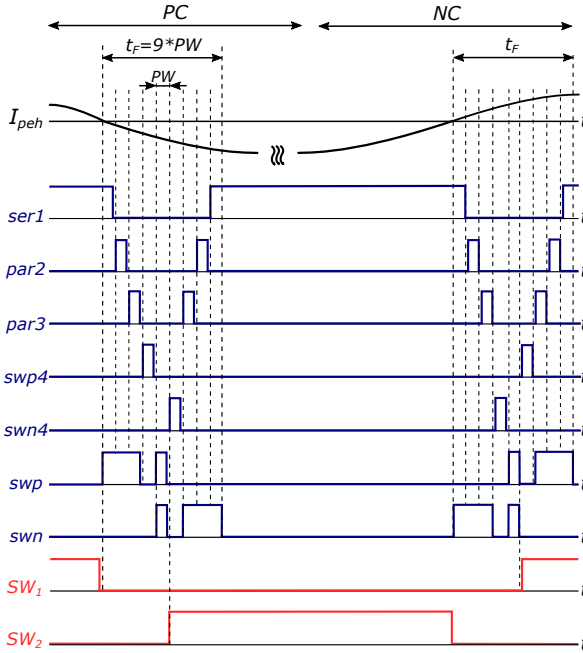


Fig. 10 Timing diagram of the control signals sequence at zero-crossing moments of I_{peh} .

signals, additional NOR and DELAY logic gates are employed (see shaded zone of the sequence generator part in Figure 9). This is important to avoid false connection between flipping capacitors nodes during the charge transfer operation, which would significantly impact the system's efficiency.

The circuit of the rectifier's control block is shown in Figure 9 (bottom). During each positive and negative alternation of V_{peh} , SW_1 and SW_2 signals are set high, respectively to connect the positive terminal of PT to node V_{sp} , and the negative terminal to ground. Furthermore both signals are set low during the damping and shorting phases to disconnect C_{peh} from C_L . This ensures proper charge transfer from C_{peh} to the flipping capacitors during the damping phases by isolating PT and D/B from the rest of the circuit.

The rectification process is realized as follows: when the damping phases start, the rising edge of V_{comp} sets the $Trig$ signal high. As a result, both SW_1 and SW_2 signals are set low, which disconnects C_L from the PT. At the end of the damping phases, signal $Trig$ goes low, and then both SW_1 and SW_2 are set to $SW_1.in$ and $SW_2.in$, respectively. The latter are the outputs of a toggle clocked by the delayed $Trig$ signal, $Trig.D$. The rectification process is also reset by the signal $RST.int$, which sets low signal $Lock$ until the next voltage flip operation.

The need for disconnecting PT from C_L during the whole voltage flip sequence imposes high impedance state at node V_{sp} , which causes its voltage to rise because of the charge injection effect in the parasitic capacitances of switches SW_1 and SW_2 . This in turn could lead V_{comp} to go low (i.e. if

$V_{sp} > V_{rec}$), which would turn on the PMOS switch of the AD while it should stay off until the voltage flip terminates. To prevent this phenomenon, this switch is controlled by signal $ADctrl$ (Figure 8). Furthermore, the control block generates signal $Vspctrl$ that ties node V_{sp} to ground during the damping period (Figure 8). This prevents spurious behaviour of the AD comparator that would increase the power consumption of the circuit.

3.5 Transistor-level simulations

The FAR-FC interface circuit has been simulated with Cadence[®] at transistor-level simulation, using the AMS-0.35 μ m CMOS technology parameters. The model of the PT used in FAR-FC simulations is based on the off-the-shelf device S118-J12S-1808YB by Piezo.com with $C_{peh} = 100nF$, which we also used in our experiments. \hat{I}_{peh} and f_{ex} were set to 62.8 μ A and 100Hz in order to have an open circuit voltage amplitude $\hat{V}_{oc} = 1V$, which corresponds to a low mechanical excitation level. For these simulations, we set $V_{rect} = 1.2V$ as an initial condition of the storage capacitor $C_L = 100\mu F$. For FAR-FC performance comparison, the SSHC circuit presented in [32] with three parallel capacitors (3cap-SSHC), i.e. with the same number of FAR-FC flipping capacitors, is also simulated. Figure 11 shows the simulated V_{peh} and V_{rect} without regulation for the two circuits. Even though the output voltage V_{rect} of both architectures rises close to $2\hat{V}_{oc} = 2V$, the zoom view shows yet that, in steady state, i.e. when C_L is completely charged, the maximum V_b achieved by the 3cap-SSHC is 1V while V_b reaches 1.5V in the FAR-FC. According to (18), in order to extract the maximum power generated by the PT, the output voltage of FAR-FC and 3cap-SSHC should be regulated to 1.75V and 1.5V, respectively. Taking into account the parasitic charge losses, V_{rect} was regulated to 1.6V and 1.35V in the FAR-FC and the 3cap-SSHC circuits, respectively, which are more realistic (Figure 12). The zoom view shows, that in steady state, the maximum V_b is only 810mV in 3cap-SSHC, which yields a maximum output power of 39.48 μ W according to (19). In contrast, the maximum V_b is 1.3V in FAR-FC, which corresponds to a maximum extracted power of 54.45 μ W. In addition, the simulations also confirm that the voltage flip efficiency of FAR-FC is higher than in 3cap-SSHC, with 90.6% and 80%, respectively, according to (10).

The maximum output of a non-ideal FBR can be expressed as $P_{FBRmax} = C_{peh}f_{ex}(\hat{V}_{oc} - 2V_{th})^2$ [22]. Therefore, the maximum output power extracted by a CMOS-diode-based FBR ($V_{th} = 0.3V$) is 1.6 μ W. Hence, the theoretical maximum output power ($MOPIR$) of the FAR-FC architecture yields 28 \times improvement compared to an FBR.

Figure 13 details the simulated behaviour of V_{peh} and the AD's comparator output V_{comp} , which is the key signal in the zero-crossing detection process of I_{peh} . The zoomed-in view shows that the comparator trips 30 μ s ahead of the actual zero crossing moment of I_{peh} . This is due to the negative offset of the AD comparator. However, as the $delta = 30\mu$ s represents only 0.6% of half the period of I_{peh} , it has negligible impact on the system's efficiency. Figure

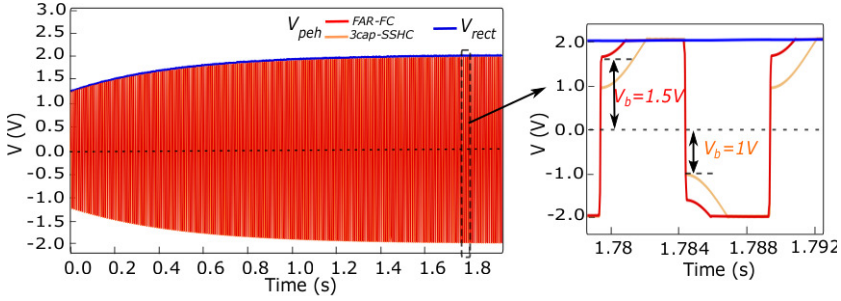


Fig. 11 Simulated V_{peh} and V_{rect} of the 3cap-SSHC [32] and the proposed FAR-FC architectures, with no regulation.

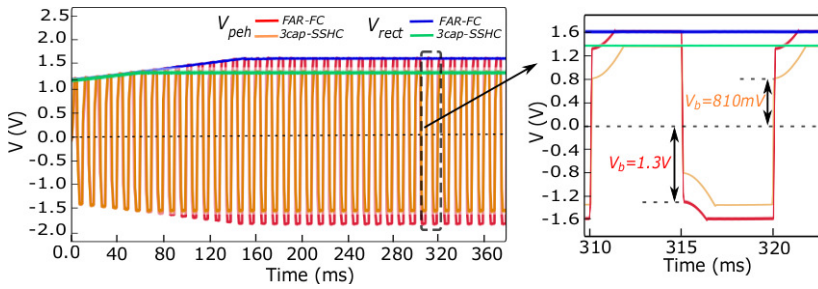


Fig. 12 Simulated V_{peh} and V_{rect} of the 3cap-SSHC [32] and the proposed FAR-FC architectures, with regulation.

13 also shows that V_{comp} returns to zero after the comparator has tripped. As mentioned in 3.4, this is due to the charge injection on V_{sp} after disconnecting this node from both C_L and C_{peh} . For this reason, connecting the node V_{sp} to ground and blocking the AD during the voltage flip operation is mandatory to avoid the instability of the AD comparator, which would lead to a significant increase in its consumption and affect the system's efficiency.

4 Experimental results and discussion

The FAR-FC prototype was designed and fabricated in AMS-0.35 μ m CMOS technology. Figure 14 shows the micrograph of the ASIC (left) with all the featured blocks outlined, and the measurement setup (right). All blocks are fully integrated except the D/B block where the 3 flipping capacitors mentioned in section 3 are implemented off-chip. The active area of the ASIC is 7.29 mm^2 and the estimated total volume occupied by the off-chip flipping capacitors is about 5.4 mm^3 . The PT is excited by an LDS[®] V400 series shaker, driven by an AC power source 6813B by Agilent[®]. The excitation signal is a 100 Hz sine waveform. The mechanical acceleration of the shaker was set so as to get $\hat{V}_{oc} = 1V$. A LabVIEW[®] platform performs both the control of the shaker and the signal acquisition via an oscilloscope. The extracted energy is stored on a conventional capacitor $C_L = 100\mu F$.

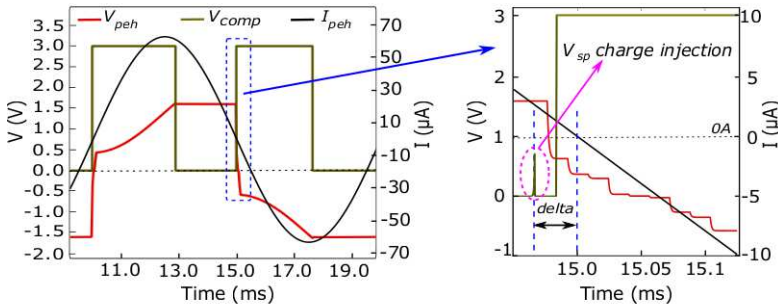


Fig. 13 Waveforms of V_{pch} , V_{comp} and I_{pch} . The zoomed-in view (right) shows the offset of the AD comparator and the glitchy behaviour of V_{comp} due to the charge injection in SW_1 and SW_2 .

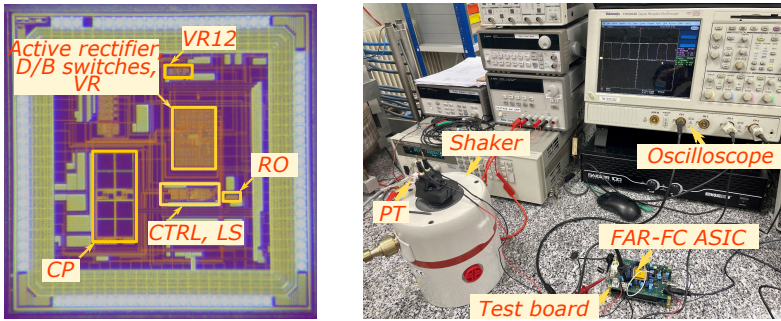


Fig. 14 FAR-FC ASIC micrograph (left), and Measurement setup (right).

Figure 15 (left) shows the measured waveform of V_{pch} and V_{rect} . As V_{rect} is regulated to 1.6V, the voltage across C_{pch} is about $V_b = 1.24V$ after the voltage inversion operation. This corresponds to 88.75% voltage flip efficiency. This value is slightly lower but yet very close to the simulated one (90.6%). The reason is the series resistance of the T-gate switches combined to total parasitic capacitance of the interconnections between the test board and the PT which increase the time constant. Figure 15 (right) shows the detailed evolution of V_{pch} during the 9-phase voltage flip operation. A phase duration $PW = 32\mu s$ was empirically determined to reach the optimal voltage efficiency mentioned above.

To evaluate the performance of the FAR-FC, we measured the output power. For this experiment, we connected a variable resistor to the FAR-FC output and disabled the voltage regulator. Figure 16 shows the output power of FAR-FC for different V_{rect} compared to the output power of an off-chip Schottky-diode based FBR. The measured threshold voltage of the Schottky diodes is around ($V_{th} \approx 0.05V$). This yields a maximum output power of $7.98\mu W$ when $V_{rect} = 0.4V$. With FAR-FC, the maximum output power

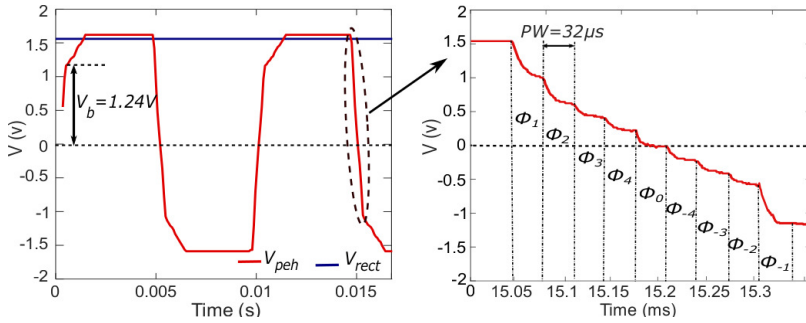


Fig. 15 Measured waveform of V_{pch} and V_{rect} (left), Zoom of view of V_{pch} inversion phases (right).

increases to $45\mu W$ at $V_{rect} \approx 1.6V$ leading to a $MOPIR$ of 5.64. This result is consistent with the theoretical $MOPIR$ estimated in 3.5 because the threshold voltage at low current of the Schottky diodes is much lower than that of integrated silicon diodes. Figure 16 (left) also shows that for V_{rect} lower than $0.9V$, the FAR-FC turns off. In fact, for $V_{rect} = 0.9V$, the output voltage of the integrated charge pump CP, normally dedicated to supply the circuit with $3V$, decreases to $1.8V$, which is not sufficient to fully turn ON/OFF the TG switches in this technology.

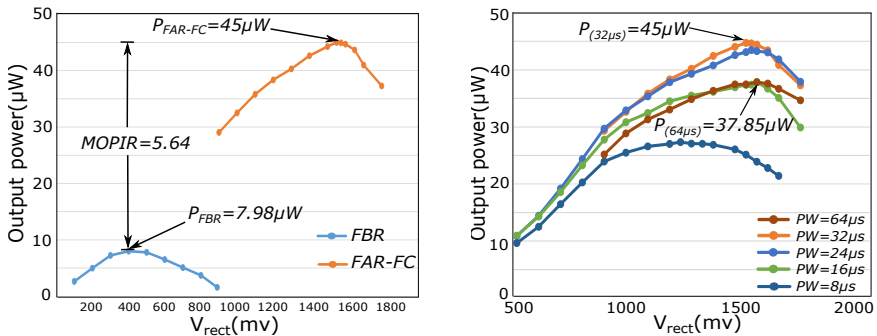


Fig. 16 Output power of both FBR and FAR-FC (left), FAR-FC output power for different PW duration (right).

We also measured the FAR-FC performance for different pulse widths PW as shown in Figure 16 (right). It is clear that best power performance is achieved when PW is set to $32\mu s$. Furthermore, increasing the pulse width to more than $32\mu s$ leads to decrease the conduction time and thus to decrease the output power.

Table 2 lists the measured power consumption of the different blocks of FAR-FC circuit. The total consumption is $4.24\mu W$ representing 9.42% of the total extracted power and 90.58% system efficiency.

Table 2 Measured Power Breakdown of FAR-FC.

Block	Power loss	percentage
Active rectifier+VR	$2.01\mu W$	47.45%
CP	$4nW$	0.094%
VR12	$485nW$	11.44%
CTRL+LS	$1.6\mu W$	37.74%
RO	$140nW$	3.3%

Table. 3 summarizes the key characteristics and performance of the proposed FAR-FC chip compared with the reported state-of-the-art architectures. As can be noticed, most interface circuits presented in the literature report \hat{V}_{oc} higher than 1V. It is thus difficult to make a fair comparison with our work. However, [37] report about the output power when $V_{oc} \simeq 1V$. As can be noticed, the maximum extracted power in [37] significantly decreases from $24.2\mu W$ to $4.7\mu W$ when the \hat{V}_{oc} decreases from 2.75V to 1.02V. In contrast, the FAR-FC circuit can extract $45\mu W$, which is $9.5\times$ higher than the maximum power extracted by [37]. This table also shows that the proposed FAR-FC can work with a high PT inherent capacitance value, i.e. $100nF$, while the value reported in the state of the art circuits is lower than $50nF$. In particular, SSHC architectures that require a large number of phase [32], [34], [40] need to keep C_{peh} as low as possible to limit the RC constant that hampers the voltage flipping speed. The optimized architecture of FAR-FC, combining the reduced nine-phases flipping process and the reduced maximum number of series switches (i.e. 3) in the D/B array, alleviates the constraint on the C_{peh} compared to other works, extending the variety of the PTs compatible with the proposed energy harvesting interface.

5 Conclusion

This paper presented an optimized SSHC interface circuit (FAR-FC) for piezoelectric energy harvesting. While the reported state-of-the-art architectures use either a large inductor (SSHI) or a large number of flipping capacitors/phases (SSHC), the FAR-FC employs only three flipping capacitors to achieve high power efficiency. Simulation results shows that the FAR-FC improves the voltage flip efficiency by 10.6% compared to the state-of-the-art three-capacitor SSHC circuit. This yields 37.91% maximum output power improvement. Moreover, measurement results show that the FAR-FC circuit can deliver up to $45\mu W$ with 88.75% voltage flip efficiency when \hat{V}_{oc} is only 1V, while most state-of-the-art works report $\hat{V}_{oc} > 2V$. This ensures sufficient energy harvesting even under tight operation conditions, i.e. the PT is weakly excited. Measurement results also reveals that the FAR-FC achieves $5.64\times$ power performance improvement compared to a conventional diode-based FBR. Furthermore, its optimized architecture allows the proposed FAR-FC circuit to be used with a wide range of PT capacitance (C_{peh}) values, i.e. up to $100nF$ or more.

Table 3 FAR-FC Performance Compared to the State of the Art.

Publication	Wu et al.[41]	Du et al.[32]	Du et al.[40]	Chen et al.[34]	Ciftci et al.[37]	This work
Year	2017	2017	2019	2019	2021	2022
CMOS technology	0.25 μm	0.35 μm	0.18 μm	0.18 μm	0.18 μm	0.35μm
Harvesting technique	SSHI	SSHC	SSHC	SPFCR	SSHCI	SSHC
f_{ex} (Hz)	144	92	219	200	415	100
C_{peh} (nF)	19	45	1.94	22	2	100
Key components	Inductor	8 capacitors	8 capacitors	4 capacitors	Inductor+capacitor	3 capacitors
Number of phases	-	17	17	21	-	9
V_{oc} (V)	4.9	2.5	2.5	1.6	2.75-1.02	1
Output power (μW)	136	161.8	16.1	64	24.2-4.7	45
<i>MOPIR</i>	2.1	9.7	8.2	9.3	4.03-5.44	5.64

The future work is currently addressing a dynamic FAR-FC able to deal with varying mechanical excitation (i.e. different values of \hat{V}_{oc}).

6 Declarations

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The authors declare that they have no competing interests as defined by Springer, or other interests that might be perceived to influence the results and/or discussion reported in this paper.

Liana Wassouf and Vincent Frick wrote the main manuscript text. Liana Wassouf prepared figures 1-13 and 15-16, tables 1-3. Ehsan Jamshidpour contributed in the elaboration of figure 3. Vincent Frick prepared figure 14. All authors reviewed the manuscript.

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