



Caractérisation, analyse et modélisation du MOSFET de puissance en carbure de silicium

Dinh-Lam Dang

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L'Université de Lorraine

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Spécialité: Génie Electrique

par

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Master diplômé de L'Institut polytechnique de Hanoi

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*Cho tình yêu của bố mẹ
Cho giấc mơ của con....*

To my beloved parents

Abstract

Silicon carbide (SiC) has actively been emerged as the most viable candidate of the wide band gap (WBG) semiconductors to replace silicon (Si) in the near future. Due to its inherent properties, SiC enables the development of new generation semiconductor devices that offer great performance improvements, resulting in more efficient and compact designs in various power electronics applications. The 1.2 kV SiC MOSFETs, which are by far the most important devices in the SiC family, have been quickly used as the replacement of Si IGBTs in many applications due to their superior characteristics. However, at an early stage of development, SiC MOSFETs come with their own list of technical and economic issues which have somehow limited their widespread implementation for power electronics applications.

The characterization and modeling, in particular on-state of the SiC MOSFET, have been investigated in this dissertation to develop insight of the unique characteristics along with the effects on the design of power converters.

In such a way, the characterization test benches for high voltage power MOSFETs have been developed. The device is characterized using appropriate methods, which allows the junction temperature to remain constant during the measurement. The characteristics are then analyzed and compared to these of Si counterpart to provide further understanding of SiC MOSFETs. Subsequently, a novel compact model has been developed for circuit simulation, taking into account physical phenomena including interface traps, short-channel, intrinsic JFET and temperature effects. As a modified version of the Shichman Hodges, the model employs a few adjustment parameters, which are mostly derived from curve fitting of experimental data, using optimization tool software. The proposed model with fairly simple current equation thus is expedient to represent the DC behavior of power MOSFET for a wide range of operation conditions. In the end, the thermal characterization of SiC MOSFETs is examined. The on-resistance has been proposed as a temperature-sensitive electrical parameter (TSEP) to estimate the junction temperature. In the presence of the interface traps, the dedicated test benches have been developed for SiC MOSFET temperature measurement based on TSEP. 3D Finite element (FEM) simulation is performed to investigate thermal distribution inside the module. By comparing with the experiments, the electro-thermal model is validated with acceptable accuracy.

Keywords: SiC, MOSFET, I-V characteristics, modeling, thermal measurement, TSEP

Résumé

Le carbure de silicium (SiC) semble être actuellement le candidat le plus viable des semi-conducteurs à large bande interdite pour remplacer le silicium (Si) dans un avenir proche. En raison de ses propriétés intrinsèques, le SiC permet de développer des dispositifs à semi-conducteurs aux caractéristiques supérieures offrant de grandes améliorations de performances, et se traduisant également par des conceptions plus efficaces et compactes dans diverses applications de l'électronique de puissance. Les MOSFET de 1,2 kV SiC, de loin les composants les plus répandus de la famille pour équiper les sources de puissance, ont rapidement été déployés pour remplacer les modules IGBT Si en raison de leur résistance à l'état passant faible et de leurs excellentes performances de commutation dans toutes les plages de température. Cependant, encore à un stade précoce de développement, les MOSFET SiC présentent leurs problèmes techniques et économiques propres, lesquels problèmes ont freiné leur expansion en électronique de puissance.

La caractérisation et la modélisation, en particulier l'état de fonctionnement du MOSFET SiC, ont été examinées dans le cadre de cette thèse afin de mettre en lumière les spécificités et les conséquences qui en découlent sur la conception des convertisseurs de puissance.

C'est ainsi qu'une méthodologie de caractérisation statique pour les MOSFET à haute tension a été développée. Les caractéristiques ont été mesurées par méthodes appropriées permettant à la température de la jonction de rester constante pendant la mesure. Les résultats expérimentaux ont été analysés et comparés à ceux relatifs aux dispositifs conventionnels en Si. Ensuite, un nouveau modèle compact du module MOSFET SiC a été mis au point sur le logiciel Saber pour des simulations orientées circuit. Ce modèle prend en compte les phénomènes physiques observés, notamment les effets des pièges d'interface, le comportement JFET intrinsèque, le canal court et la température. En tant que version modifiée de Shichman Hodges, le modèle utilise un nombre raisonnable de paramètres d'ajustement, lesquels sont principalement extraits par identification des courbes de données expérimentales à l'aide d'un logiciel d'optimisation, et pour les autres étant basés sur les données disponibles dans la fiche technique du composant étudié. Finalement, nous avons abordé la caractérisation électro-thermique des MOSFET de SiC. Pour remédier à la présence de pièges d'interface, des bancs de test dédiés ont été développés pour la mesure de la température MOSFET au SiC sur la base du TSEP. Une simulation par éléments finis 3D (FEM) est réalisée pour étudier la distribution thermique à l'intérieur du module. En comparant avec les expériences, le modèle électro-thermique a été validé avec une précision acceptable.

Mots-clés: SiC, MOSFET, caractéristiques I-V, modélisation, mesure thermique, TSEP

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List of Abbreviations and Symbol

N	The doping density (cm^{-3})
N_A	Acceptor doping concentration (cm^{-3})
N_D	Donor doping concentration (cm^{-3})
q	The electronic charge (1.6×10^{-19} C)
K_B	Boltzmann's constant ($1.38066 \cdot 10^{-23}$ J/K)
T	Temperature ($^{\circ}\text{C}$)
n_i	Intrinsic carrier concentration (cm^{-3})
A	Area (cm^2)
C_{OX}	Oxide capacitance (F)
t_{OX}	Oxide thickness (mm)
BJT	Bipolar junction transistor
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal oxide semiconductor field effect transistor
JFET	Junction Field Effect Transistor
SBD	Schottky barrier diodes
D_{it}	Density of interface traps ($\text{cm}^{-2} \text{eV}^{-1}$)
E_{BR}	Breakdown electric field (MV/cm)
E_C	Conduction band (eV)
E_V	Valence band (eV)
E_G	Energy band gap (eV)
E_F	Fermi level (eV)
χ	Electron affinity (eV)
Φ_B	Schottky barrier (eV)
Φ_M	Metal work function (eV)
Φ_S	Semiconductor work function (eV)
Φ_{MS}	Difference between metal and semiconductor work functions (eV)
φ_s	Surface potential (V)
φ_s	Fermi potential (V)
V_{DS}	Drain-source voltage (V)
V_{GS}	Gate-source voltage (V)
V_{FB}	Flat-band voltage (V)
V_{TH}	Threshold voltage (V)
g_m	Transconductance (S)
I_{DS}	Drain-source current (A)
I_{DSsat}	Saturation drain-source current (A)
L	Length of the MOSFET channel (μm)
W	Width of the MOSFET channel (μm)
ϵ_0	Vacuum permittivity (8.85×10^{-14} F/cm)
ϵ_s	Dielectric constant of the semiconductor
ϵ_{Si}	Dielectric constant of the silicon ($11.7 \times \epsilon_0$)
ϵ_{OX}	Dielectric constant of gate oxide ($3.97 \times \epsilon_0$)
μ_e	Electron mobility (cm^2/Vs)

μ_p	Hole mobility (cm^2/Vs)
μ_{inv}	Inversion layer mobility (cm^2/Vs)
v	Electron drift mobility (cm/s)
ρ	Resistivity (Ωcm)
θ	Thermal conductivity (W/cmK)
X_D	Width of drift region (cm)
W_D	Width of depletion region (cm)

Introduction générale

Contexte de l'étude

De principe similaire au MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) de signal, le MOSFET de puissance présente une géométrie différente avec une structure verticale où la source et le drain sont placés respectivement au-dessus et en dessous de la matrice de silicium. La première génération de MOSFET de puissance a été commercialisée au début des années 1980 par International Rectifier. Cette technologie, désignée par DMOS, met en œuvre une procédure de fabrication par double diffusion et une grille planaire, elle offre des capacités de blocage jusqu'à 300V. Dans les années 1990 est apparue la structure à grille en tranchée. Connue comme étant la seconde génération de MOSFET de puissance, elle a été commercialisée sous l'appellation TrenchFET par l'entreprise Vishay Siliconix. Le TrenchFET présente une nette supériorité sur le DMOS en terme de résistance à l'état passant et de charge de grille pour les produits spécifiquement en deçà de 100V. La superjonction CoolMOS, désignée comme la troisième génération de MOSFET de puissance, a été mise au point par Siemens (désormais Infineon) en 1999. Celui-ci apporte des avancées considérables par la mise en œuvre d'une nouvelle structure permettant de bloquer des tensions de 600V.

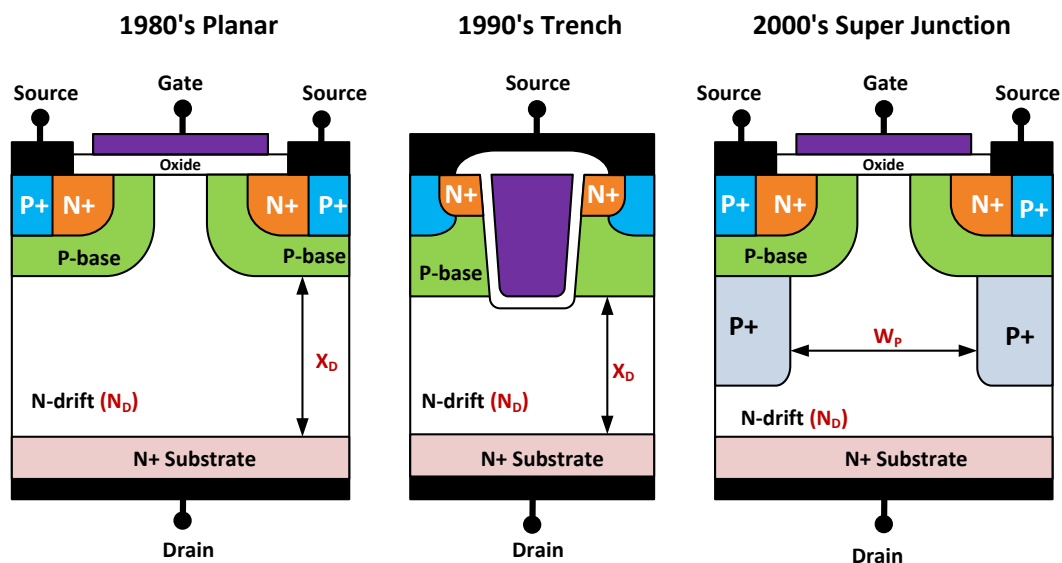


Figure 1. Comparaison des structures MOSFET à grille planaire, à grille en tranchée et superjonction

Le MOSFET de puissance exhibe plusieurs avantages au premier rang desquels une haute impédance d'entrée, des commutations rapides et un bon rendement (sous l'effet de faibles pertes par commutation et par conduction). Ces caractéristiques bénéfiques ont favorisé son introduction en électronique de puissance dans les applications de fréquences allant de 300 kHz à 2 MHz (convertisseurs DC/DC, onduleurs...). Quand bien même la technologie MOSFET de puissance a été en constante amélioration durant 30 ans sur de nombreux aspects, la tenue en tension est néanmoins restée limitée à la plage 100 V à 600 V. Par conséquent, les IGBT (Insulated Gate Bipolar Transistors) représentent l'alternative au MOSFET pour les tensions supérieures à 600 V.

Une vue en coupe des trois générations de MOSFET de puissance est présentée schématiquement en Figure 1, il est clairement observable que la capacité de blocage du composant repose sur la combinaison de deux paramètres de la région épitaxiée N, l'épaisseur (X_D) d'une part et le dopage (N_D) d'autre part. La résistance spécifique (i.e. résistance par unité de surface) $R_{ON,sp}$ est quant à elle déterminée pour une certaine tension de claquage V_{BR} selon l'expression (0-1). $R_{ON,sp}$ augmente avec V_{BR} à la puissance 2.4, de là découle un compromis entre tenue en tension et perte à l'état passant, lequel constitue le frein majeur à l'entrée du MOSFET de puissance dans le domaine des hautes tensions. La version superjonction ouvre la voie à un gain substantiel par l'augmentation de la tenue en tension tout en maintenant une résistance à l'état passant raisonnable. La dépendance de $R_{ON,sp}$ vis-à-vis de V_{BR} n'étant plus qu'une relation linéaire, il apparaît des bénéfices évidents en termes de pertes à l'état passant.

$$R_{ON,sp} = 8.9 \times 10^{-19} \times V_{BR}^{2.4} \quad (\Omega \cdot \text{cm}^2) \quad (0-1)$$

$$R_{ON,sp(SJ)} = 0.198 \times W_p^{5/4} \times V_{BR} \quad (\Omega \cdot \text{cm}^2) \quad (0-2)$$

Des innovations technologiques tant au niveau de la structure planaire que de la structure superjonction ont permis l'amélioration des performances. Néanmoins le taux d'amélioration du MOSFET de puissance à base de silicium a diminué au fur et à mesure de la convergence vers la valeur théorique.

Le MOSFET de puissance a cependant connu un regain d'attention dernièrement pour les futures applications en électronique de puissance grâce à la mise en œuvre du carbure de silicium (SiC). Combinant les excellentes propriétés du carbure de silicium avec les avantages potentiels du MOSFET, le MOSFET SiC a très nettement dépassé les limites théoriques du MOSFET Si, en atteste sa capacité de blocage de tensions allant de 1.2 kV à 1.7 kV. Le MOSFET SiC de puissance présente une plus faible résistance à l'état passant, des pertes moindres en commutation et des potentialités de fréquence de découpage plus élevées eu égard aux IGBT de calibre en tension équivalent. En tant que composant naturellement ouvert, le MOSFET SiC tout autant que l'IGBT Si peut donc être mis à profit pour la conception de convertisseur d'électronique de puissance.

Résultats et contributions essentiels

Quand bien même le MOSFET SiC s'annonce prometteur, il n'est pas encore arrivé à pleine maturité de développement technologique, il soulève encore des inquiétudes en terme de fiabilité et ses performances pratiques n'ont toujours pas rejoint les valeurs théoriques. Les MOSFET SiC et Si sont fabriqués et dimensionnés selon des principes similaires, cependant le MOSFET SiC présente des propriétés comportementales qui lui sont propres. Par conséquent, il est nécessaire d'identifier clairement ces particularités de sorte à tirer le meilleur parti du MOSFET SiC lors de son implémentation dans un environnement d'électronique de puissance. Par ailleurs, la disponibilité d'un modèle précis est de première importance pour réaliser des simulations numériques et des prédictions quelle que soit l'application envisagée. Par conséquent un travail préalable de caractérisation expérimentale et de modélisation est nécessaire et il fait actuellement l'objet de nombreux programmes de recherche aussi bien académiques que de la part des acteurs du secteur industriel.

Le présent document est composé de cinq chapitres traitant respectivement de l'état de l'art sur les composants à large bande interdite, du MOSFET de puissance, de sa caractérisation, de sa modélisation électrique puis thermique. Le détail de chaque chapitre est abordé dans les sections suivantes.

Le chapitre 1 est un état de l'art sur les composants à large bande interdite, il aborde les aspects technologiques des composants à base de carbure de silicium. Le chapitre débute avec les particularités des matériaux à large bande interdite et il souligne les avantages que l'on peut en extraire pour en faire des composants de puissance en électronique de puissance. Ce chapitre montre que les propriétés physiques de ces composants leur permettent d'opérer à haute température, à tension élevée et à haute fréquence. Pour des raisons économiques et technologiques, les composants SiC ont connu un meilleur essor que leurs homologues GaN. C'est la raison pour laquelle les composants SiC dominent actuellement le marché. Les composants essentiels de l'électronique de puissance sont passés en revue pour dégager les propriétés spécifiques des composants SiC. Les composants unipolaires ont été commercialisés récemment, lesquels exhibent des performances électriques intéressantes avec de faibles pertes par commutation et conduction. Malheureusement les composants SiC rencontrent encore des difficultés technologiques qui limitent leur mise en œuvre dans des systèmes exigeant une fiabilité irréprochable. Eu égard à la métallisation du SiC, la majorité des contacts métal semi-conducteur N sont des contacts Schottky. En outre, il est difficile de concevoir un contact ohmique avec le SiC, en particulier avec les dopages P. Les composants de type MOS à large bande interdite rendent plus basse la barrière que les électrons doivent franchir pour accéder à l'oxyde, ce qui conduit à de sérieuses difficultés en terme de fiabilité pour les applications à haute température.

Le chapitre 2 est entièrement dédié au MOSFET de puissance. Il débute par une introduction à la physique et à la structure des deux modèles disponibles sur le marché, en l'occurrence les structures à grille plane et à grille en tranchée. Le chapitre s'oriente ensuite vers une analyse détaillée des difficultés technologiques propres au MOSFET SiC à double implantation, lesquels présentent un principe d'opération et une procédure de fabrication pourtant similaire à leurs homologues Si. Les caractéristiques statiques aux états fermé et ouvert sont considérées en ce qui concerne la structure à grille plane. La discussion porte ensuite sur les problèmes liés à l'oxyde de grille SiO_2 . La présence d'atomes de carbone dans le composé SiC induit une interaction entre les entités C, SiC et SiO_2 de façon complexe. La densité de défauts à l'interface semi-conducteur-oxyde de grille (SiC-SiO_2) a été évaluée à des ordres de grandeur 2 à 3 fois supérieurs à ceux rencontrés dans l'interface SiC- SiO_2 . La densité D_{it} en question est composée de trois types de pièges, (centres P_b , groupes C et pièges de proche interface), elle est représentée sur la Figure 2. En particulier, la plus haute densité de piège est située à seulement 0.1 eV en dessous de la bande de conduction du semi-conducteur 4H-SiC, elle est à l'origine de la capture d'électrons et elle affecte significativement les caractéristiques en conduction du canal d'inversion sous la grille.

L'occupation des états d'interface, i.e. le nombre de charges piégées, dépend à la fois de la température et de la tension V_{GS} appliquée sur la grille. Par conséquent, le nombre de porteurs libres dans le canal, la tension seuil et la mobilité doivent être considérés comme fonction de la température et de la tension V_{GS} . Plusieurs clarifications et discussions sont développées dans le chapitre à ce sujet. Des précautions d'usage doivent être respectées pour tirer le meilleur parti des MOSFET SiC, par exemple la tension V_{GS} doit atteindre 20V à l'état passant. Il peut malgré tout

subsister des instabilités de la tension seuil et une dégradation de la grille. La diode intrinsèque SiC présente une chute de tension significativement plus élevée que la diode intrinsèque Si, ce qui induit davantage de pertes à l'état passant en fonctionnement inverse malgré d'excellentes caractéristiques en commutation. A cet égard il est vivement recommandé d'employer une diode Schottky en parallèle.

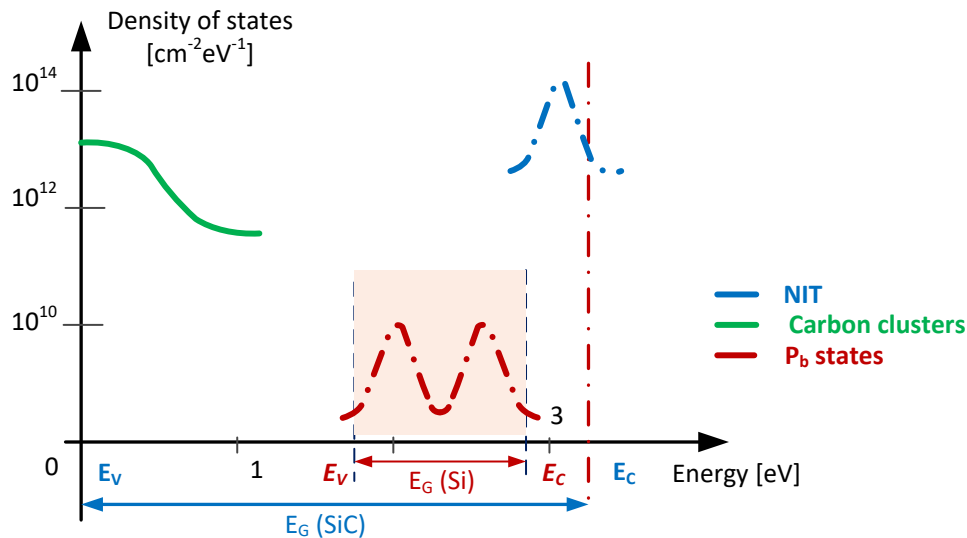


Figure 2. Représentation schématique des niveaux d'énergie en jeu dans l'interface SiC-SiO₂

Le chapitre 3 est l'objet d'investigations en terme de caractéristiques statiques sur un composant 100 A – 1.2 kV, l'accent est mis sur les distinctions à observer entre les MOSFET Si et SiC. La température devient un facteur d'influence majeure dans les essais expérimentaux associés car elle affecte l'ensemble des paramètres et par suite le comportement du composant. Pour s'affranchir de cet inconvénient, il a été fait usage d'une enceinte thermique permettant de mettre à température désirée le composant, cette phase dure 12 heures et assure un parfait équilibre thermique du composant. Les composants MOSFET de puissance mettent en jeu des courants tels que l'auto échauffement n'est pas négligeable, c'est pourquoi des procédures expérimentales spécifiques sont requises et elles ont été décrites en détail. Les essais en question ont été réalisés par pas de 10°C de -30°C à 150°C.

En ce qui concerne la tension seuil V_{TH} , elle a été mesurée par une méthode à courant constant. A l'instar des MOSFET Si, il a été observé que celle des MOSFET SiC diminue avec la température. Cependant la présence d'états d'interface implique une réduction non linéaire de V_{TH} avec la température, cette spécificité doit être prise en compte dans le modèle.

Les caractéristiques courant tension (I_D vs V_{DS}) sont quant à elles obtenues par pulse de largeur 500 μ s de sorte à éviter l'auto échauffement. Ces caractéristiques présentent une forte dépendance avec la tension de grille V_{GS} , ce qui souligne la forte contribution de la résistance de canal (R_{ch}) dans la résistance totale à l'état passant. D'ailleurs le comportement thermo-électrique du MOSFET SiC dépend significativement de la tension V_{GS} , la Figure 3 en est l'illustration. Pour les tensions de grille élevées, par exemple $V_{GS} = 20$ V, le courant décroît avec la température. En revanche, pour des tensions de grille plus faibles, par exemple $V_{GS} = 12$ V, le courant augmente avec la température. Il convient de garder à l'esprit ce comportement particulier vis-à-vis de la stabilité thermique d'un

composants MOSFET d'une part, et de la distribution du courant sur plusieurs MOSFET connectés en parallèle d'autre part.

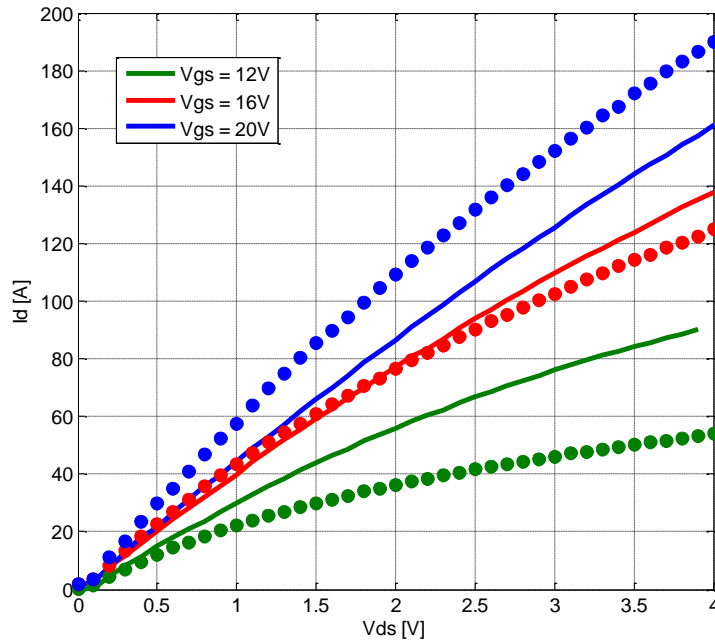


Figure 3. Caractéristique de sortie du MOSFET SiC 100A-1.2kV à 30°C (courbe continue) et à 150°C (courbe discontinue)

La résistance à l'état passant $R_{DS(ON)}$ a également été quantifiée et le rôle joué par la résistance de canal a été examiné. Pour éviter les problèmes d'auto échauffement ces recherches ont été menées par le biais de la spectroscopie d'impédance à 0 A. Les résultats ont permis d'identifier $R_{DS(ON)}$ comme un sérieux candidat en tant que paramètre électronique thermo-sensible (TSEP) en vue d'estimer la température de jonction du transistor. Suite à cette étude, les conditions optimales ont été identifiées, en l'occurrence l'application d'une faible tension de grille V_{GS} pour améliorer la sensibilité de R_{ON} vis-à-vis de la température. De plus amples détails sont fournis dans le chapitre 5.

Le chapitre 4 propose un nouveau modèle compact sur la base des résultats de caractérisation expérimentaux, lequel prend en compte les divers phénomènes physiques impliqués dans le fonctionnement du MOSFET SiC. L'influence des pièges d'interface est traitée en détail. Après avoir commenté les principaux modèles existants dans la littérature, le modèle proposé est développé et les paramètres intervenants sont déterminés par moindres carrés.

$$I_D = k_{(V_{GS}, T)} \times \left[(V_{GS} - V_{TH}) - \frac{\alpha}{2} \times \frac{a_{(V_{GS}, T)} \times V_{DS}}{V_{DS} + b_{(V_{GS}, T)}} \right] \times \frac{a_{(V_{GS}, T)} \times V_{DS}}{V_{DS} + b_{(V_{GS}, T)}} \quad (0-3)$$

Un modèle simplifié est mis en œuvre sur la base de la relation (0-3), lequel intègre l'effet des états d'interface par le biais du paramètre k , ainsi que la faible longueur du canal par le biais du facteur α . Pour une tension de grille V_{GS} donnée, le courant de drain I_D augmente avec V_{DS} , et il tend progressivement vers l'état saturé. Ce comportement se traduit par le contrôle de la tension de canal V_{CH} au travers des paramètres a et b dans l'expression de I_D . Par conséquent les mécanismes de saturation du MOSFET SiC apparaissant dans la région dite JFET sont également pris en compte. La

dépendance thermo-électrique a également été traitée, incluant son effet sur la tension seuil, sur la mobilité dans la couche d'inversion, sur la résistance de drift et sur la résistance de canal.

Le chapitre commence par traité les effets des états d'interface sur la tension seuil. Une loi polynomiale est mise en œuvre pour en rendre compte. Le chapitre se poursuit par la modélisation du gain en courant k sur la base des essais expérimentaux sur R_{ON} à 0A. Celui-ci est représenté par une relation spécifiant son évolution avec deux paramètres, la tension de grille V_{GS} et la température. Enfin les paramètres a et b sont déterminés de sorte à corroborer l'ensemble des caractéristiques I_D vs V_{DS} expérimentales.

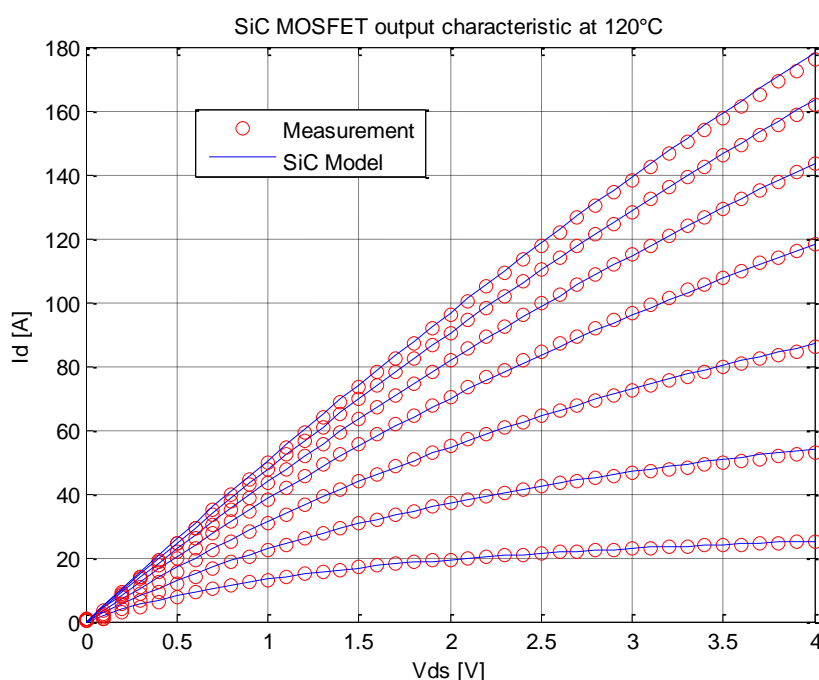


Figure 4. Caractéristiques I_D vs V_{DS} , comparaison du modèle (lignes) et des essais expérimentaux (cercles) à 120°C

Les quatre paramètres (k , α , a and b) nécessaires à ce modèle compact ont été extraits et le modèle se conforme bien au comportement expérimental, la figure 4 l'atteste. La procédure d'extraction des paramètres repose sur la mise en œuvre d'un outil d'optimisation du logiciel Matlab. Le modèle a également été implanté sur le logiciel SABER, lequel modèle prédit correctement le comportement du MOSFET pour divers modes d'opération.

Le chapitre 5 est consacré à la caractérisation et à la modélisation thermique. La mesure de la résistance thermique requière la mise en œuvre d'un TSEP pour estimer la température de jonction. La méthode retenue repose sur la mesure d'un paramètre électrique du transistor qui évolue avec la température, en l'espèce la résistance à l'état passant R_{ON} . La méthode proposée comporte deux étapes, la calibration du TSEP d'une part, et l'enregistrement de la température au cours d'un cycle de dissipation de puissance d'autre part. La phase de calibration consiste à déterminer la relation entre la tension V_{DS} (ou la résistance $R_{DS(ON)}$) et la température de jonction. Nous avons montré qu'il est nécessaire d'appliquer un faible courant de calibration ($I_c = 1$ A ou 100 mA) pour éviter l'auto-échauffement et qu'il convient d'imposer une faible tension de grille ($V_{GS} = 7$ V) pour accroître la sensibilité. Nous avons expliqué comment éviter d'une partie des effets indésirables des états d'interfaces.

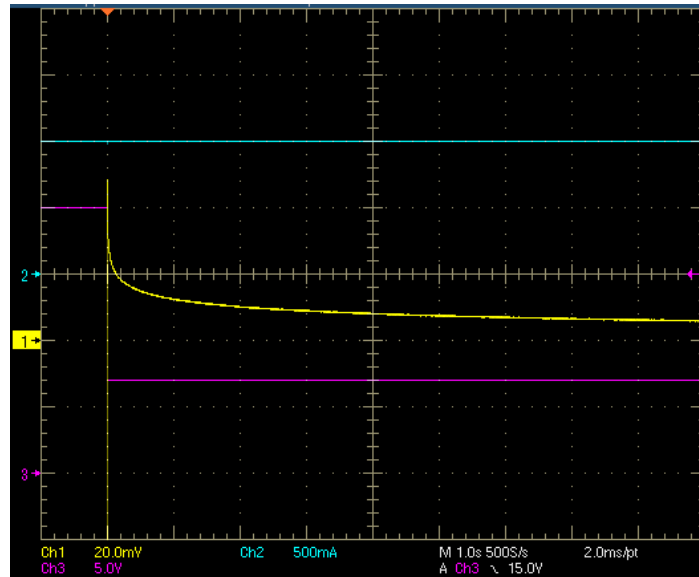


Figure 5. Formes d’ondes obtenues avec $I_c = 1\text{ A}$ à 10°C au cours d’une transition de la tension de 20V à 7V.

Cependant, nous n’avons pas été en mesure de nous en affranchir complètement. La Figure 5 en est l’illustration, on y observe les formes d’ondes obtenues après la commutation de la tension de grille de 20 V à 7 V, le composant sous test étant parcouru par un courant constant. Il apparaît une forte surtension (40 mV) et un long transitoire (100 s) sur la tension V_{DS} qui rend la mesure de température inexploitable. C’est pourquoi nous nous sommes alors tournés vers l’estimation non pas de la résistance thermique propre mais de la résistance thermique mutuelle. Avec bien plus de succès, nous avons développé une méthodologie et validé les résultats expérimentaux par le biais d’une modélisation tridimensionnelle par éléments finis sur le logiciel COMSOL. En outre, le modèle électrique développé dans le chapitre 4 voit sa précision confirmée en recoupant avec les essais thermiques du chapitre 5.

Les conclusions des travaux de recherche menés sont dressées et des propositions d’investigations futures sont également suggérées dans une dernière section.

General Introduction

Background

Owing the same operation principle with its low power counterpart, the power MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) has a modified geometry with a vertical structure where the source and drain electrodes are placed at the front and backside of silicon die. The first generation of power MOSFETs was commercially introduced into the market the early 1980s by International Rectifier. This technology uses the double-diffusion process with a planar gate structure, known as DMOS, offers the blocking voltage capability up to 300 V. In the 1990s, a vertical trench gate MOSFET structure, commercialized as TrenchFET®, was introduced by Vishay Siliconix as the second generation of power MOSFET. TrenchFET exhibits a clear superiority over DMOS in terms of on-resistance and gate charge for specific products lower than 100 V. The super-junction (SJ) CoolMOS®, also known as the third generation of power MOSFETs, was released by Siemens (Infineon now) in 1999s. The power SJ MOSFET breaks the limit line of silicon, employing a novel drain structure which adopts mainly for 600 V products.

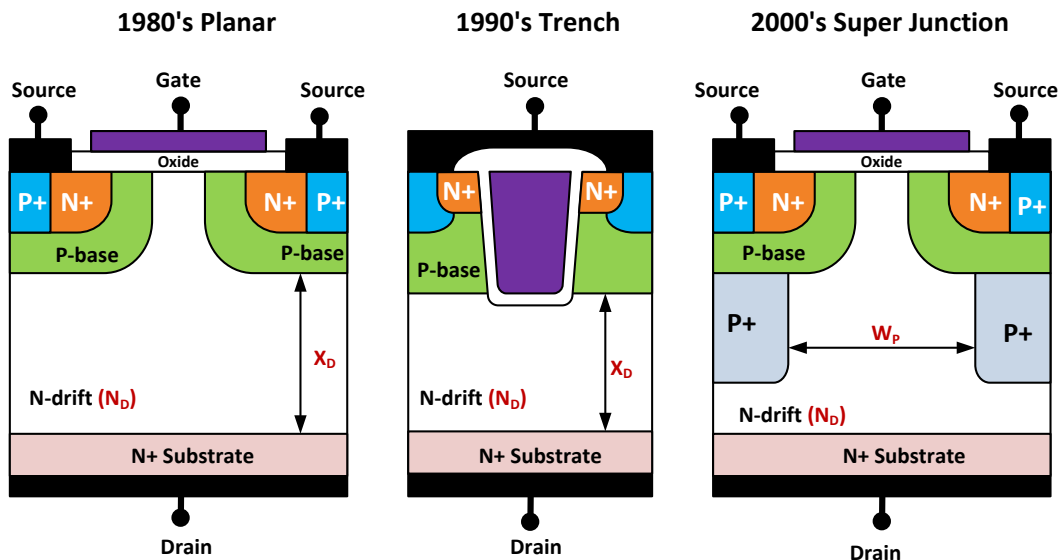


Figure 6. Planar, trench and super-junction MOSFET unit cell comparison

The power MOSFETs have several distinct advantages including high input impedance, fast switching speed and high efficiency (low switching losses, low on-resistance). Thus, they have been widely used in high frequency (300 kHz to 2.0 MHz, or more) power electronics applications such as switch-mode power supplies (SMPS), DC to DC converters, and motor controllers. Although power MOSFET technology has been ceaselessly improved for over 30 years to satisfactorily serve many segments, they have been limited at voltage ranges from 100 V to 600 V. Consequently, IGBTs (Insulated Gate Bipolar Transistors) are primarily used as alternatives to MOSFETs for medium-to-high power applications above 600 V.

As shown in Figure 6, for conventional MOSFET, the voltage blocking capability of device is determined through the combination of thickness (X_D) and doping (N_D) of N-type epitaxial region. The specific on-resistance (on-resistance per unit area) $R_{ON,sp}$ is determined for a given breakdown voltage

V_{BR} , referred to “silicon limit”, as expressed in equation (0-4). $R_{ON,sp}$ increases approximately by the 2.4th power of the V_{BR} , which is a barrier to the inroads of power MOSFET in the high voltage arena. The SJ structure technology allows power MOSFET with substantial increasing of the blocking voltage while maintaining the low on-resistance. The great reduction of on-resistance offers obvious conduction loss benefits compared to conventional structure that creates new limit for vertical MOSFET as equation (0-5).

$$R_{ON,sp} = 8.9 \times 10^{-19} \times V_{BR}^{2.4} \quad (\Omega \cdot \text{cm}^2) \quad (0-4)$$

$$R_{ON,sp(SJ)} = 0.198 \times W_p^{5/4} \times V_{BR} \quad (\Omega \cdot \text{cm}^2) \quad (0-5)$$

The performance improvements have been witnessed with technology innovations from planar gate to trench gate and today's super-junction structure. However, the rate of improvement of the silicon-based power MOSFET has been slowed when they have asymptotically approached its theoretical maturity.

Recently, power MOSFETs with silicon carbide (SiC) technology have gained more attention as the promising devices for next-generation power electronics applications. Combining the excellent properties of SiC material with the potential advantages of MOSFET, SiC MOSFETs have far exceeded the theoretical limit of Si power counterparts to enter the medium applications in particular 1.2 kV - 1.7 kV voltage range. SiC MOSFETs exhibit lower on-resistance, lower switching loss, and higher frequency operation in compared with IGBTs at the similar voltage rating. SiC MOSFETs have the further major advantage of satisfactory operation at high temperatures. As normally-off and voltage-controlled device, designers can greatly leverage the design experience using Si MOSFETs and IGBTs. Thus, SiC MOSFETs are foreseen to replace Si IGBTs for emerging applications.

Outline of this work

Although promising, but being at a relatively immature technology, SiC MOSFETs have their own list of concerns that had slowed down their performance and reliability far from the theoretical potential of material. SiC MOSFETs are designed and essentially processed the same way of their Si counterparts. However, they exhibit quite different characteristics. Thus, understanding of the unique operating characteristics and their effects in design are required to fully utilize the advantages of SiC MOSFETs. The accurate device models are also needed in the circuit simulators to evaluate the potential utilization of SiC MOSFETs in different applications. Consequently, the characterization and modeling of SiC MOSFETs have received a great deal of attention from the aspect of power circuit and system designers.

The PhD dissertation is composed of 5 chapters dealing with the characterization and modeling of SiC MOSFETs. Details regarding the approach taken to achieve these goals and the results of the research are discussed in the following chapters.

Chapter 1 describes the background information about WBG materials and power devices. This chapter is presented starting from unique WBG materials properties to their advantages in power devices. Some key components in power electronic systems (power diodes and switches) are reviewed to emphasize distinctive characteristics of SiC devices.

Chapter 2 is entirely dedicated to SiC power MOSFETs. The chapter presents a detailed analysis of the technological problems of SiC MOSFETs double-implanted MOSFET (DiMOSFET) that have the same operating principle and manufacturing process as their counterpart's Si MOSFETs. It begins with the introduction of physics and device structures of the SiC MOSFET. Afterwards, the static characteristics including on-state and blocking mode are considered. A detail regarding the physics of SiC MOS-based devices with emphasis on gate oxide growth concerns is discussed in this chapter. Finally, a review of the SiC MOSFET technical issues related to interface charge traps is also presented.

Chapter 3 investigates the SiC MOSFET characterization where the difference of the characteristics between SiC and Si power MOSFETs is also discussed and clarified. The measurement setups are presented to characterize the device at different temperatures ranging from -30° to 150°C . The threshold voltage and I-V characteristics are measured to identify the temperature dependence on the device performance. The static on-resistance is quantified, and the role of channel resistance is further investigated by impedance spectroscopy method.

Chapter 4 deals with the development of a new compact model, accounting for various physical phenomena of SiC MOSFET. The influence of interface trap on developing 4H-SiC MOSFET model is discussed in detail. For high voltage SiC MOSFET modeling, the existing works are then reviewed. The proposed model with a single set of equations is investigated that accurately predicts the device operation in variety of operating modes. The model parameters are extracted using fitting techniques by comparison the simulation to experimental results. The implementation of the model into Saber is also described.

Chapter 5 focuses on the thermal characterization of the power SiC MOSFET using thermal sensitive electrical parameter (TSEP). The fundamental theories for the thermal analysis of packaged semiconductor devices are presented. The TSEP for the SiC MOSFET has been identified. Due to the interface traps affects, a modified thermal resistance measurement is developed for the SiC MOSFET thermal characterization. From the measured results, the thermal distribution for the packaged SiC MOSFET using 3D finite element (FEM) method is carried out. The extracted results from the 3D FEM model are used in electrical model to validate the proposed device model with experiments.

The main conclusions of this dissertation and potential future work are presented at last section.

Chapter 1 Fundamentals of wide band gap power devices

1.1. Background

Power electronics is the application of solid-state electronic components to control and convert electrical power from the available input forms into the desired electrical output forms. As illustrated in Figure 1.1, the converters are constructed with semiconductor devices, passive components and control devices into different circuit topologies, to connect and control the power between two systems in the proper, reliable, and efficient manner. The power electronics has recently emerged as a complex and multidisciplinary technology, mainly concerning the field of semiconductor devices, converter configurations, and control techniques.

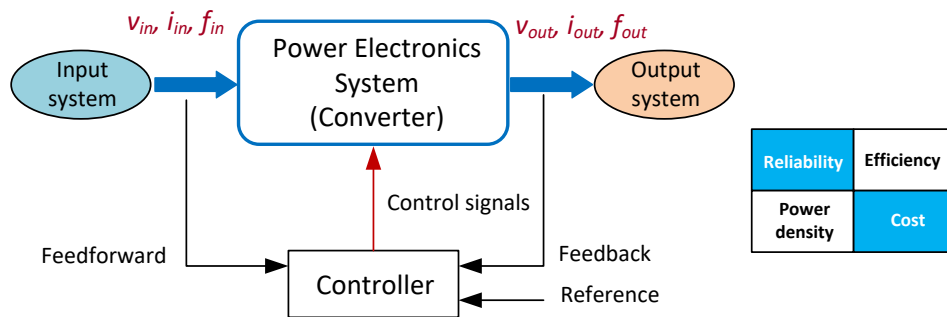


Figure 1.1. Power electronics system structure

With the widespread adoption of converters in many applications, the power electronics has already been anticipated to be a significant impact for efficient using and reducing overall energy consumption. As the intermediate stage, deployment of advanced power electronics in four major applications (buildings and lighting, power supplies, smart electricity grid, and industrial drives) can reduce the current electricity consumption in European Union by 25% [1].

As the heart of any power electronics converter, power semiconductor is the key in determining the efficiency of the conversion system. By far, silicon has been the predominant semiconductor used by most power electronics systems. However, the maturity in material, device and system has nearly reached the highest possible performance. Hence, the Si-based power devices fail to offer the cost and performance ratio to power efficient, especially for emerging applications with the stringent requirements (more compact, lower weight, higher temperature, and higher power density). Accordingly, new materials and devices structures are needed to fill this performance gap.

WBG semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) allow new power semiconductor devices for greater efficiency, smaller size, and lighter weight. Moreover, the new devices can operate at higher voltages, temperatures, and frequencies, which help significantly to reduce volume, decrease cooling requirements and passive components, contributing to overall efficiency of systems [2-4].

1.2. Band gap energy

As illustrated in Figure 1.2, the electrons in the outermost shell of an atom are known as valence electrons which occupy series of energy levels within an energy band, referred as valence band E_V . The band above the E_V is denoted the conduction band E_C where electrons can move freely, enabling the flow of electricity. It should be noted that the bands below the E_V are normally completely filled and play no part in the conduction process. Hence, it is sufficient to consider only valence and conduction bands while discussing the electrical properties.

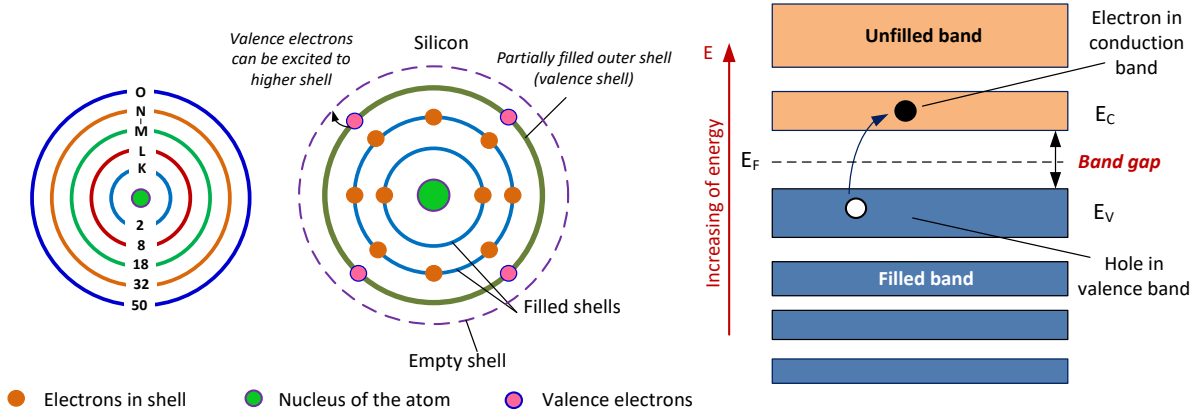


Figure 1.2. Orbital model of some atoms and simplified energy band diagram

The band gap E_G (eV) relates to the amount of energy required to promote an electron from the top of the E_V to the bottom of the E_C to serve as free charge carrier participating in current conduction. The band gap is a major factor to determine the electrical conductivity of substances. The materials with large E_G are referred as insulators, whereas conductors either have very small or none E_G . Most of the conventional semiconductors have band gap in the range 1-1.5 eV, whereas WBG materials are so-called due to a relatively high E_G in the range of 2-4 eV. In the case of diamond (C), though band gap of 5.5 eV is technically considered as insulator, it exhibits actually the ultimate semiconductor.

The band gap decreases slightly with temperature and introduction of impurities. It can be expressed for Si and other semiconductors in the form [5-7]:

$$E_G(T) = E_G(0) - \frac{\alpha \cdot T^2}{T + \beta} \quad (1-1)$$

$$\Delta E_G(N) = -\frac{3q^2}{16\pi\epsilon_s} \cdot \sqrt{\frac{q^2 N}{\epsilon_s K_B T}} \quad (1-2)$$

where $E_G(0)$ is the value of the band gap at 0 K, α and β are constants chosen to obtain the best fit to experimental data. K_B is the Boltzmann constant; T is the absolute temperature. N is the doping concentration, q is the electronic charge, ϵ_s is the dielectric constant of the semiconductor. The band gap narrowing is proportional to the square root of the doping concentration. From this expression, it can be found that the band gap shrinkage could typically be ignored for doping less than 10^{18} cm^{-3} .

1.3. Electric characteristics of wide band gap semiconductors

The popular WBG materials in use today are compound semiconductors SiC and GaN. Among many different crystal structures (often referred as polytypes), 3C-SiC, 4H-SiC, and 6H-SiC are the most common SiC polytypes used for semiconductor applications. The characteristics for the most popular WBG semiconductors are shown in Table 1.1 and are explained in the following sections.

Material	Diamond	GaN	4H-SiC	6H-SiC	3C-SiC	GaAs	Si
Band gap E_G (eV)	5.45	3.39	3.26	3	2.2	1.4	1.1
Electron mobility μ_{e} ($\text{cm}^2/\text{V}\cdot\text{s}$)	2200	1200	850	800	900	8500	1400
Hole mobility μ_{h} ($\text{cm}^2/\text{V}\cdot\text{s}$)	1600	150	115	90	40	400	600
Breakdown electric field strength E_{BR} (MV/cm)	10	3.3	2.5	2.8	1.2	0.4	0.3
Saturation velocity v_{sat} (10^7 cm/s)	2.7	2.7	2.2	1.9	2	2	1
Intrinsic carrier concentration n_i (cm^{-3})	1.6×10^{-27}	1.9×10^{-10}	8.2×10^{-9}	2.3×10^{-6}	6.9×10^{-10}	1.8×10^{-6}	1.5×10^{10}
Thermal conductivity λ (W/cm·K)	20	2	4.9	4.9	4.9	0.5	1.5
Dielectric constant ϵ	5.5	9	9.7	9.7	9.7	12.8	11.8
Bulk growth of substrate	In research	Difficult to obtain	Available	Available	Difficult to obtain	Easily obtain	Easily obtain
Direct/Indirect	I	D	I	I	I	D	I

Table 1.1. Electrical properties of semiconductors at room temperature [3, 4]

1.3.1. Wide band gap energy and low intrinsic carrier concentration

An electron skips into the E_C and simultaneously leaves an empty space (hole) in the E_V . Thus, n_i intrinsic carrier concentration refers to either the electron in E_C or hole concentration in E_V in intrinsic materials. It exponentially decreases with the E_G , and increases with temperature [7]:

$$n_i = A \cdot T^{3/2} \cdot \exp\left(-\frac{E_G}{2 \cdot K_B \cdot T}\right) \quad (1-3)$$

where A is a constant of material. The wider band gap makes an electron more difficult to cross the band gap. Fewer electrons crossing the gap translate to higher operation temperature and smaller leakage current [8]. In practical devices, for an abrupt P^+N junction ($N_A \gg N_D$), the undesired junction reverse-bias leakage current can be expressed as [6, 7]:

$$j_{leakage} = j_s + j_{sc} = q \cdot \left(\frac{n_i^2}{N_D} \cdot \frac{L_p}{\tau_p} + \frac{n_i}{\tau_g} \cdot \sqrt{\frac{2 \cdot \epsilon \cdot (V_{bi} + V_r)}{q \cdot N_D}} \right) \quad (1-4)$$

where j_s is the minority carrier diffusion current density, j_{sc} the reverse current density generated in the depletion region (the space-charge generation). L_p , τ_p is diffusion length and lifetime of hole, respectively. τ_g is the generation lifetime in the depletion region. V_{bi} is built-in voltage of the depletion. V_r is reversed voltage. It can be seen from the equation (1-4), the j_s is proportional to n_i^2 , whereas the j_{sc} increases only linear with n_i . Particularly, the n_i for 4H-SiC is approximately $8.2 \times 10^9 \text{ cm}^{-3}$, which is smaller by the order of 10^{-18} compared to Si. Hence the leakage current is much small with WBG materials.

Depending upon the specific device, the smallest doped region of a semiconductor device is usually between 10^{14} and 10^{17} cm^{-3} , thus, intrinsic carriers are negligible. In operating temperature range,

the conduction is controlled by the extrinsic dopant density. However, the n_i increases exponentially with temperature by the equation (1-3). When n_i reaches a value comparable with N_D in the equation (1-4), the P-N structure begins to be leveled out due to large leakage current. In theory, to keep n_i below N_D , the temperature must remain below about 190 °C for Si, about 800 °C for 4H-SiC [6].

Due to the larger band gap, WBG has a lower intrinsic carrier concentration, which allows the device to operate at higher temperatures without suffering from excessive leakage.

1.3.2. High breakdown electric field

In most power devices, the reverse-bias voltage is supported within a depletion layer formed across a lightly doped P–N junction where avalanche breakdown is dominant.

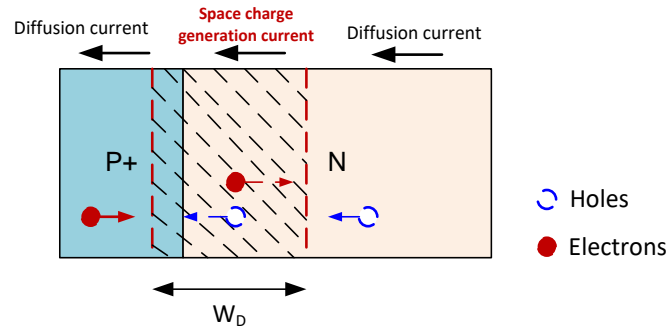


Figure 1.3. Leakage current in a PN junction

As mentioned above, the leakage current is due to the space-charge generation or diffusion. Since the minority carriers enter the depletion layer, they are swept out by the electric field as shown in Figure 1.3. At high reverse voltage, the electric field in the depletion region increases, resulting in acceleration of the carriers to higher velocities. The carriers gain sufficient energies for creating additional electron-hole pairs via collisions with bound electrons, is referred to as the impact ionization. As the new carriers are swept into the depletion region, they too are accelerated. The process for the creation of further pairs of electron and hole repeats itself. Consequently, due to the carriers being transported through the depletion region, the leakage current rapidly increases, leading to an avalanche breakdown [3]. In device design, the onset of avalanche breakdown occurs when the electric field within the depletion approaches the critical electric field, as referred to breakdown electric field strength (E_{BR}) [7, 9].

In a non-punch through PN junction, the low doped region N-drift is thick enough to accommodate the depletion. The electric field profile is then triangular as shown in Figure 1.4. E_{BR} is used to determine the blocking voltage capability according to [17]:

$$V_{BR} = \frac{\epsilon_s \cdot E_{BR}^2}{2 \cdot q \cdot N_D} \quad (1-5)$$

Particularly, the E_{BR} is about 10 times higher for SiC than for Si. Therefore, SiC devices have 100 times greater in V_{BR} than the one of a Si device for the same doping (N_D). For the same blocking voltage, the SiC device can be structured with a 10 times thinner drift thickness (X_D). The specific on-resistance $R_{ON,sp}$ of the drift region is calculated, as [7]:

$$X_D = \frac{2 \cdot V_{BR}}{E_{BR}} \quad (1-6)$$

$$R_{ON,sp} = \frac{4 \cdot V_{BR}^2}{\epsilon_s \cdot \mu_e \cdot E_{BR}^3} = \frac{X_D}{q \cdot \mu_e \cdot N_D} \quad (1-7)$$

$R_{ON,sp}$ varies as the square of the V_{BR} voltage, and is inversely proportional to the cube of E_{BR} . Thus, $R_{ON,sp}$ of 4H-SiC drift theoretically gets 500 times smaller than comparable Si devices.

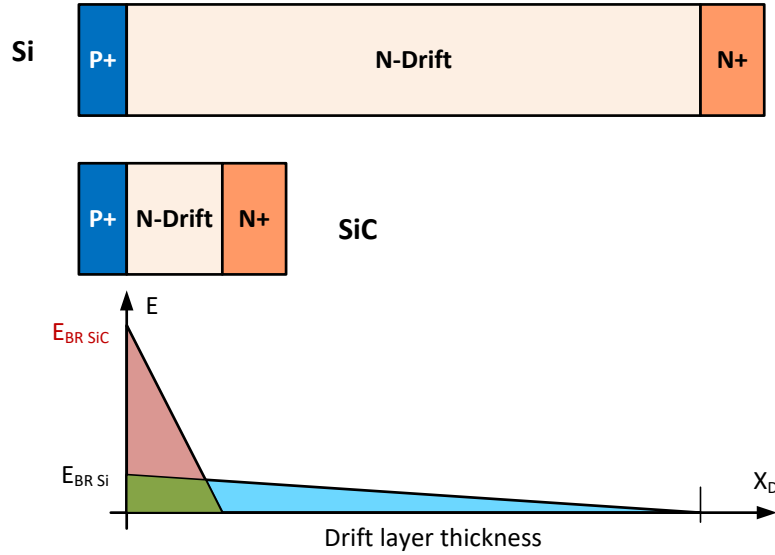


Figure 1.4. Electric field in an abrupt one-sided PN junction

From power device perspectives, the high critical field strength allows WBG devices operate at much higher breakdown voltages than Si-based devices. For a given blocking voltage, SiC devices are structured with a thinner drift layer with more heavily doped than Si, thereby reducing the on-state resistance as illustrated in Figure 1.4.

1.3.3. Other properties

High thermal conductivity

Higher thermal conductivity, the lower the thermal resistance (the thermal resistance will be further investigated in the chapter 5) and easier to bring heat out of the junction to the environment, allows for increased power densities of device. Especially for high voltage devices, a thick drift layer can result in a high thermal resistance.

Indeed, SiC is an excellent thermal conductor with thermal conductivity λ (4H-SiC: $3.3 \text{ W.cm}^{-1}.\text{K}^{-1}$), close to Cu ($3.97 \text{ W.cm}^{-1}.\text{K}^{-1}$). Thus, high thermal conductivity would make SiC a superior semiconductor material in terms of heat transfer for high power applications. This advantage can contribute to decrease the cooling equipments, and therefore to increase power density of system using WBG devices, compared to Si devices [9].

High saturated drift velocity

The saturated velocity v_{sat} is the maximum velocity of the carriers at high electric fields which is a pivotal parameter to determine speed of materials in switching applications [7, 10, 11]. For example,

in a MOSFET channel, carriers are travelling at their saturation drift velocity v_{sat} . The channel transition time can then be calculated as:

$$\tau_t = \frac{L}{v_{sat}} \quad (1-8)$$

L is the channel length. A frequency equal to $1/\tau_t$, higher saturation velocity can achieve higher frequency. Particularly SiC has two times higher saturated drift velocity for electrons, compared to Si. Therefore, SiC is used in high power device (RF and microwave) operating at high frequencies (range of GHz) [12].

Small dielectric constant

Dielectric constant (ϵ_r) or the relative permittivity is a key factor for capacitors and capacitance calculations. In general, a material with a small dielectric constant enables lower values of capacitance. The static dielectric constant of SiC ($\epsilon_r = 9 - 10$) is lower for SiC than for Si ($\epsilon_r = 11.8$), which means that the parasitic capacitance is smaller, leading to faster devices [13].

1.4. Emerging trends in WBG devices

As shown in the Figure 1.5, WBG semiconductor devices are expected to achieve much higher performance than Si counterparts.

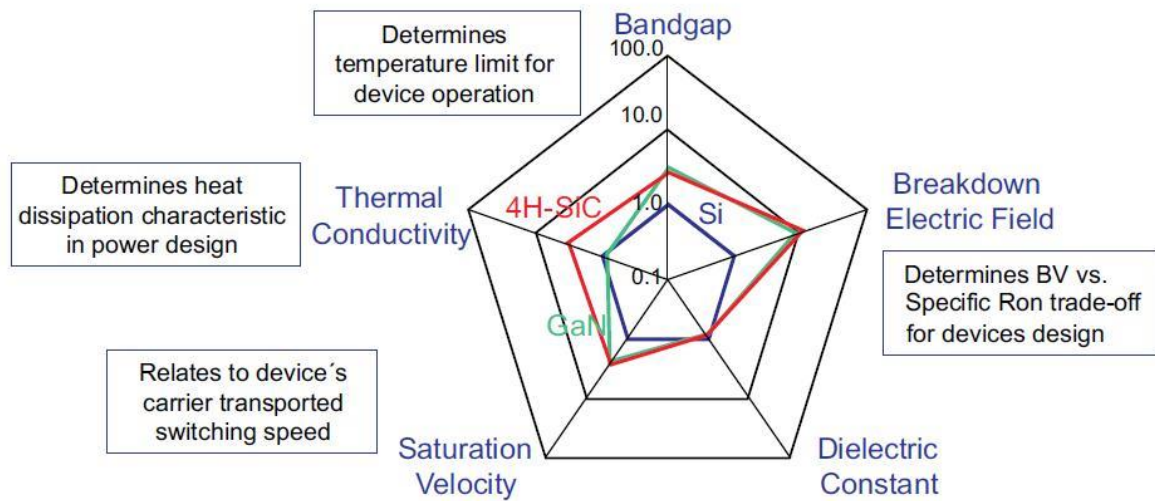


Figure 1.5. Impact of different physical parameters of semiconductor on devices

Today, SiC and GaN products are available, albeit in limited quantities but have distinct benefits for specific applications. Despite similar band gaps and electric breakdown fields, GaN exhibits lower thermal conductivity but higher electron mobility than SiC. Therefore, SiC is regarded as a stronger candidate for high power applications, while GaN is ideal for high-frequency applications [2]. The main obstacles for the power WBG device development are the quality and costs of the wafers, which are extremely expensive and difficult to manufacture, compared with Si wafers.

1.4.1. Wafers

A wafer serves as the substrate upon which epitaxial growth (epitaxy) is carried out to create a device epiwafer. The wafers are made of a nearly pure, defect-free crystalline substantial. As the compound semiconductors, WBG cannot be grown using typical Czochralski process used for Si

growth. Moreover, the relatively high thermal stability of SiC and GaN has brought significant technological difficulties in the growth as bulk crystals. They are carried out at elevated temperatures above 2000 °C. Therefore, more demanding processes, new methods have been developed, which are expensive. Especially, GaN is non-silicon semiconductor, more difficulties arises [14-17].

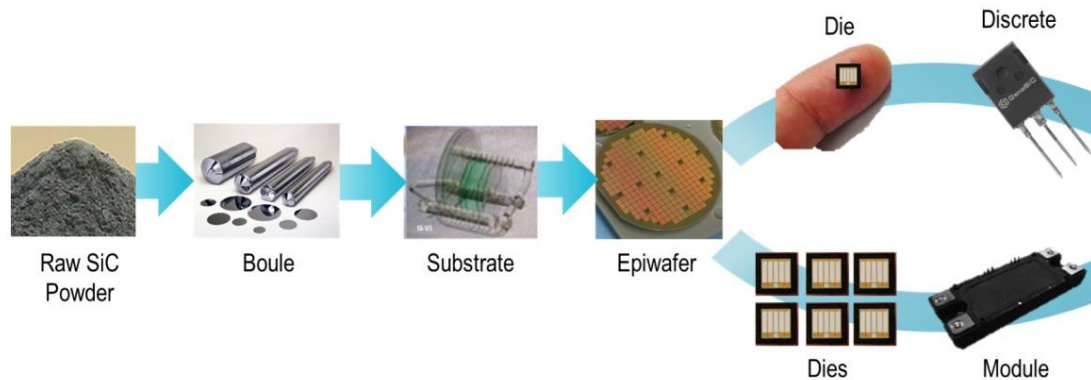


Figure 1.6. SiC manufacturing process

Larger wafers allow improvements in manufacturing efficiency, as more chips can be fabricated on each wafer, lower the costs of devices. Si technologies have used 300-mm (12-inch) wafers for several years. With the recent progress in WBG epitaxial materials, 100-mm (4-inch) 4H-SiC substrates are feasible for manufacturing power devices. While the GaN N-type wafer 50 mm in diameter will be commercially available, with development of 100-mm GaN wafers underway. Thus, the WBG devices are built in on small wafer diameter, making them expensive than Si counterparts.

1.4.2. Structures

With a wafer, the epilayers are deposited on the same material with the substrate, typically called as homoepitaxial layers, or are grown on a foreign substrate, referred as heteroepitaxial layers. Similar to Si technology, SiC devices are now almost homoepitaxial, thereby the avoidance of a mismatch at the boundary between substrate and epilayer. Due to technical complexities, limited availability and the high cost of pure bulk GaN wafer, different foreign substrates are used to develop GaN-based devices. Thus, GaN heteroepitaxial layers are grown on either SiC or Si, instead of GaN.

- GaN-on-Si is actually able to take advantage of Si larger wafer size and there is expected to be more cost effective. The devices are used for power GaN devices.
- GaN-on-SiC has excellent heat dissipation performance and is suitable for high-frequency operation. Today, this technology is widely used for GaN RF device manufacturing and LED manufacturing.

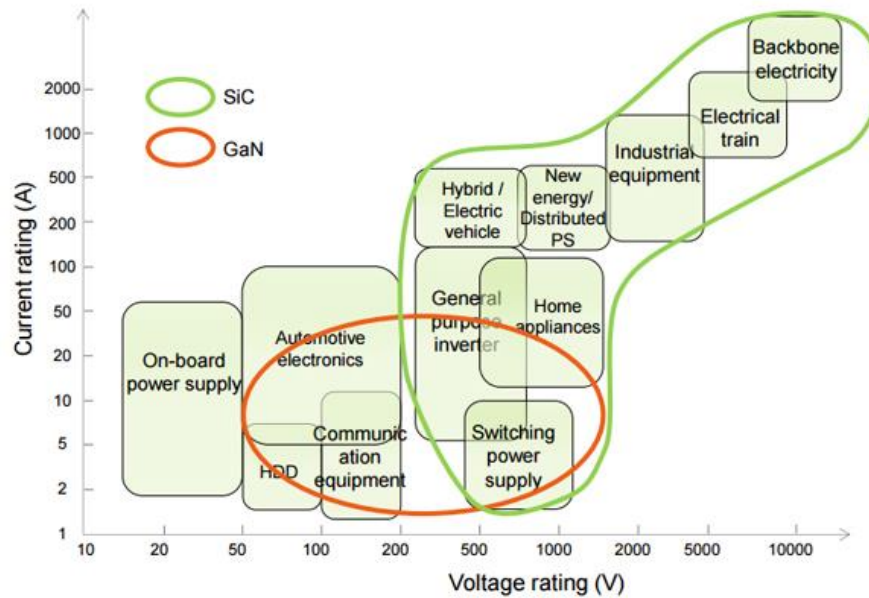


Figure 1.7. Application of SiC and GaN devices by the power

GaN technology faced technical challenges when lattice mismatch and thermal expansion coefficient mismatch between materials are inevitable. In such way, most of the GaN power devices being developed adopt a lateral structure meaning current flows laterally, along the semiconductor's surface. For this reason, GaN devices are suited for medium power applications and enable high-speed switching as shown in Figure 1.7.

Until now, SiC has emerged as the most mature of the WBG semiconductors. From the device manufacturer's perspectives, SiC shows the best trade-off between theoretical characteristics, real commercial availability of the material (wafers and epitaxial layers) and the manufacturing processes maturity. Therefore, SiC is attractive to develop the superior alternative of Si devices to work in harsh environments, especially high temperature or high power [2, 3, 18].

1.4.3. SiC power devices

As shown in Table 1.1, the physical properties of SiC polytypes differ from each other, which affect the substrate growth and the device development. The main material advantage of 3C-SiC (cubic polytype) over the hexagonal polytypes (4H-SiC and 6H-SiC) is higher electron mobility. In addition, due to the narrower band gap of 3C-SiC, a lower density of interface states at the 3C-SiC oxide with respect to 4H-SiC and 6H-SiC have been observed [19]. Thus, 3C-SiC is more advantageous for MOS structure with higher channel mobility. However, 3C-SiC device development is still low due to the lack of reliable 3C-SiC substrates that forces 3C-SiC device to be grown hetero-epitaxially on different substrates (Si, 4H or 6H-SiC).

Despite having similar properties with 6H-SiC, 4H-SiC is preferred for vertical power device due to shallower dopant ionization energies. Moreover, 4H-SiC electron mobility is identical along both the horizontal and vertical planes of the crystal, whereas 6H has anisotropic behavior [9, 20]. Therefore, the majority of researches and developments for SiC power devices have concentrated on 4H-SiC.

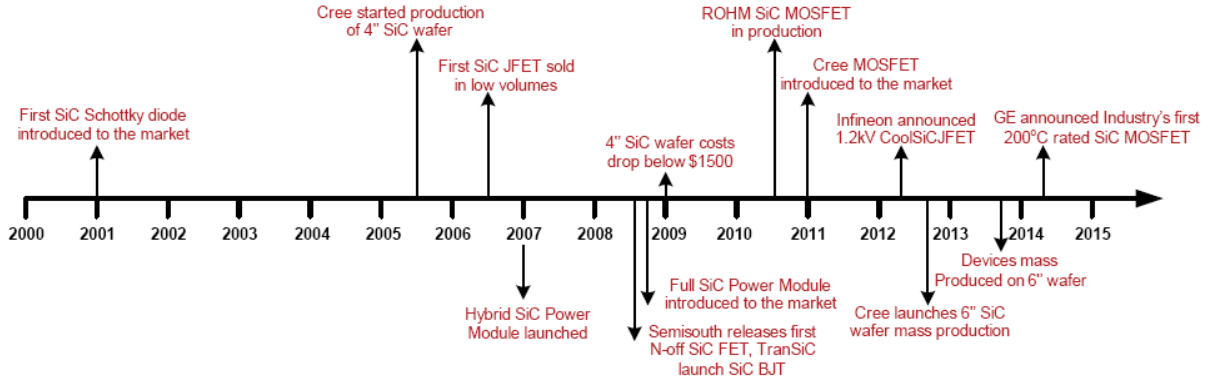


Figure 1.8. The development process of SiC semiconductor devices [21]

SiC devices have been researched and developed since 1980s. Nowadays, a rapid improvement in SiC substrate quality and device fabrication processes has been achieved as illustrated in Figure 1.8. SiC devices began commercially in 2001 with the introduction of SiC Schottky barrier diode (SBD). Then, various kinds of SiC devices such as MOSFETs, JFETs, BJTs, and other SiC diodes have been developed. Now many companies have the ability to supply SiC power devices. Therefore, the performance can be expected to rapidly improve with affordable cost in the near future.

1.5. Technical issues in power SiC devices

In spite of recent progress in SiC epitaxial materials, SiC power devices deal with some technical challenges, which stem from the material characteristics.

1.5.1. Metallization

Generally, the barrier height Φ_B (eV) is an important parameter to determine the electrical behavior of metal-semiconductor contacts. It is defined as the potential difference between the Fermi level of the metal (E_{FM}) and the band edge where the majority carriers reside [10, 22] as:

$$\Phi_{Bn} = \Phi_M - \chi_S \quad (1-9)$$

$$\Phi_{Bp} = (\chi_S + E_G) - \Phi_M \quad (1-10)$$

where Φ_{Bn} and Φ_{Bp} are the barrier heights for N-type and P-type semiconductors, respectively. χ_S (eV) is the electron affinity ($\chi_{SiC} = 3.6$ eV, $\chi_{Si} = 4.05$ eV). Φ_M (eV) is the work function of metal.

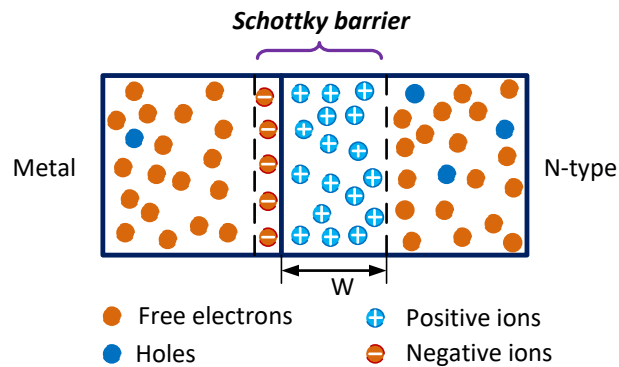


Figure 1.9. Metal-semiconductor junction with Schottky barrier at thermal equilibrium

A junction formed between a metal and N-type semiconductor is considered, as illustrated in Figure 1.9. When materials get into contact, due to $\Phi_M > \Phi_S$, electrons transfer from the semiconductor to the metal. At thermal equilibrium, a depletion region is formed.

In Schottky contact, the Φ_B is high enough to form a depletion region in the semiconductor, near the interface. On the other hand, in ohmic contact, the barrier height is low where depletion region is negligible or absent, offering free carriers flow in or out of the semiconductor. In such case, there is a minimal resistance across the contact.

Metals	Al	Ti	W	Ni	Au	Pt
Φ_M	4.28	4.33	4.55	5.1	5.15	5.65
Φ_{Bn} (4H Si-face)		1.12		1.69	1.81	
Φ_{Bn} (4H C-face)		1.25		1.87	2.07	
Φ_{Bn} (Si)	0.68	0.5	0.67	0.61	0.8	0.9

Table 1.2. Measured barrier heights for metal-semiconductor junctions on N-type [7, 23, 24]

The barrier heights for metal-SiC N-type junction Φ_{Bn} is experimentally given in Table 1.2 that also depends on the surface polarity of SiC (Si-face and C-face). It is clearly seen that most metal and N-type SiC contacts are generally Schottky due to a large Φ_{Bn} .

In addition, it is hardly feasible to form an ohmic contact with SiC, especially to P-type semiconductors, since Φ_M of most metals is less than 6 eV. On the other hand, the depletion width W_D depends on the doping level. Despite the same Φ_B , high doped semiconductor results in smaller thickness W_D . In this condition, the electrons can tunnel through the depletion by the field emission mechanism, formation of a tunnel ohmic contact. For that reason, low resistance ohmic contact can be formed with the heavily doped SiC. However, lattice defects are formed during the ion implantation, which need to be recovered via post-annealing at an extremely high temperature, thereby complicating mass production of SiC devices [22, 25, 26].

1.5.2. Metal-Oxide-Semiconductor in SiC

Among the WBG semiconductors, SiC is considered as a significant advantage material with natural oxide SiO_2 , which enables the fabrication of SiC Metal–Oxide–Semiconductor (MOS) devices. However, SiC MOS devices are limited by the gate dielectric reliability that stems from the large band gap of the SiC.

As shown in Figure 1.10, when three materials are brought into contact, the different work functions of the metal and semiconductor cause distortion in the band shape. The Fermi levels E_F are aligned at the equilibrium of system. At the semiconductor–oxide interface, the barrier height in gate oxide Φ_{BO} is defined as the difference between the electron affinities of the semiconductor and the gate oxide:

$$\Phi_{BO} = \chi_S - \chi_{OX} \quad (1-11)$$

The barrier is an important parameter for controlling the injection of electrons from semiconductor to oxide which determines the reliability of MOS system [27-29].

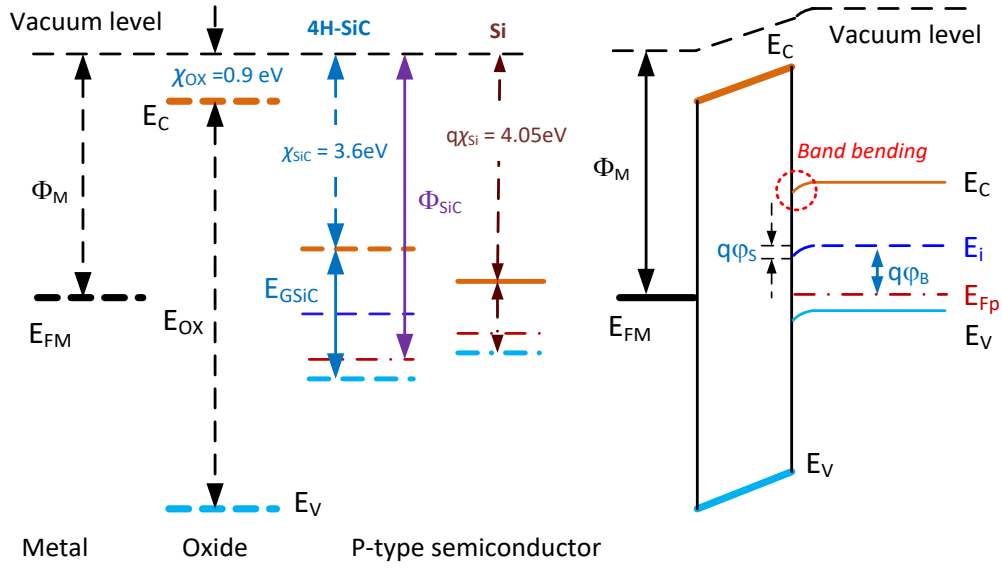


Figure 1.10. Band diagram at the MOS interface after and before contact (after [3, 27, 29, 30])

Since electrons gain sufficient energy, they can overcome the barrier into the gate oxide, producing a Fowler-Nordheim (FN) tunneling. The FN phenomenon is known as contribution to breakdown of gate oxides [31, 32]. It is exponentially dependent on both the electric field in the dielectric and the barrier height [29, 33]:

$$J_{F-N} = A \cdot E_{OX}^2 \cdot \exp\left(-\frac{B}{E_{OX}}\right) \quad (1-12)$$

where J_{FN} is the tunneling emission current density, E_{ox} is the electric field across the oxide. $A \propto (\Phi_{BO})^{-1}$ and $B \propto (\Phi_{BO})^{3/2}$ are adjustable parameters. The Φ_{BO} reduces at higher operating temperatures [20]. As a result, F-N tunneling is proportional to the square of temperature [29].

The Φ_{BO} provides a measure of the oxide quality. With higher band gap, the Φ_{BO} from the 4H-SiC to the oxide is only 2.7 eV in compared to 3.15 eV in a Si MOS system, resulting in higher FN tunneling current through the oxide for the same oxide field. It raises serious concerns about the long-term reliability of SiC MOS devices at high temperatures, high voltages. Particularly, high current density of SiC MOSFET may lead to high temperature in the channel, which increases the FN tunneling effect. Therefore, temperature of oxide must be maintained by its rupture strength conditions for reliable operation.

1.6. SiC power diodes

Power SiC diodes are generally used in conjunction with power transistors in converters or speed motor drives applications. SiC power diodes are with unipolar, bipolar or integrated diode structures, corresponding to three diode types as shown in Figure 1.11. The ohmic contacts of power diodes can be formed on the N-type SiC by nickel (Ni) and on P-type SiC by aluminum/titanium (Al/Ti) after high thermal annealing in the range of 1000 °C [34, 35].

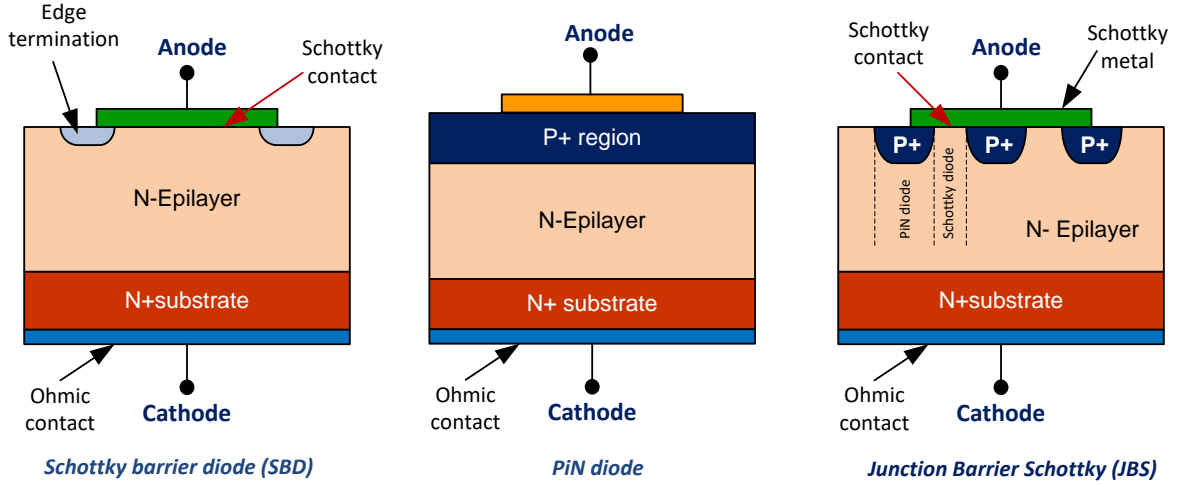


Figure 1.11. Cross sections of power diodes

1.6.1. Schottky Barrier Diode (SBD)

SBD is an attractive device for power electronics applications, due to its relatively low on-state voltage drop and its superior dynamic performance. Regarding the static characteristics, the off-state leakage current J_L and forward voltage V_F of SBD can be expressed as [34]:

$$J_L = -A \cdot T^2 \cdot \exp\left(-\frac{\Phi_B}{kT}\right) \quad (1-13)$$

$$V_F = \frac{n \cdot k \cdot T}{q} \ln\left(\frac{J_F}{A \cdot T^2}\right) + n \cdot \Phi_B + R \cdot J_F \quad (1-14)$$

where A is the Richardson constant (for N-type: $110 \text{ A} \cdot \text{cm}^{-2} \cdot \text{K}^{-2}$ with Si, and $146 \text{ A} \cdot \text{cm}^{-2} \cdot \text{K}^{-2}$ with 4H-SiC), T is the absolute temperature, and k is the Boltzmann constant. The factor n (with $n \approx 1$) is the ideality coefficient, and J_F is the forward current density.

The most remarkable advantage of SiC SBD is high blocking voltage. Expressed by the equations (1-13) and (1-14), due to the higher Φ_B , SiC SBD has a smaller off-state leakage current (J_L) but a larger forward voltage V_F than its Si counterpart for the same blocking voltage rating. However, SiC SBDs are structured with much thinner drift layer, thereby a lower R . The leakage current of SBD is independent of the magnitude of the applied reverse bias voltage (V_R), based upon the equation (1-13). However, in actual power SBD, the J_L increases with reverse bias voltage that can be explained by Schottky electric-field-induced barrier lowering (SBL) phenomenon. For this reason, 1700 V is the limit for SiC SBD.

The commercial SiC SBD products with a breakdown voltage of 600 - 1700 V are now available with V_F in a range of 1 - 2 V. In addition, SiC SBD V_F has a positive thermal coefficient, making SiC SBD well suited for parallel implementation without the risk of thermal runaway. It allows parallel connection of the SiC SBD to handle higher current [36, 37].

While a diode changes from the forward conducting state to the reverse blocking state, the reverse recovery characteristics are illustrated in Figure 1.12. Being majority carrier devices (unipolar), SiC SBDs have no minority carriers stored in the drift layer. As a result, the reverse recovery charge (Q_{RR})

for a SiC SBD is extremely low (< 100 nC), achieving considerably less loss than Si counterpart. Without stored charge, however, there is a small amount of reverse recovery current for discharging the junction capacitance. The reverse recovery time (t_{rr}) of SiC SBD is measured in range of nanoseconds. Moreover, the reverse recovery characteristics observed in SiC SBDs are nearly independent of temperature, forward current (I_F) level as well as turn-off di/dt . These characteristics enable SiC SBD operation high-speed recovery possible under high temperature without increased switching losses [38].

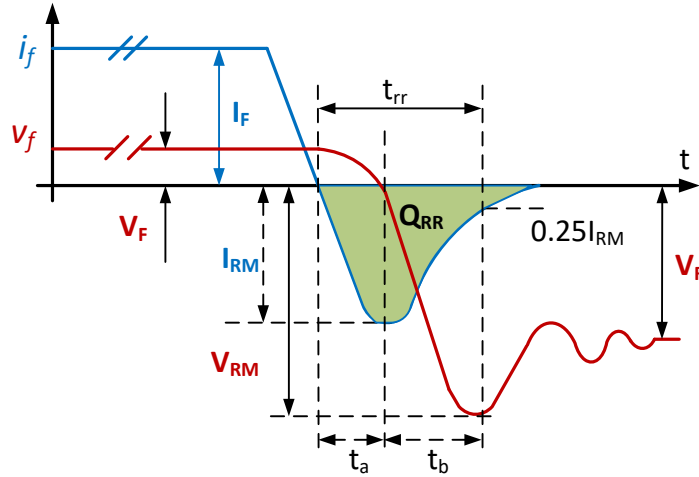


Figure 1.12. Reverse recovery waveform of a diode

Based on an analysis, the features of SiC SBDs are excellent switching operation and high blocking voltages that are well suited for high frequency applications for reducing of the switching losses. It is even foreseen that SiC SBD may replace Si bipolar diodes in medium power modules. The higher thermal conductivity allows the SiC SBD to operate at higher current density with smaller size cooling systems. However, a tradeoff can be involved when the reverse leakage current increases, especially at high temperatures, due to its lower Φ_B with temperature.

1.6.2. SiC PiN

As a bipolar device, PiN diode offers high breakdown voltage and low resistance, simultaneously, thanks to high level injection of minority carriers into the drift region. For the same breakdown voltage, SiC PiN diodes can be achieved with thinner and more doped drift regions, thereby a smaller amount of stored charge that allows far higher switching speed than Si PiN. However, with higher band gap, 0.8 – 1.0 V and 3.2 – 4.0 V are typical V_F for Si PiN diode and 4H-SiC one, respectively. Hence, high conduction loss is a drawback for SiC PiN diodes, at least in the medium voltage ranges. Furthermore, due to the higher Schottky barrier, ohmic contact formation on P-type side (anode) is even more difficult than N-type materials, as mentioned in section 1.5.1.

However, large reverse recovery current during the turn-off leads to high switching losses. Unlike SBD, the minority carrier charge storage increases with the temperature and the forward current. Therefore, as shown in Figure 1.13, reverse recovery time (t_{rr}) and reverse recovery current (I_{RM}) are both larger relative to the values at room temperature, causing significant change in losses [39].

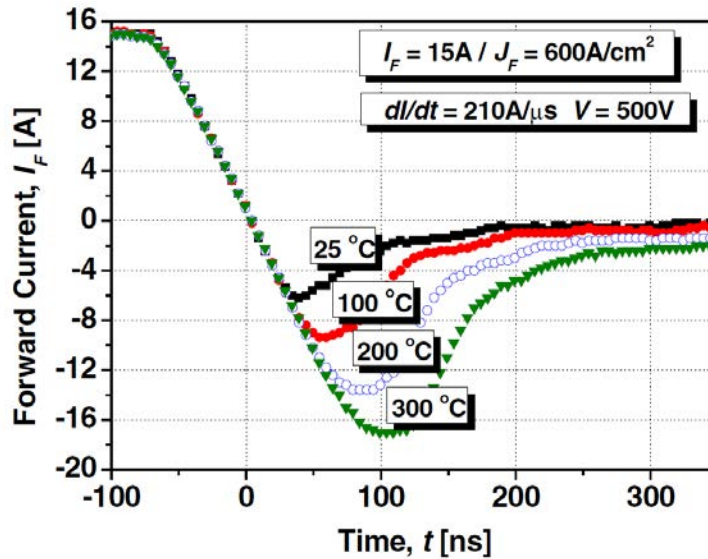


Figure 1.13. Turn-off switching waveform of the SiC PiN [39]

Indeed, SiC PiN diodes are gaining more and more attention in high-voltage applications (power distribution systems, rapid transit railways...) exceeding 3 kV, due to high breakdown voltage, small size and weight, and improved switching speed.

1.6.3. SiC JBS

High reverse leakage current due to electric-field-induced barrier lowering of SiC SBD can be overcome using Junction Barrier Schottky (JBS) or Merged PiN Schottky (MPS) diodes. As illustrated in Figure 1.11, JBS/MPS diodes are integrated diode structures where regions of P-N and Schottky barrier (SB) junctions are alternated. These diodes combine the advantages of both Schottky diodes (low on-state voltage drop, fast switching speed) and PiN diodes (low leakage current at off-state).

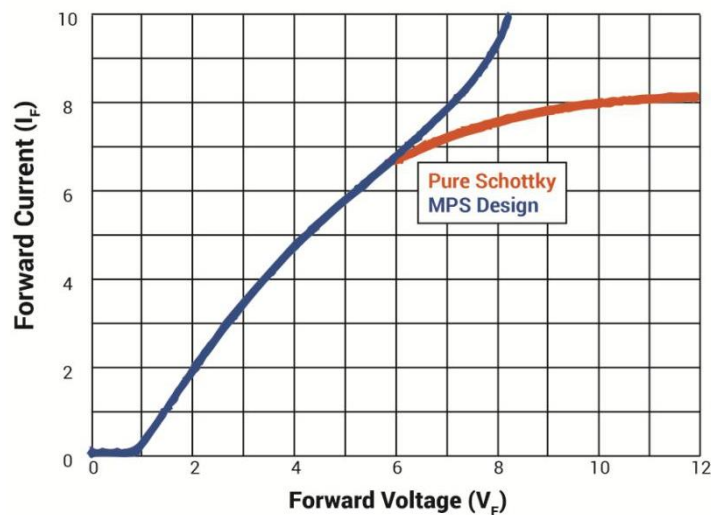


Figure 1.14. Forward bias characteristics of a SiC MPS diode and a SBD (Data from Wolfspeed)

The typical forward characteristic of JBS concept is illustrated in Figure 1.14. When operating at the voltages lower than the turn-on voltage of the P-N junction, these junctions remain inactive. Accordingly, P-N layers do not contribute to the forward current. Without minority carrier injection in the drift region, the JBS diode behaves as an SBD, thereby a fast switching speed. At high forward

voltage drops, JBS structure benefits from the injection minority carriers by the P-N junctions inserted within the main SB contact. Thus, modulation of resistivity induces a lower V_F .

Moreover, the PN grid placed around the Schottky contact creates a potential barrier that shields the SB junction against high electric field in the reverse blocking mode. Hence, lower leakage currents and higher the breakdown voltages than standard SBDs are reported. However, with the presence of P-type doping in a partial region of the SB, extra ion implantation and high-temperature annealing processes are required, making it difficult to fabricate a JBS. The SiC is well suited for JBS structures development with very high breakdown voltages. Typical SiC 1.2 kV JBS diodes have on-state voltage drop of less than 1.5 V due to the low specific resistance of the drift region [36].

1.7. SiC unipolar transistors

1.7.1. SiC JFET

After the success of the SiC SBD, the vertical trench SiC junction field-effect transistor (JFET) was developed and eventually commercialized by SemiSouth in 2008.

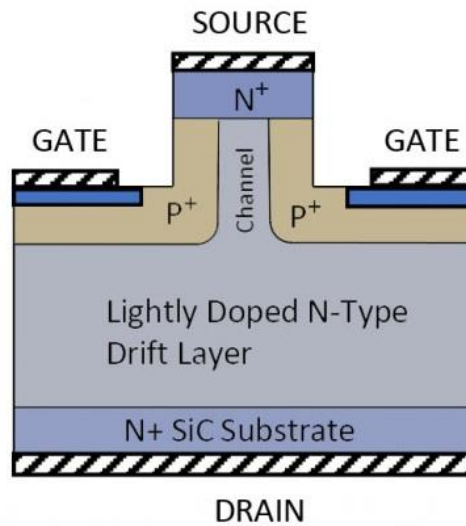


Figure 1.15. Cross-sectional view of SiC vertical JFET

The general structure of vertical JFET is shown in Figure 1.15. Normally-off or normally-on mode of JFET can be determined by choosing a vertical channel width. At zero gate bias, the channel width is designed to be completely depleted for a normally-off device; on the other hand, the channel width is chosen to be opened to conduct high drain current for normally-on device.

Absence of gate oxide and use only P-N junctions in the active area, SiC JFET structures avoid the oxide reliability issues. Thus, JFETs can fully exploit the high temperature capability of SiC. Moreover, the pinch-off voltage V_p of N-channel (equal to the MOSFET threshold voltage) is practically independent of temperature that is determined by the channel doping and its geometry as:

$$V_p = \frac{q \cdot N_D \cdot a^2}{2 \cdot \epsilon_s} - V_{bi} \quad (1-15)$$

where q is the electron charge, N_D is the channel doping, a is the half of the channel height and ϵ_s is the SiC permittivity. Due to the relatively small built-in voltage V_{bi} , the dependent temperature of V_p can be neglected which is the additional advantage of SiC JFET.

The SiC normally-on JFET takes the advantage of low $R_{DS(ON)}$ at zero gate bias ($V_{GS} = 0$ V) and ability to handle high temperatures of SiC which is ideal for solid-state circuit breakers and circuit protection. From application point of view, normally-off JFET structure is preferred. Recently, SiC normally-off JFETs have been developed, enabling their adoption into high voltage switching. However, in a normally-off JFET, the pinch-off in channel at zero gate bias and a reasonable on-resistance are expected at the same time. Thus, it requires a precise control of the channel width which makes the process more challenging. For this reason, the production of SiC JFETs has taken focus on the normally-on SiC JFETs which are primarily commercialized by UnitedSiC at voltage rating 1200 V and 650 V in the market.

1.7.1. SiC MOSFET

Three years after the release of the SiC JFET, CREE Inc. (now Wolfspeed) commercialized the first SiC MOSFET. With the availability of SiC wafers from 1990's, SiC power MOSFET development has progressed rapidly. Today, the SiC MOSFETs are available rated 900 V, 1.2 kV, and 1.7 kV in discrete package or power modules from the many other manufacturers including General Electric, ROHM Semiconductor, Mitsubishi Electric, Infineon, etc. Up till now, SiC MOSFETs are by far the most prominent switching device among the WBG power device family.

SiC MOSFET can operate at the comparable voltage to those of IGBTs with thinner drift layers, leading to lower on-state resistance. Furthermore, SiC MOSFET can withstand higher temperature with lower leakage current. Although the intrinsic allowed temperature for 4H-SiC is around 500°C, interconnect and packaging set the SiC MOSFET temperature limit in practice at 150 °C. As far as the switching behavior is concerned, compact chip size of SiC MOSFET ensures lower capacitance and smaller gate charge over standard Si devices. With the advantage of majority carrier device, the SiC MOSFET can operate at higher switching speed and lower switching losses compared to Si-based IGBTs. Therefore, they make power conversion systems more efficient, more compact, lighter and thermally cooler.

Despite the benefits of material, the performance of SiC MOSFETs is far from the theoretical potential. When the carriers flow at the semiconductor surface underneath the gate, the quality of oxide interface is crucial for MOS device technology. However, the SiC-SiO₂ system is still not satisfactory which presently limits the device capability. The interface contains high density of interface states, which results in low electron mobility at the channel [3, 40]. As well discussed in 1.5.2, an intrinsic disadvantage of SiC in the reliability is the smaller barrier height in gate oxide compared to Si-oxide. This leads to premature oxide breakdown of SiC MOSFETs at high temperatures and high electric field. These problems will be further discussed in chapter 2.

1.8. SiC bipolar transistors

Because of minority carrier injection during operation, bipolar devices such as BJT and IGBT take the advantage of conductivity modulation that reduces on-resistance and forward voltage drop. However, the minority carrier charge stored in drift region has to be removed by recombination

during turn-off, which leads to a low speed and high switching losses [41]. SiC bipolar power devices are also becoming available.

SiC has given the BJT new life. Fairchild launched the first SiC BJTs in 2012. Compared to their Si counterparts, the SiC BJTs improve the current gain and switching speed. They exhibit more efficiency due to the reduction of switching losses and on-state voltage. Now, GeneSiC has released its 1200 V and 1700 V SiC super junction transistors (SJT) which are described as the normally-off, quasi-majority carrier devices. As gate-oxide free device, the manufacturing process of these SiC devices is even simpler than that of a JFET. However, being current controlled devices, the driving circuit for SiC BJT/SJT is more complex than a voltage-controlled device one (like MOSFET).

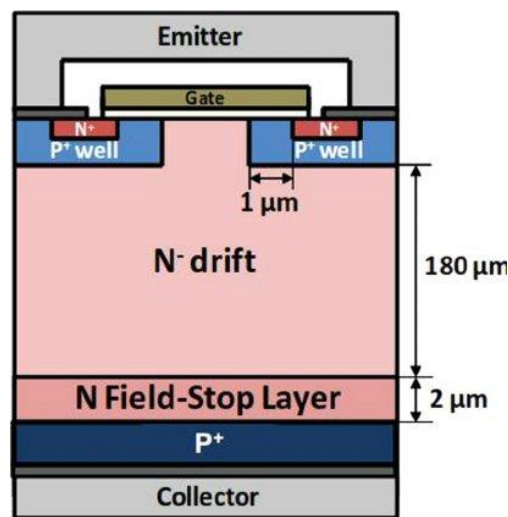


Figure 1.16. Cross section of 22kV 4H-SiC N-IGBT [42]

In the area of SiC IGBT, with the structure as shown in Figure 1.16, ultra-high voltage 4H-SiC IGBT has been reported in [42, 43]. SiC IGBTs show superior behavior including high blocking voltage, high temperature operation and improved switching capability that outperform Si counterpart in power conversion at power grid voltage levels.

However, SiC bipolar device technology faces the problem of basal plane dislocations (BPDs) which cause the device degradation. The Shockley stacking fault (SSF) expansion occurs when the electron-hole recombination takes place at a BPD. During forward bias operation, the expansion of an SSF inside the active region causes the increase of on-resistance, called “forward voltage drift”. Breakdown voltage degradation with SSF expansion due to leakage current has also been observed in reverse bias [44, 45]. Since the SiC bipolar devices outmatch unipolar ones at high blocking voltages in excess of 3 kV, therefore, 1.2 kV SiC BJTs are no longer available. Up till now, SiC IGBT has not commercialized in the market.

1.9. Conclusions

The chapter highlights the benefits of WBG power devices compared to the Si counterparts. The large band gap, thereby a low intrinsic carrier concentration, permits WBG devices to operate at high operation temperatures without suffering from excessive leakage. Due to much higher breakdown electric field, WBG devices offer higher voltage blocking capability. For a given blocking voltage, WBG devices are structured with thinner and more heavily doped drift layers than those of Si, resulting in

lower on-state resistance. In terms of heat transfer (to the environment) of device, the higher thermal conductivity makes WBG superior to Si, allowing larger current carrying capability and higher power densities. Furthermore, WBG devices are more suitable for high frequency applications because of higher saturation drift velocity. Therefore, WBG-based converters are expected to be improved the efficiency, size, and weight.

With the refinements for 10 years in material quality, substrate size, epitaxial deposition, device fabrication and packaging, most of the WBG market is now focused on SiC. For the same breakdown voltage, the on-resistance of a unipolar SiC device can be made comparable to that of a Si bipolar counterpart. Furthermore, the inherent difficulties including the Shockley stacking fault (SSF) and the formation of ohmic contact on SiC P-type prevent the development of SiC power bipolar devices. For high-speed switching applications, the unipolar SiC devices take the advantage of the absence of reverse recovery charge in drift layer, thereby the superior dynamic performance by dramatically reducing the losses. Consequently, in the market of medium voltage rating of 600 V-1.7 kV, SiC unipolar power devices (namely Schottky diodes, MOSFETs) are the forerunner as the most successful WBG devices.

Despite SiC devices' efficiency and capacity, technical problems still limit their use in many high reliable applications. As the most prominent WBG devices, SiC MOSFETs have been commercially available from many manufacturers for several years. However, the SiC-SiO₂ interface quality with respects to reliability and channel mobility has been proved to be a challenge for their widespread use. In the long run, having superior oxide quality is crucial for the development of SiC MOS-based device such as MOSFETs and IGBTs. Furthermore, the conduction of intrinsic body diode can also initiate the Shockley stacking faults which result in the device degradation of high voltage SiC MOSFET. SiC SBDs have been commercialized to apply in high voltage area. Even with the advantages of acceptable on-state losses and high-speed switching characteristics, SiC SBDs exhibit the degrading due to the presence of material defects, thereby lower Schottky barrier heights. As a result, the leakage current of currently available SiC SBD increases rapidly with temperature, which leads to the temperature limitation below 125 °C.

Chapter 2 High voltage 4H-SiC power MOSFET technical discussion

2.1. Structure of SiC MOSFET

2.1.1. Overview

Since the first introduction in 1978 by International Rectifier, many generations of power MOSFET have been explored and developed by manufacturers. Within the vertical structure, the carriers flow from the source (S) at the top to the drain (D) at the bottom. In a planar gate MOSFET (DMOS), the gate electrode (G) is located on the flat upper surface of the channel. In contrast, the gate electrode is deposited inside a trench etched in the silicon which forms a vertical channel in TrenchFET [6, 46-48]. The difference between planar gate and trench gate MOSFET is illustrated in Figure 2.1.

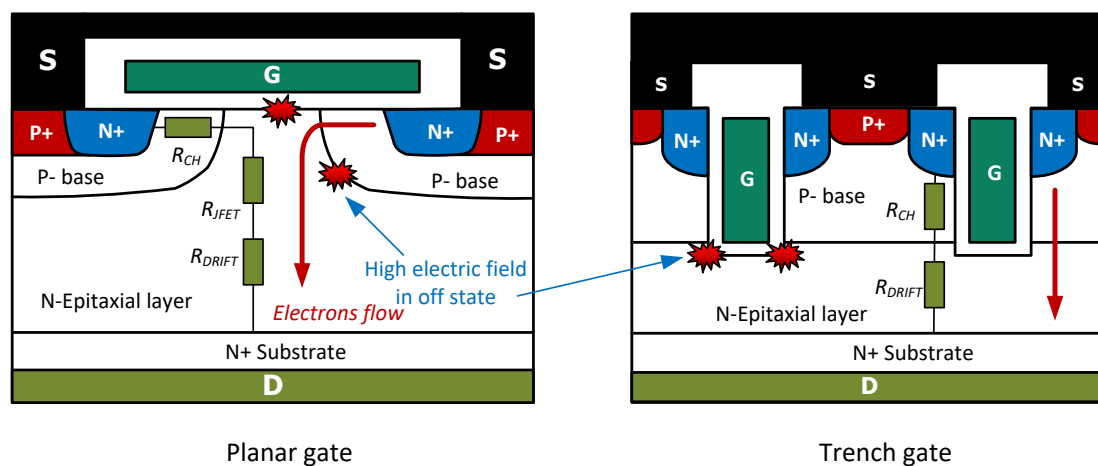


Figure 2.1. Planar versus trench gate MOSFET unit cell comparison (after [8, 20, 49])

In the planar gate MOSFET structure, there is a trade-off between on-resistance and breakdown voltage. The parasitic JFET appearing between the P-body implants restricts current in on-state, results in high on-resistance (the resistance associated to the JFET structure will be investigated in the upcoming section 2.4.3). However, the presence of the P-N junctions below the gate region can screen it from the high drain voltage [50, 51]. Thus, the planar gate structure is beneficial for high voltage rating power MOSFETs.

Trench gate structure offers more efficient wafer use (higher cell density) and lower on-resistance by removing the JFET resistance compared to a planar structure. However, the trench MOSFET faces to the oxide breakdown issues at the sharp trench corners, which leads to long-term operation faults in high voltage applications. In addition, the cell density improvements increase the overlap region of gate-to-drain and gate-to-source, resulting in higher capacitance. The reverse transfer capacitance for the power trench MOSFET structure is greater than for the planar MOSFET structure, leading to higher switching delays [7, 20, 48, 52].

After three generations of the planar gate structure (SiC DMOSFET) by Wolfspeed, trench gate SiC MOSFETs have been available by ROHM with double trench structure. The new structure reduces

electric field concentration in the trench gate portion, and then guarantees long-term device reliability. Reduction of on-resistance and input capacitance translates to lower switching loss and faster switching operation, then improving efficiency of device. However, design solutions for improvement gate performance may result in dramatically complicated transistor structure. Thus, the classical DMOS structure with the planar gate, once again attracted manufacturer's attention. Comprehensive study of this structure is focused exclusively in the rest of this chapter.

2.1.2. Structure of planar gate SiC MOSFET

SiC MOSFETs are designed and essentially processed the same way as silicon MOSFETs. However, due to the extremely low diffusion coefficients of impurities in the material even at elevated temperature (1600°C), the diffusion in SiC is negligibly slow. Thus, SiC MOSFET doping profiles in the P-base and N+ source regions are produced by ion implantation. Since the term DMOS is used to refer to a “double-implanted” MOSFET, resulted in a new name for a SiC MOSFET this context – DiMOSFET [8, 53, 54].

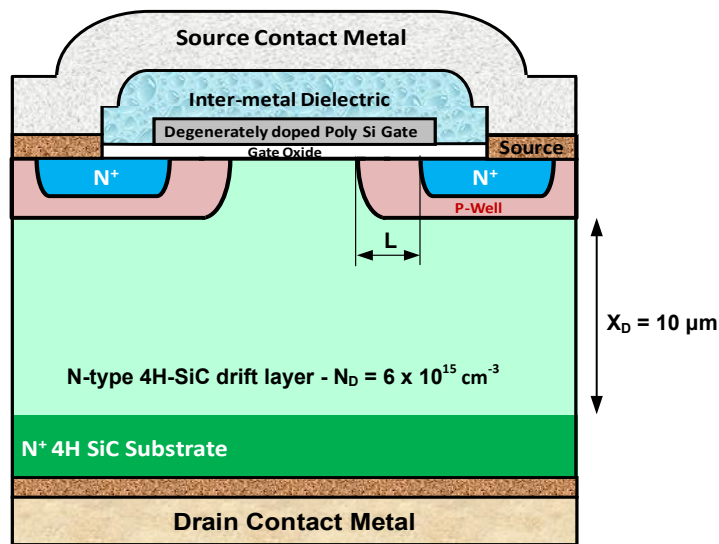


Figure 2.2. Cellular design of the 1.2 kV 4H-SiC DMOSFET [55]

Specific information about the cellular design of the 1.2 kV 4H-SiC DMOSFET can be found elsewhere [55-58]. As represented in Figure 2.2, the N-type 4H-SiC epitaxial layer is grown on an N+ SiC substrate with the thickness about 180 μm at the 1.2 kV-rated [59]. Since this N-epitaxial layer serves as the drift layer of the power MOSFET, the doping (N_D) and the thickness of this layer (X_D) is selected to achieve the desired blocking voltage rating as given in Table 2.1.

V_{BRDSS} [kV]	X_D [μm]	N_D [cm ⁻³]	$R_{ON,sp}$ [mΩ-cm ²]	Avalanche [kV]
0.9	10	1.1×10^{16}	2.4	1.1
1.2	10	8×10^{15}	3.7	1.6
1.7	10	6×10^{15}	5.5	1.9
3.3	30	3×10^{15}	14.2	4.1

Table 2.1. Blocking voltage and N-drift structure (after [60-62])

The MOS channel length (L), defined by the P-well and N+ source regions, is approximately 0.4-1 μm . A self-aligned implantation technique was used to achieve a desired channel length. A heavily doped N+ polycrystalline silicon (called degenerately doped Poly Si Gate) is used as a gate electrode. The ohmic contact in drain electrode is made of Ni. The source and P-well contact were made of Ti/Al. After the source and gate electrodes are formed, the Al electrode layer is deposited and isolated electrically from each other. The gate is then covered with inter-metallic dielectric.

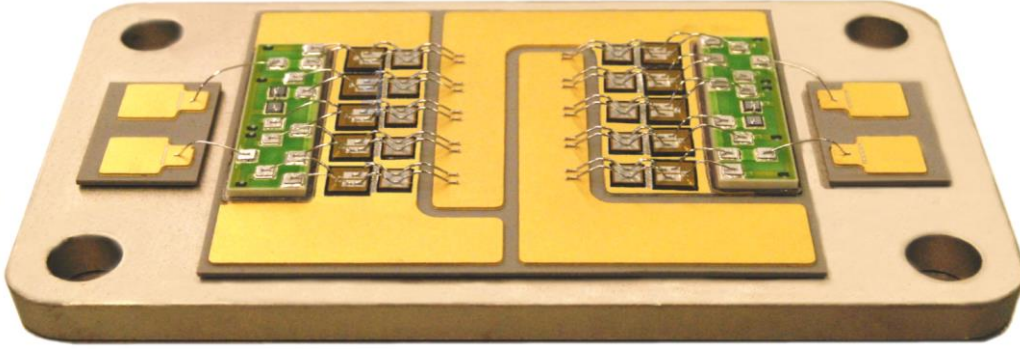


Figure 2.3. Internal layout of SiC MOSFET CAS100H12AM1 module (picture from the CREE flyer)

A 4H-SiC MOSFET at rated of 1.2 kV is structured with an N- drift layer thickness of 10 μm , doped at $6 \times 10^{15} \text{ cm}^{-3}$ and the channel length of 0.5 μm . The chip is with a 4.09 mm x 4.09 mm die size and an active conducting area of 0.101 cm^2 with more 50,000 cells [58, 63]. Our study is made on the CREE module CAS100H12AM1 within a single half-bridge package. As shown in Figure 2.3, each switch is designed with 5 parallel-connected SiC DMOSFET chips and 5 SiC Schottky diodes with voltage ratings of 1200 V.

2.2. The modes of operation

The physics of operation for the enhancement N-type power MOSFETs are analyzed in detail in the textbooks [47, 48]. The same concepts are applicable to the SiC MOSFET structure.

2.2.1. The threshold voltage and the formation of channel

At zero gate-voltage condition, the band bending occurs at MOS interface due to gate-semiconductor work function difference Φ_{GS} as shown in Figure 1.10.

$$\Phi_{GS} = \Phi_G - \Phi_S \quad (2-1)$$

The amount of band bending at the surface is represented by the surface potential ϕ_s , which is measured from the bulk intrinsic level E_i . Note that ϕ_s is positive when bands bend downward. The Φ_S depends on the position of E_{Fp} can be calculated by on the impurity and its doping [3, 30]:

$$\Phi_s = \chi_s + (E_C - E_F) = \chi_s + \frac{E_G}{2} \pm q\phi_B \quad (2-2)$$

The equation (2-2) takes a plus for P-type. The Fermi potential ϕ_B for the P-substrate is given versus the doping concentration N_A and the semiconductor intrinsic carrier concentration n_i by:

$$\phi_B = \frac{k \cdot T}{q} \cdot \operatorname{argsh} \left(\frac{N_A}{2 \cdot n_i} \right) \approx \frac{k \cdot T}{q} \cdot \ln \left(\frac{N_A}{n_i} \right) \quad (2-3)$$

With a positive gate voltage, the E_{FM} moves down in the band diagram by qV_{GS} as shown in Figure 2.4. A positive charge Q_G is introduced to the gate. Holes of the P-substrate underneath the gate are then repelled away from the substrate surface. Simultaneously, a negative charge layer (electrons and ionized acceptors) is formed at the oxide-semiconductor interface, with the same amount of a positive charge induced in the gate electrode. Thus, the surface layer in P-region is depleted.

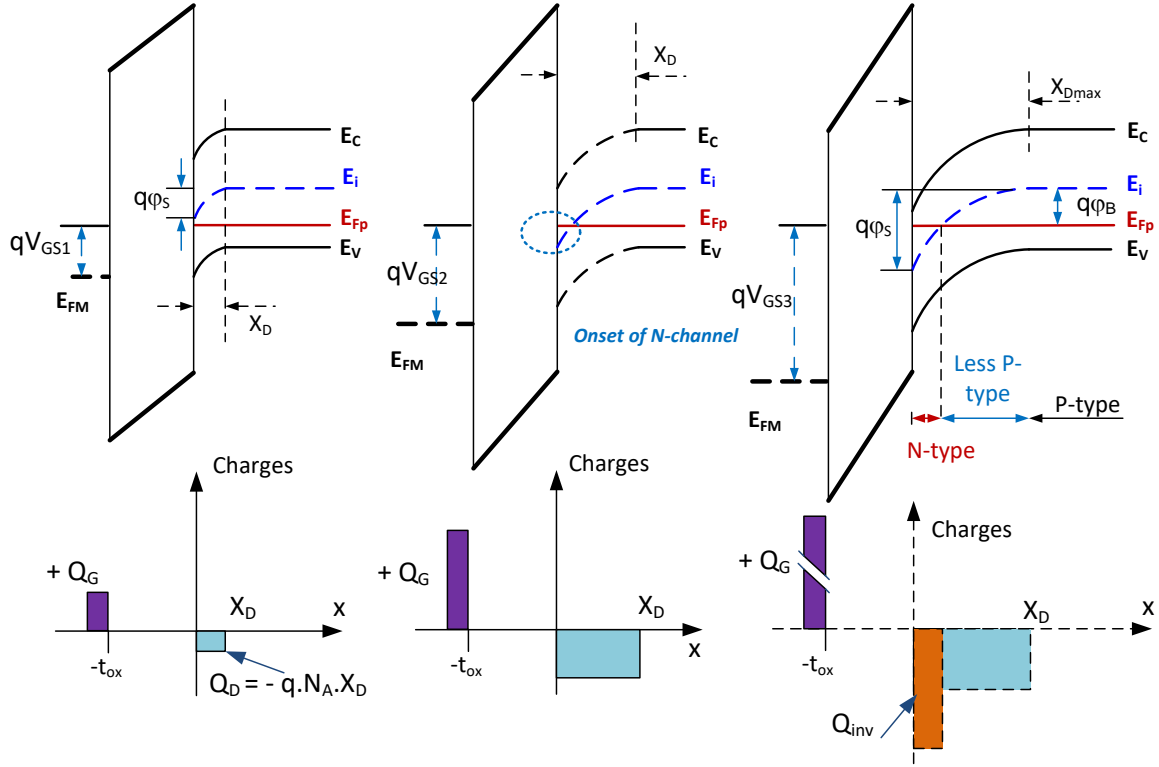


Figure 2.4. Energy-band diagrams for an N-channel MOSFET under different conditions (After [3, 27, 30])

Since the E_{Fp} crosses the E_i , minority carriers (electrons) are thermally generated to form an inversion layer, the sequence $\phi_B < \phi_S < 2\phi_B$ is called weak inversion. If the gate voltage is further increased so that $\phi_S = 2\phi_B$, the density of the free electrons at the interface exactly equals the free holes of the body. At this point, the depletion region disappears, and an inversion layer of the electrons is formed at the surface. It is said that the P-base interface is inverted to N-type. This particular set point defines the threshold voltage and it marks the beginning of strong inversion.

As shown in Figure 2.5, by applying an external voltage $V_{GS} = V_{FB}$, referred as flat-band voltage that caused no band bending (i.e. $\phi_S = 0$) in the semiconductor.

$$V_{FB} = \frac{\Phi_G - \Phi_S}{q} = \frac{\Phi_{GS}}{q} \quad (2-4)$$

For N-channel MOSFET, V_{FB} is negative because Φ_{GS} is negative. The gate-applied voltage is distributed partly across the oxide and across the surface region of the semiconductor:

$$V_{GS} = V_{FB} + V_{OX} + \phi_s \quad (2-5)$$

From the charge point of view, there are 3 charges in the system: the gate charge Q_G , the interface charge Q_{OX} due to the imperfections of the oxide, and the total charge Q_S induced in the P-substrate by the gate voltage. The charge balance gives:

$$Q_G + Q_{OX} + Q_S = 0 \quad (2-6)$$

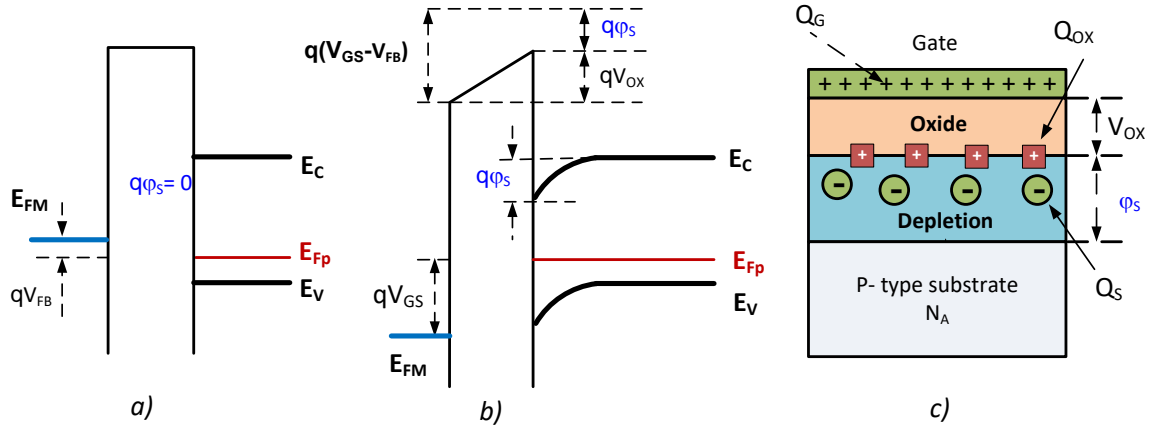


Figure 2.5. Charges and potentials of MOSFET with different gate bias [30]

Under positive gate bias, the total charge Q_S in the P-substrate is composed of a fixed charge Q_D in the depletion region under the gate, and a mobile charge Q_{inv} filling the inversion layer at oxide-semiconductor interface. The voltage across the oxide is given by:

$$V_{OX} = -\frac{Q_S}{C_{OX}} = -\left(\frac{Q_D}{C_{OX}} + \frac{Q_{inv}}{C_{OX}}\right) \quad (2-7)$$

where C_{OX} is oxide surface capacitance (in $F \cdot cm^{-2}$, electrical charges being expressed in $C \cdot cm^{-2}$). Under depletion or weak inversion regime ($0 < \phi_s < 2\phi_B$), surface potential is essentially held by the depletion region, the width of which can then be written as:

$$X_D = \sqrt{\frac{2 \cdot \epsilon_s \cdot \phi_s}{q \cdot N_A}} \quad (2-8)$$

Under strong inversion regime ($\phi_s > 2\phi_B$), it is assumed that additional gate charges induce the electrons in the inversion layer [3]. Therefore, the charge Q_D in the depletion region, and the associated width, remain almost constant. As a result, the applied gate voltage can be expressed under positive bias as follows:

$$\begin{cases} 0 \leq \psi_s \leq 2\psi_B \Rightarrow V_{GS} = V_{FB} + \phi_s + \frac{q \cdot N_A}{C_{OX}} \cdot \sqrt{\frac{2 \cdot \epsilon_s \cdot \phi_s}{q \cdot N_A}} \\ \psi_s > 2\psi_B \Rightarrow V_{GS} = V_{FB} + \phi_s + \frac{q \cdot N_A}{C_{OX}} \cdot \sqrt{\frac{4 \cdot \epsilon_s \cdot \phi_B}{q \cdot N_A}} - \frac{Q_{inv}}{C_{OX}} \end{cases} \quad (2-9)$$

Finally, this results for the threshold voltage V_{TH} in:

$$V_{TH} = V_{FB} + 2\phi_B + \frac{\sqrt{4 \cdot q \cdot N_A \cdot \epsilon_s \cdot \phi_B}}{C_{OX}} \quad (2-10)$$

2.2.2. The first quadrant operation

In the above-threshold regime, an inversion layer is formed in the entire length of the channel. Since the thickness of the inversion layer remains uniform, the charge density is approximately constant along the whole length of channel, and can be evaluated through:

$$Q_{inv} = -C_{ox} \cdot (V_{GS} - V_{TH}) \quad (2-11)$$

In the forward on-state, as I_D flows through the channel, the voltage drop $V_{CH}(y)$ increases alongside the channel due to its ohmic nature. As a result, the channel surface potential V_{OV} decreases along the channel, as depicted in Figure 2.6:

$$V_{OV}(y) = V_{GS} - V_{TH} - V_{CH}(y) \quad (2-12)$$

The inversion layer charge density can then be written as a function of the local charge density which in turn depends on the local channel voltage $V_{CH}(y)$ and the V_{GS} voltage:

$$Q_{inv}(y) = -C_{ox} \cdot (V_{GS} - V_{TH} - V_{CH}(y)) \quad (2-13)$$

The resistive voltage drop $dV_{CH}(y)$ across a small section of channel is given by:

$$dV_{CH}(y) = I_D \cdot dR_{CH}(y) \quad (2-14)$$

where $dR_{CH}(y)$ is the resistance of the considered small section:

$$dR_{CH}(y) = \frac{dy}{\mu \cdot W \cdot |Q_{inv}(y)|} \quad (2-15)$$

with dy the length of the considered small section, W its width, and μ the charge carrier mobility in the channel. Then, equation (2-14) leads to:

$$I_D \cdot dy = W \cdot \mu \cdot C_{ox} \cdot (V_{GS} - V_{TH} - V_{CH}(y)) \cdot dV_{CH}(y) \quad (2-16)$$

which results, by integrating the above equation from the source to the drain, in:

$$I_D = \frac{W \cdot \mu \cdot C_{ox}}{L} \cdot \int_{V_{CH}(0)}^{V_{CH}(L)} (V_{GS} - V_{TH} - V_{CH}) \cdot dV_{CH} \quad (2-17)$$

Finally, as $V_{CH}(0) = 0$, and as $V_{CH}(L)$ is the drain to source voltage V_{DS} , the channel output characteristic can be written as:

$$I_D = \frac{W \cdot \mu \cdot C_{ox}}{L} \cdot (V_{GS} - V_{TH} - \frac{V_{CH}}{2}) \cdot V_{CH} \quad (2-18)$$

If V_{DS} is far lower than $V_{GS} - V_{TH}$, it can be deduced from equation (2-18) that the channel electrical behavior is nearly linear. This operation mode is usually referred as the ohmic region, and it constitutes the steep part of the output characteristics, which corresponds to the fully on-state of MOSFET [7, 64].

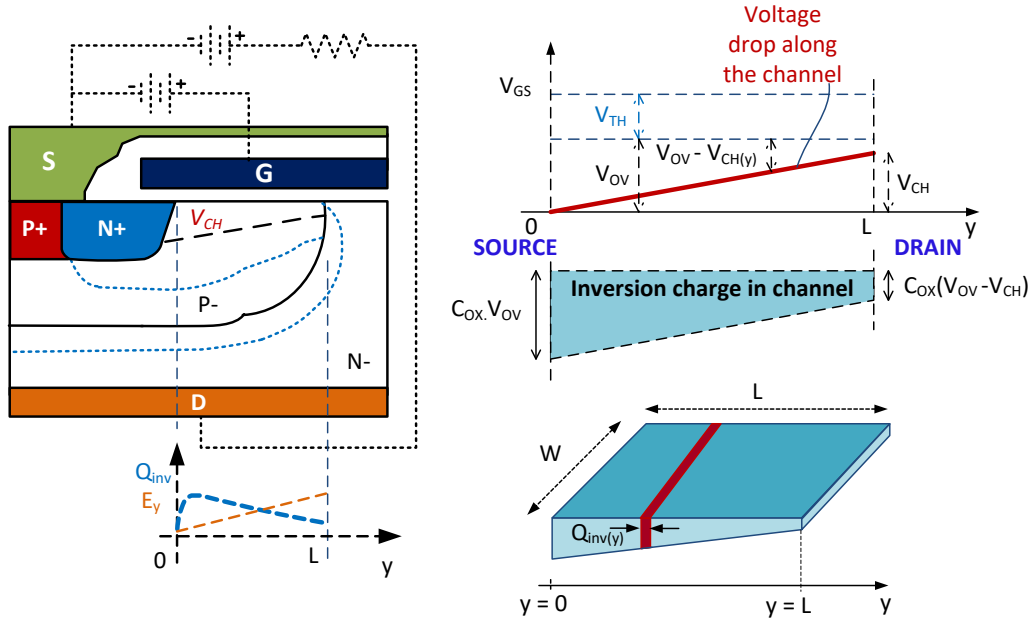


Figure 2.6. Inversion layer thickness vs V_{DS}

As soon as the V_{DS} increases substantially, the V_{CH} become large enough, so

$$V_{CHsat} = V_{GS} - V_{TH} \quad (2-19)$$

At the drain side, the inversion layer does not exist any longer ($Q_{inv}(L) = 0$), which is referred as the channel pinch-off. The drain-source voltage V_{DS} for channel pinch-off is called the saturation voltage, V_{Dssat} at which the saturation current I_{Dsat} is calculated as:

$$I_{Dsat} = \frac{W \cdot \mu \cdot C_{ox}}{2 \cdot L} \cdot (V_{GS} - V_{TH})^2 \quad (2-20)$$

The current does not increase with change of V_{DS} and is entirely controlled by V_{GS} . The MOSFET acts as a current source in saturation region. Beyond the pinched-off, the depletion region penetrates the P-body. Consequently, the channel is shortened (length reduced to $L' < L$, as shown in Figure 2.7).

This shortening of the channel length involves a slight ascent of the current at high V_{DS} [6]. The channel-length modulation λ usually is used in the current calculation:

$$I_{Dsat} = \frac{W \cdot \mu \cdot C_{ox}}{2 \cdot L} \cdot (V_{GS} - V_{TH})^2 \cdot (1 + \lambda \cdot V_{DS}) \quad (2-21)$$

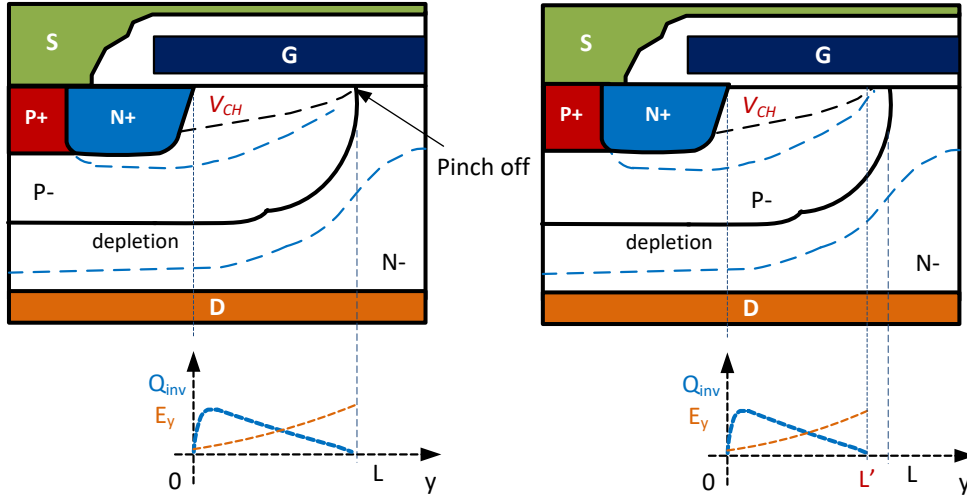


Figure 2.7. The inversion layer after pinch-off

Figure 2.8 hereafter presents typical forward output characteristics of a SiC power MOSFET. Only ohmic operating mode previously described can be clearly observed: a quite resistive electrical behavior at low drain voltage, and a quasi-saturation behavior at higher drain voltage, notably at low level of gate voltage.

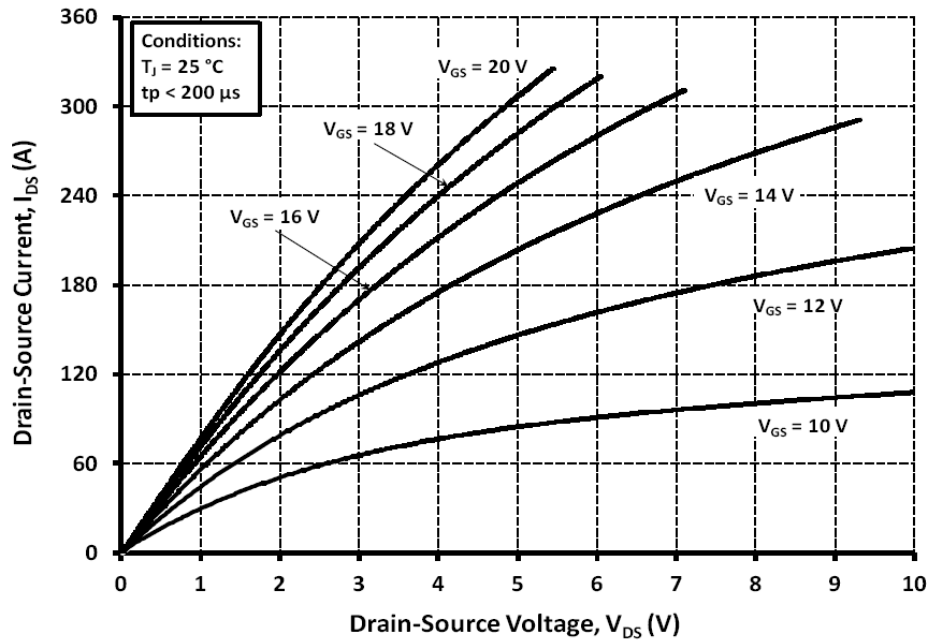


Figure 2.8. Forward output characteristics of 120 A – 1.2 kV SiC MOSFET at 25°C

2.2.3. The third quadrant operation

Third quadrant operation corresponds to a reverse conduction mode under negative V_{DS} . As indicated in Figure 2.9, the reverse current flows through the body diode, or/with the conduction of the channel as the same path described for forward conduction. Therefore, the body diode determines the MOSFET third quadrant operation, especially for zero gate bias $V_{GS} = 0$. The inherent presence of the body diode makes MOSFET attractive to bi-directional application.

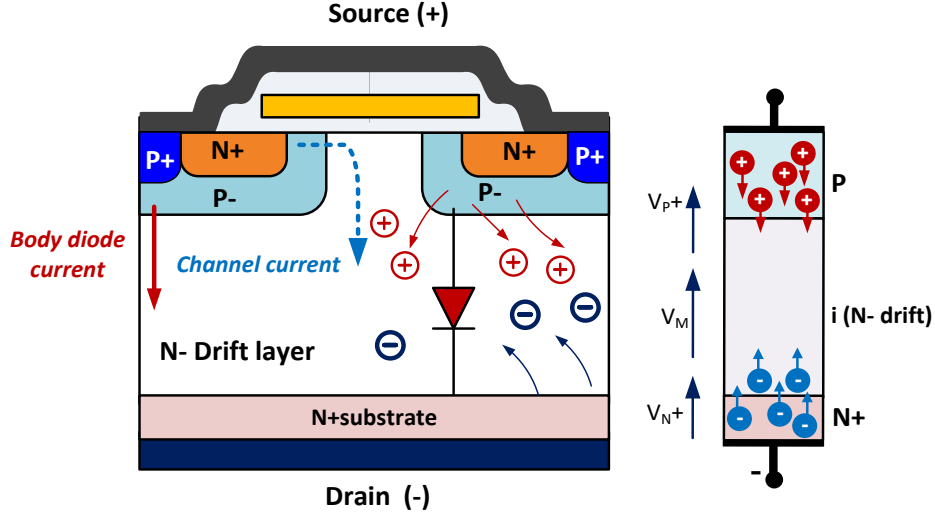


Figure 2.9. Current in reverse conduction

The MOSFET body diode is formed by a lightly N- drift between N+ drain and P-body of source. It shares the operation principles with PiN diode. During the forward conduction, the carriers inject from high concentration regions into the N-drift layer as illustrated in Figure 2.9. Thus, the forward voltage of body diode V_F comprises three main terms: the voltage drop across the drift region V_M , junction voltages V_{P+} and V_{N+} .

The V_M depends on carrier lifetime and N-drift layer thickness. As expected, high minority carrier lifetime (τ_p) and a small epitaxial layer achieve a lower V_M [3, 6, 65]. However, low τ_p of about 10 ns in 4H-SiC can result in high V_M . Moreover, the sum of the two junction voltage drops can be written as:

$$V_{P+} + V_{N+} = \frac{k \cdot T}{q} \cdot \ln \left(\frac{p(0) \cdot p(W)}{n_i^2} \right) \quad (2-22)$$

The sum of 2 voltages significantly depends on the n_i , which is far lower for 4H-SiC ($6.7 \times 10^{-11} \text{ cm}^{-3}$ at 300 K) than for Si ($1.4 \times 10^{10} \text{ cm}^{-3}$ at 300 K). As a result, V_F of SiC body diode is on the order of 2-4 V for a 4H-SiC in compared with 0.82 V for the silicon. In the third quadrant, the power dissipation in the 4H-SiC body diode is therefore four times greater than in the Si counterpart [6].

During the turn-off, the minority carriers (holes) must be removed from the drift region. Due to smaller physical area of the die, there is much smaller area for stored charges in SiC MOSFET body diode. Furthermore, the short τ_p facilitates faster the carriers' recombination. For these reasons, SiC MOSFETs body diode have excellent switching performance by reducing reverse recovery time [66,

67]. However, it is recommended to use Schottky diodes (SBD) in anti-parallel with 4H-SiC power MOSFETs to carry the current in the third quadrant due to the large on-state power loss [68].

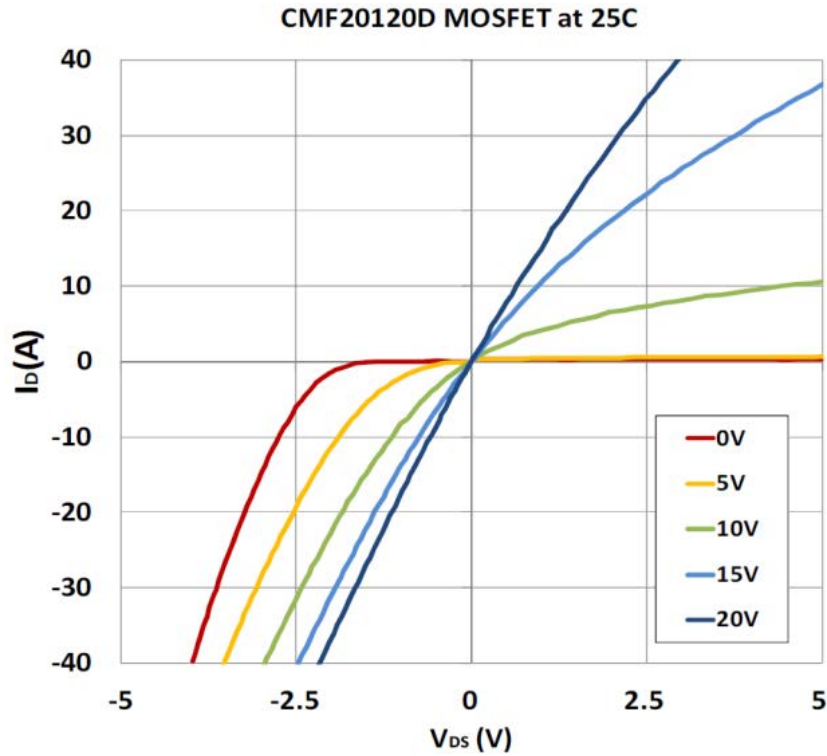


Figure 2.10. Output characteristics curves

Figure 2.10 presents typical output characteristics of a SiC MOSFET in both first and third quadrants. Since the inversion channel is turned-on, the third quadrant operation is symmetric to that of the first quadrant operation at low current level. At high current level, $V_{DS(on)}$ approaches the V_F , the body diode connects in parallel with the channel, leading to a greater current in comparison with first quadrant operation. Another consequence is that no current saturation is observed in the third quadrant mode. The MOSFET is current reversible, meaning that the current can also flow from the source to the drain. This mode of operation enables the device to be used for synchronous rectification, an asset not allowed with IGBT or BJT.

2.2.4. Forward off state (blocking)

Without gate bias, the power MOSFET can support a high positive V_{DS} . The N+ source and P-body junction are shorted via source metallization to suppress the parasitic bipolar transistor (BJT). Therefore, the blocking voltage is supported across a depletion layer of body diode and a MOS interface as illustrated in Figure 2.11 [3, 7, 48, 69].

The power MOSFET blocking capability is limited by the avalanche breakdown of P-N junction as discussed in section 1.2.2. It can be seen in Figure 2.11, the depletion region extends mostly into N-drift region. Therefore, the voltage breakdown is determined by the doping concentration of donors (N_D) and the thickness X_D of the N-epitaxial drift layer [7, 70]. The avalanche breakdown voltage MOSFET increases with the increase of the junction temperature [71, 72].

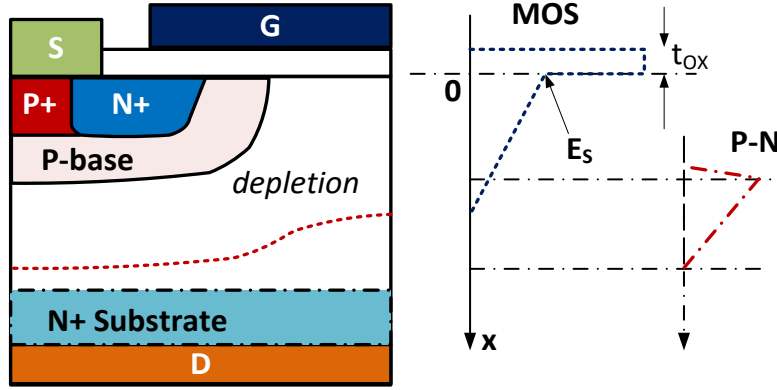


Figure 2.11. Electric fields in the VDMOSFET in the blocking state (after [3, 73, 74])

The maximum electric field at $x = 0$ (at the surface of N-drift) can be calculated as:

$$E_s^{\text{off}} = \frac{q \cdot N_D \cdot X_D}{\epsilon_s} \quad (2-23)$$

As shown in Figure 2.11, the oxide field is higher than the peak field in the semiconductor, due to the difference in dielectric constant for the two materials. The electric field E_s increases rapidly with increasing V_{DS} . Since the gate oxide is not shielded from the drain potential, high electric field in the gate oxide in the blocking mode causes reliability MOS problems. It will be discussed in section 2.3.2.

With the V_{DS} increase, the depletions can be developed in P-base region as shown in Figure 2.12. In a lightly doped and narrow P-base region, the depletions can exceed its thickness prior to the onset of avalanche breakdown. This phenomenon is called punch-through or reach-through. Hence, the blocking capability of power MOSFET is also limited by the width and doping in the P-base [7, 48]. However, longer channel results in higher channel resistance R_{CH} . High implant dose in P-base is beneficial from the punch-through, which results in carrier mobility reduction and increase of threshold voltage [75].

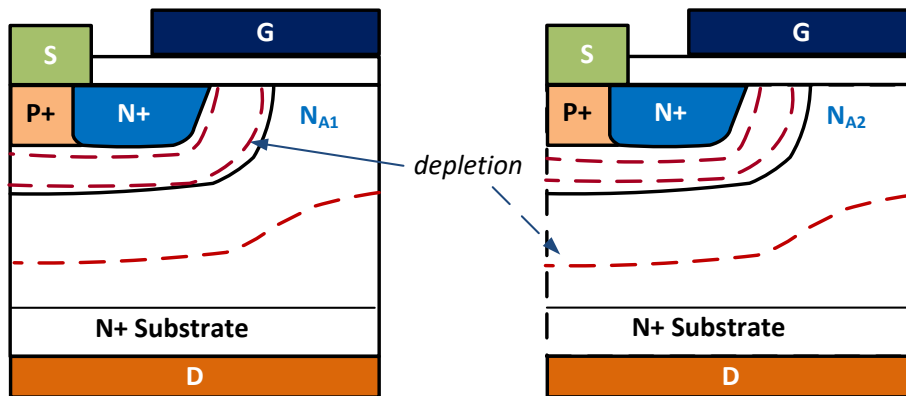


Figure 2.12. Reach-through and P-base doping

Nevertheless, P-base doping N_A influences the parasitic bipolar junction transistor (BJT). Looking at Figure 2.13, the parasitic transistor is formed by the N+ region of source, P-base region of the body, and N-drift region.

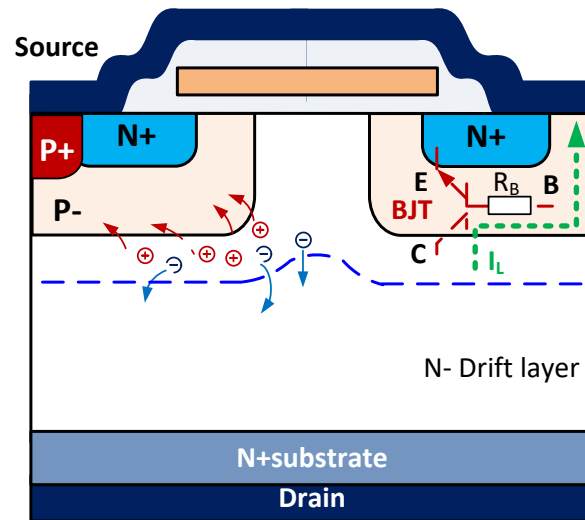


Figure 2.13. Second breakdown from the parasitic NPN bipolar transistor (after [7, 20])

Ideally, the base current is held at zero ($I_B = 0$). In blocking mode, at high electric field, electron-hole pairs are generated within depletion region. The generated holes I_L flow towards the source via the R_B of the P-base region, as illustrated in Figure 2.13 [20]. If the base resistance R_B is high, a voltage drop in the base $V_{BE} = I_L \times R_B$ can exceed a certain level (0.7 V as mentioned in [75]) to turn on parasitic BJT, referred to the secondary breakdown of the parasitic BJT. Typically, a heavily doped P+ region is formed inside the N+ source region to reduce R_B [7, 20, 76].

No	Breakdown by	Effects
1	P-N junction	Avalanche multiplication
2	Parasitic BJT	Near avalanche (snapback)
3	Depletion region	Punch or reach through
4	Gate structure	Gate breakdown

Table 2.2. Breakdown occurs in a MOSFET by some effects

As discussed above, the blocking capability of power MOSFET is not only determined by the avalanche of the N-drift region but also by the effects on P-base and gate, as given in Table 2.2.

2.3. SiC MOSFET gate oxide challenges

2.3.1. Gate oxide growth

Thermal growth of SiO_2 on SiC can be carried out in a wet (H_2O) or dry (O_2) oxidation method in a diffusion furnace [9, 77-80]. The dry oxidation is done in pure O_2 (oxygen gas) in the high temperature in dry environment that results in a very good interface quality and high dielectric breakdown (11-12 MV/cm). Wet oxidation consists of supplying a mixture of saturated H_2O vapour and O_2 to the oxidation environment. The growth rate is much faster than in a dry one but wet oxidation also results in a lower dielectric breakdown strength [81-83]. Typically, the oxide growth rate of SiC is much lower than that of Si under the same conditions. The temperatures in excess of 1000°C are more practical to achieve the desired oxide thickness. As a compound material, the presence of C in SiC makes the interaction of the C-SiC- SiO_2 within oxide growth an extremely complex.

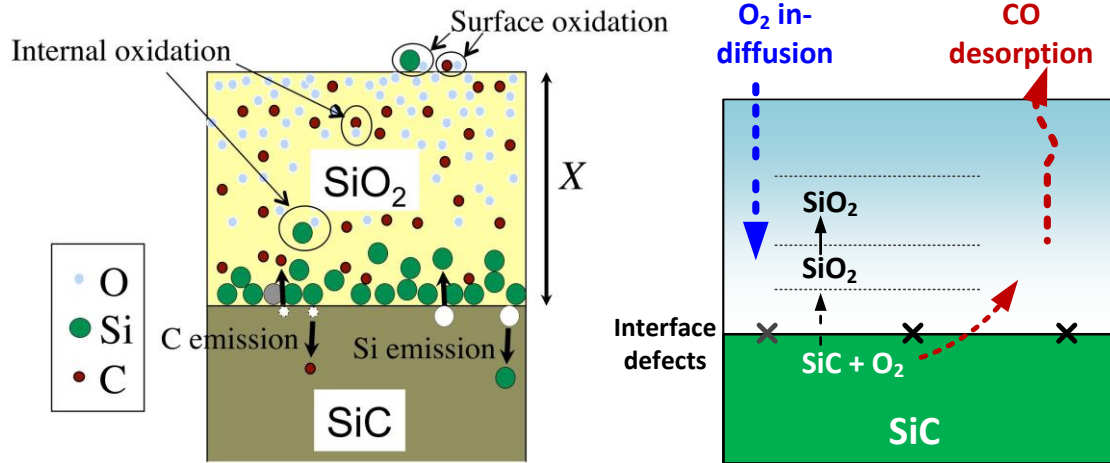


Figure 2.14. A schematic of SiO_2 growth by thermal oxidation of SiC (after [84, 85])

Several studies [86-88] indicated that the presence of C directly affects the dielectric properties of MOS structures. During thermal oxidation, most of the C in SiC converts to gaseous CO and CO_2 and releases from the oxide layer as shown in Figure 2.14. However, some of the carbon can remain within the oxide and form carbon clusters or graphitic regions. Such regions near the SiC-SiO₂ are expected to be electrically active and could be responsible for the interface states [89].

2.3.2. Gate oxide reliability

SiC MOS requires a special attention due to the reliability. Typically, the breakdown field of SiO₂ (E_{OXBR}) is about 10 MV/cm. Moreover, the oxidation of SiC under high temperature conditions results in the formation of a very high defect density at the oxide-SiC interface, leading to the MOS interface quality issues [29, 31, 69, 73, 90]. For the long-term reliability of SiC MOSFET, the maximum electric field in the dielectric is limited to approximately 4 MV/cm with positive bias, about 1.6 MV/cm under negative bias [91, 92].

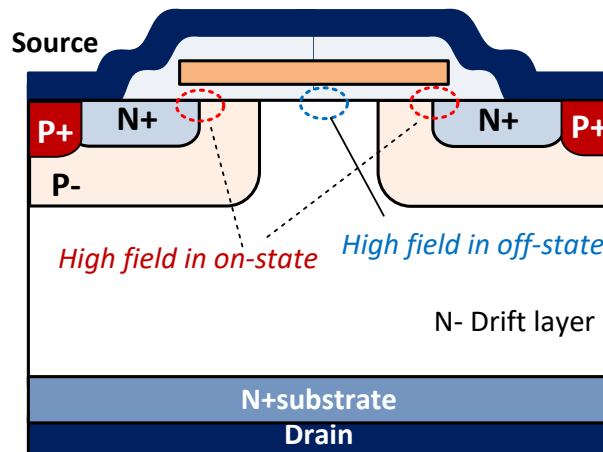


Figure 2.15. Planar gate VDMOSFET oxide reliability (after [20, 73, 74])

The electric field in the gate oxide (E_{SiO_2}) for the power planar MOSFET structure is larger than in the semiconductor by the ratio of dielectric constants [3]:

$$E_{\text{SiO}_2}^{\text{off}} = \frac{\epsilon_{\text{SiC}}}{\epsilon_{\text{SiO}_2}} \cdot E_{\text{Si(0)}}^{\text{off}} \quad (2-24)$$

Using $\epsilon_{\text{SiC}} \approx 10$, $\epsilon_{\text{SiO}_2} \approx 3.9$, meaning the E_{SiO_2} is about 2.5 times higher than the peak field in the semiconductor $E_{\text{Si(0)}}^{\text{off}}$. As depicted in Figure 2.15, at blocking mode, $E_{\text{Si(0)}}^{\text{off}}$ is about 0.3 MV/cm of Si MOSFET, leading to $E_{\text{SiO}_2}^{\text{off}}$ of 0.75 MV/cm. However, working at high voltage, SiC MOSFET $E_{\text{Si(0)}}^{\text{off}}$ can reach to 1.5 MV/cm. $E_{\text{SiO}_2}^{\text{off}}$ then is about 3.75 MV/cm, close to the maximum allowable field for long reliability.

Because of the larger band gap, the lower barrier heights for electrons' injection into SiO_2 enhance the FN tunneling which may lead to the failures of gate oxide in on-state at high gate voltage and high temperatures, as discussed in section 1.5.2. Therefore, the gate voltage applied to the oxide without any failure is determined as:

$$V_{\text{OXBR}} = E_{\text{OXBR}} \cdot t_{\text{OX}} \quad (2-25)$$

where V_{OXBR} is the gate oxide breakdown voltage, t_{OX} is the oxide thickness. For the typical 50 nm gate dielectric thickness at room temperature, the maximum gate bias must be limited within [-5 V, +15 V].

2.3.3. Interface traps

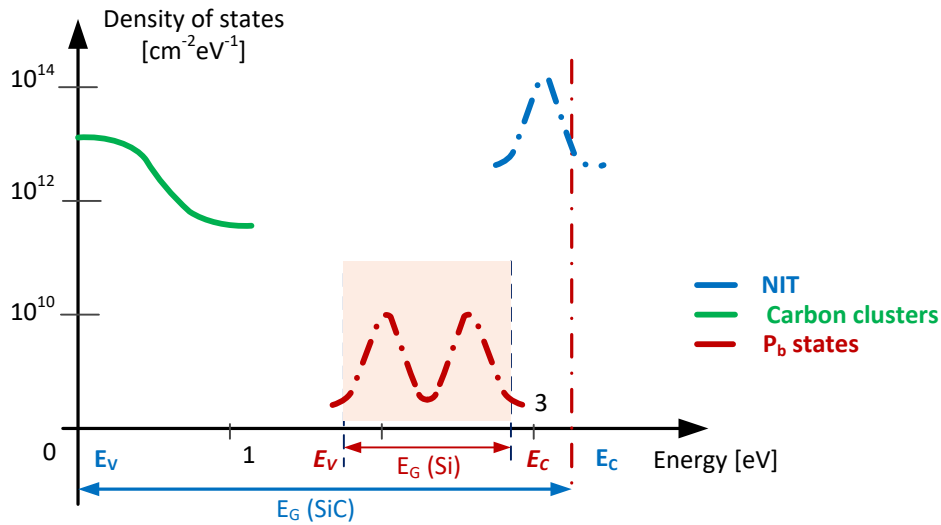


Figure 2.16. Schematic energy distribution and contributions to the SiO_2 interface (after [20, 93, 94])

As shown in Figure 2.16, the density of states D_{it} at SiC-SiO_2 is composed of 3 different types of traps: dangling bond centers (so-called P_b centers), carbon clusters and Near Interface Traps (NITs)[94].

It has been many times repeated in the literature [13, 95-97], P_b is silicon or carbon dangling bond centers in the SiC-SiO_2 , which appear at the mid-gap. The dangling bond centers play only a marginal role compared to the total density of traps at SiC-SiO_2 interfaces. That is why the impact of hydrogen annealing which is key to the quality of Si-SiO_2 interfaces, proved ineffective on improvement D_{it} in SiC-SiO_2 structures [93, 98, 99].

NIT states are observed typically in oxide of Si and SiC, due to an intrinsic oxide defect. The traps appear at 2.8 eV below the SiO₂ conduction band bottom, about 0.35 eV above the E_C of Si. The highest D_{it} lies outside the Si band gap energy. Therefore, the states do not affect the channel mobility at Si-SiO₂ interfaces. However, these states located slightly close (0.1 eV below) to the E_C edge of SiC which may contribute to D_{it} at particularly 4H SiC-SiO₂ interfaces [96, 100]. The high density of trap states D_{it} close to the conduction band decreases the inversion layer mobility, thereby limiting the performance of SiC MOSFET devices.

The carbon cluster-related interface states can energetically be distributed over the whole SiC band gap, particularly at the valence band edge. The defect states at the interface can be passivated by NO [11, 13, 94].

Compared with Si, the interface trap issue is more serious in SiC-based MOS devices. The density of interface traps D_{it} is about $10^{10}\text{cm}^{-2}\text{eV}^{-1}$ for Si MOS while the D_{it} for SiO₂-4HSiC is widely reported to be above to $10^{13}\text{cm}^{-2}\text{eV}^{-1}$ [40, 93, 98, 101, 102]. Furthermore, the total D_{it} distribution is not uniform over energy as shown in Figure 2.16 which leads to technical issues of SiC MOSFET.

2.3.4. Oxide charges

There are general 4 types of charges associated with non-ideal SiC-SiO₂ system as shown in Figure 2.17, that affect the devices in different ways [3, 30].

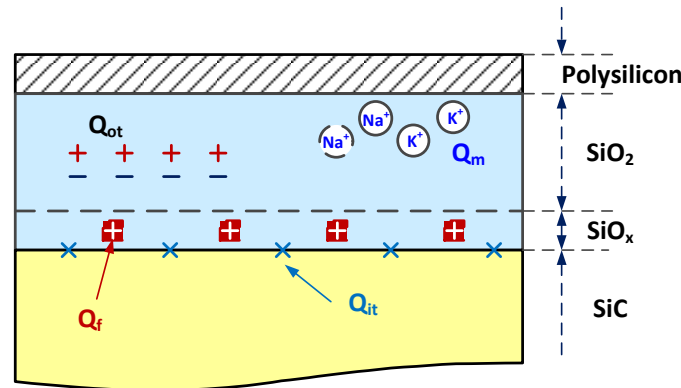


Figure 2.17. Oxide charges in SiC-SiO₂ (after [30])

Fixed oxide charge (Q_f) is fixed positive, located near the interface due to primarily structural defects in the oxide layer. Oxide trapped charge (Q_{ot}) is distributed in the bulk of the oxide, due to injection of carriers from the substrate or from the gate material. Mobile ionic charge (Q_m) is due to the presence of ionic impurities such as Na⁺, K⁺ and possible H⁺ during the oxidation process. These charges strongly affect the V_{TH} of the MOS devices [30, 103, 104].

Interface trapped charge (Q_{it}) is due to the states at the SiC-SiO₂ interface. The interface states introduce energy levels throughout the whole band gap. The states above the intrinsic energy level E_i is called as the acceptor-like states. The donor-like states are located below E_i . All the interface states above E_{Fp} are empty, while the states below the E_{Fp} are occupied by electrons. Thus, the charge of the interface states is thus a function of the gate voltage applied across the MOS device as illustrated in Figure 2.18 [105].

Q_{it} is positive at flat-band biased. After filling the states by electrons, the acceptor-like states become negatively charged, while the donor-like ones become neutral. Therefore, Q_{it} decreases in depletion mode. At inversion condition, the more bands bending in the surface, more acceptor-like traps are filled by electrons and Q_{it} becomes negative.

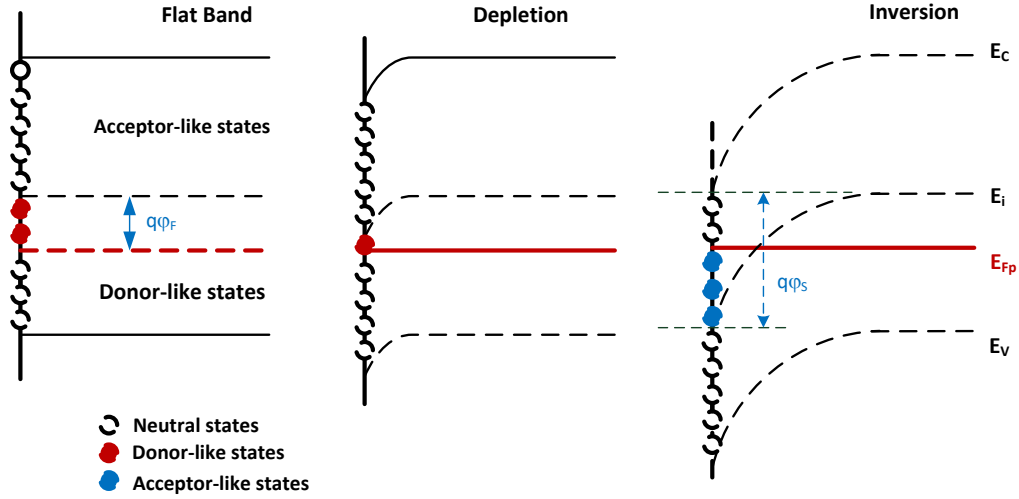


Figure 2.18. Band diagram of N-channel MOSFET in different gate bias

Thus, acceptor-like traps close to the E_c of SiC with the negative charges form the Coulomb scattering centers which have several effects on the device performance [3, 106]:

1. Trapping of electrons from the inversion layer
2. A shift of the threshold voltage
3. A reduction of the mobility of the electrons in the inversion layer

Parameters	Q_f	Q_{ot}	Q_m	Q_{it}
Location	Near interface	Within the oxide	Within the oxide	At interface
Charge	+	+/-	+	+/-
Cause	Structural defects	Ionizing radiations	Ionic impurities	Structural defects
Depend on V_{GS}	Not	Not	Yes	Yes
Charging state	Fixed	Changed and discharge under specific conditions	Fixed at small T	by V_{GS} , T
Affect	V_{FB}	V_{FB}	V_{FB}	V_{FB} , mobility

Table 2.3. Oxide charges and effects

2.4. SiC MOSFET technical issues

2.4.1. Threshold voltage

The V_{TH} instability is one of the most critical challenges in the reliability of SiC MOSFET, which has been examined in numerous reports [74, 107, 108]. For N-channel MOSFET, a negative shift of V_{TH}

leads to significant leakage current in the off-state, and potentially to a device failure. On the other hand, the increase of V_{TH} results in higher on-resistance, reducing the efficiency.

Due to the imperfections of the SiC-SiO₂ interface, the oxide charges cause a significant variation of the ideal V_{FB} as shown in the Table 2.3. Thus, the oxide charges Q_{OX} is considered in the expression for flat-band voltage, the equation (2-4), now is [30, 41]:

$$V_{FB} = \frac{\Phi_{GS}}{q} - \frac{Q_{OX}}{C_{OX}} \quad (2-26)$$

$$Q_{OX} = q \cdot (N_{it} + N_{ot} + N_f + N_m) \quad (2-27)$$

where N_{it} , N_{ot} , N_f and N_m are the density of occupied interface traps, oxide traps, fixed charge and mobile ions, respectively. V_{TH} depends on gate bias, temperature, and time which stems from the charging and discharging of oxide traps [90, 108-110].

The V_{TH} variation is explained by the electron filling or emptying at the interface traps in response to gate bias stress. The V_{TH} increase relates to the trapping of electrons with a positive gate bias stress; while the V_{TH} drops with a negative gate voltage because of the trapping of holes. A high magnitude gate bias stress results in a large V_{TH} instability. The longer the stresses, the deeper traps into the oxide interface are. Therefore, longer stress times leads to larger V_{TH} shifts. Although the gate bias changes between positive and negative in the normal switching operation, the repeated charge and discharge of the traps have no significant change in the V_{TH} of SiC MOSFET [41, 107, 109].

2.4.2. Channel mobility

Under the influence of an electric field E (V/cm), the carriers subject to an electrostatic force, accelerate and progressively acquire greater speed. However, due to collisions (often called scattering) with other carriers and with atoms in the semiconductor, the carriers lose some energy and momentum to reach new values of velocity. The ratio of the average velocity v (cm/s) to the applied field is defined as the mobility μ (cm²/Vs) which is dependent on scattering mechanism and effective mass as:

$$\mu = \frac{v}{E} = \frac{q \cdot \tau_s}{m^*} \quad (2-28)$$

where m^* is the mass of the carrier, τ_s is scattering time.

a. Bulk mobility

In the bulk, the mobility is a strong function of the lattice temperature and ionized impurity concentration [6, 7]. The atom vibrations in a crystal lattice create waves by means of phonons that collide with the carriers, known as lattice scattering μ_{LS} . The mobility μ_{LS} reduces with temperature. The collision of carriers with the ionized doping atoms is referred as impurity scattering μ_{IS} . The probability for collision increases at high impurity concentrations, resulting in lower mobility μ_{IS} . At high temperatures, carriers move more quickly, less time for them to interact with charged impurities. As a result, the mobility μ_{LS} increases with temperature which is the opposite of the effect of μ_{IS} . The two scattering phenomena affects simultaneously the carriers through Matthiessen rule where bulk mobility μ_B can be written as:

$$\frac{1}{\mu_B} = \frac{1}{\mu_{LS}} + \frac{1}{\mu_{IS}} \quad (2-29)$$

The bulk mobility depends on both doping and temperature, which is described by [3, 6, 111, 112]:

$$\mu_{e(4H-SiC)} \approx \frac{1020}{1 + \left(\frac{N_D + N_A}{1.8 \times 10^{17}} \right)^{0.6}} \cdot \left(\frac{T}{300} \right)^{-n} \quad (2-30)$$

where the value n strongly depends on the doping. The n value is 2.2-2.8 for lightly doped and 1.5 for highly doped N-type 4H-SiC [3, 113, 114].

b. Surface scattering - vertical electric field dependence of mobility

The channel mobility is affected by surface scattering mechanisms when carriers flow at the surface of a semiconductor, resulting in a lower mobility than bulk one. Similar to the ordinary lattice vibrations in the bulk, the surface acoustic phonon scattering (μ_{AC}) is the lattice vibration within an active area near the surface. The mobility μ_{AC} decreases with the increase of temperature and vertical field, which can be written [115-117] as:

$$\mu_{AC} = \frac{A}{E_x} + \frac{B}{T \cdot (E_x)^{1/3}} \quad (2-31)$$

where A and B are parameters evaluated by fitting theory to experiment, and E_x is the vertical electric field (perpendicular to the surface).

In SiC MOSFET, the trapped electrons form charged centers near the SiC-SiO₂ interface which are the same charge type as the mobile inversion charge in channel, leading to Coulomb repulsion. Coulomb mobility can be expressed as [111, 118-120]:

$$\mu_c = \frac{\Gamma_c \cdot (N_{inv})^{\zeta_B}}{(N_{it} + N_f)} T \left(1 + \frac{n}{n_c} \right)^{\zeta_C} \quad (2-32)$$

where N_{inv} is the density of electrons in the MOSFET inversion layer, n is the electron concentration at the surface, Γ_c , n_c , and ζ_C are empirical parameters. ζ_B is a factor that describes the screening effects that are known as the damping of electric field of charged traps by the presence of mobile charge carriers.

Surface roughness scattering (μ_{SR}) is caused by imperfections between two different materials. The interface roughness produces a fluctuating oxide thickness, as well as inconsistent boundary at the surface in P-body, which causes variation in the electric field at the interface. Electrons are scattered at the interface. At relatively high vertical electric field E_x , the number of inverted mobile carriers increases. The carriers are confined closer to the gate oxide-semiconductor interface, resulting in lower μ_{SR} . As temperature increases, μ_{SR} slightly reduces [121, 122]. Thus, this scattering is essentially independent of temperature, which can be characterized by the following expression:

$$\mu_{SR} = \frac{\delta_{SR}}{E_x^2} \quad (2-33)$$

where δ_{SR} is a proportionality constant. The effect of scattering mechanisms on the inversion layer is multifaceted which can thus be described by the sum of all four terms:

$$\frac{1}{\mu_{inv}} = \frac{1}{\mu_B} + \frac{1}{\mu_{AC}} + \frac{1}{\mu_C} + \frac{1}{\mu_{SR}} \quad (2-34)$$

With additional scattering occurring in inversion layer, μ_{inv} is about 50 % for Si MOSFET, only about 5–10 % for 4H-SiC in compared with μ_B [3]. High density of interface traps (D_{it}) at the SiC-SiO₂ makes Coulomb scattering a strong influence to SiC MOSFET inversion mobility. Since μ_C is small, it controls the total inversion mobility. The extremely low channel mobility values, 5–10 cm².V⁻¹.s⁻¹ for 4H-SiC (0001) MOSFETs and 30–35 cm².V⁻¹.s⁻¹ for 6H-SiC (0001) MOSFETs are reported [93, 99, 101, 123].

c. Velocity saturation - longitudinal electric field dependence of mobility

The drift velocity increases linearly at low values of the electric field. The constant value of μ_{inv} is called the low-field mobility. As the lateral electric field is increased, the carrier velocity increases sub-linearly and asymptotically towards a maximum possible value, called the saturation velocity v_{sat} (1×10⁷ cm/s for Si, while for 4H-SiC, it is close to 2×10⁷ cm/s). This velocity is a characteristic of the material and a strong function of doping and temperature.

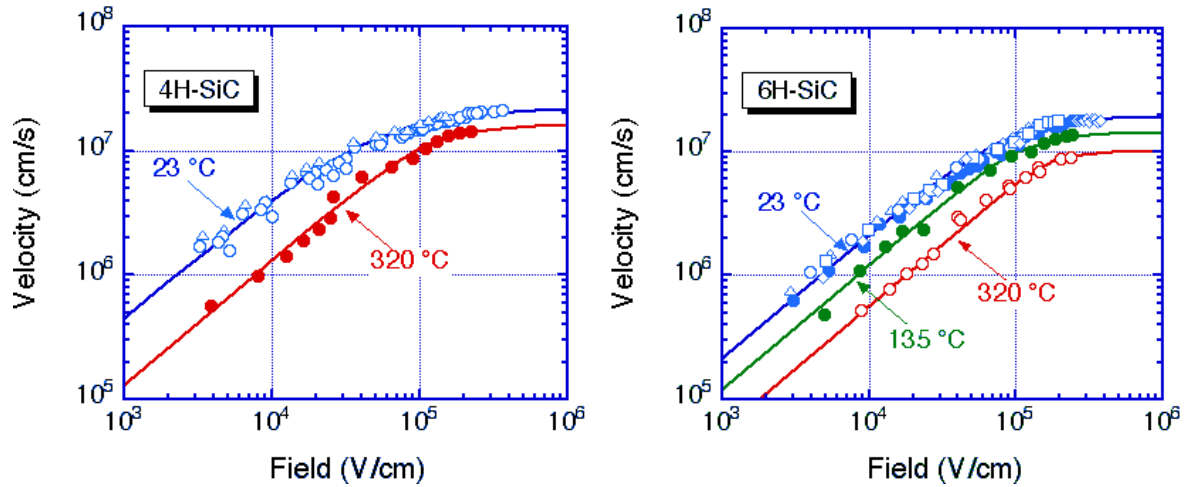


Figure 2.19. Drift velocity for electrons in SiC [12]

The v_{sat} results from a process called optical phonon scattering [111]. The only experimental data was published by Khan and Cooper [12] where the drift velocity of SiC (with N-doped at about 10¹⁷ cm⁻³) was measured as a function of electric field at different temperatures as seen in Figure 2.19. The saturation velocity decreases with temperature [124].

2.4.3. On-resistance

When the $V_{GS} > V_{TH}$, an inversion layer is formed in the channel. The electrons flow from N+ source through the inversion channel in a P-body region (P-well), and then turn downwardly to N-drift layer or vice versa. Thus, the drain and source are connected by a total on-resistance, referred to $R_{DS(ON)}$. The factors influencing the total on-resistance of the VDMOSFET are well understood and described

by Baliga in [48]. It is assumed here that the contact resistances to the source and backside drain regions are negligible. As depicted in Figure 2.20, the $R_{DS(ON)}$ consists of several terms:

$$R_{DS(ON)} = R_S + R_{CH} + R_{ACC} + R_{JFET} + R_{DRIFT} + R_{SUB} \quad (2-35)$$

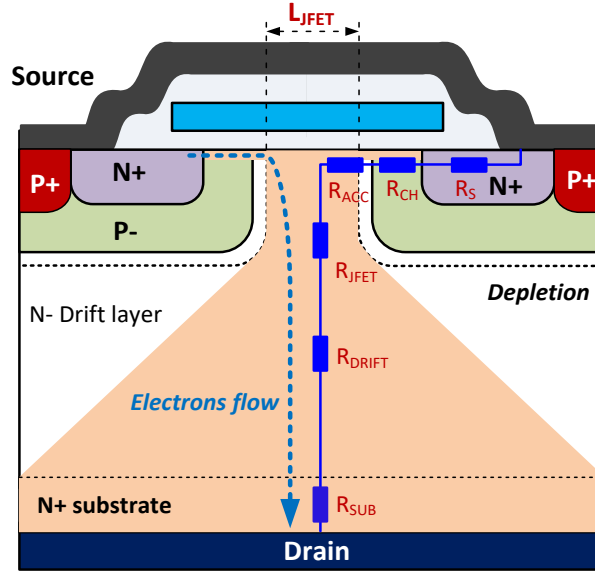


Figure 2.20. The internal resistances in a power MOSFET (after [49, 125])

The resistance of N+ source R_S is neglected. R_{CH} represents the channel resistance which depends on the length L , the width W of the channel, the carrier mobility μ , and the gate voltage [48, 126]:

$$R_{CH} = \frac{L}{W \cdot \mu \cdot C_{ox}} \cdot \frac{1}{V_{GS} - V_{TH}} \quad (2-36)$$

According to the above equation, shortening channel length results in lower R_{CH} . Therefore, 4H-SiC DMOSFETs with very short channel length (0.5 - 0.7 μm) have been developed. However, because of the various surface scattering mechanisms, low inversion-layer mobility has been observed in 4H-SiC MOSFETs that leads to their high channel resistances.

R_{ACC} is the resistance of the accumulation layer, appearing at the surface of the N-drift region under the gate electrode. As an electron-rich area, R_{ACC} plays a relatively small contribution in $R_{DS(ON)}$ which is often neglected.

R_{JFET} is the resistance of the JFET-like region between the two P-body implants which is the main inherent design issue in the planar gate DMOSFET structure [7, 49]. As depicted in Figure 2.20, the current flow is controlled by the JFET width in N-drift region (called L_{JFET}). With increasing of V_{DS} , the lateral depletion layers are extended into the N-drift region which restricts the vertical electron flow, resulting in higher JFET resistance. Thus R_{JFET} can be described by the following expression [7, 20]:

$$R_{JFET} = \frac{\delta_j}{W \cdot q \cdot \mu_{JFET} \cdot N_{JD} \cdot (L_{JFET} - k_J \cdot V_{DS})} \quad (2-37)$$

where N_{JD} is the doping concentration of the JFET region, μ_{JFET} is the bulk electron mobility within this region, k_j is a coefficient describing the reduction of JFET region width, and δ_j is the JFET region resistivity. The JFET resistance increases with the reduction of cell pitch (smaller L_{JFET}). Thus, for minimizing JFET resistance, the JFET doping concentration (N_{JD}) has been increased by phosphorus (P) implantation. This method is applied for the devices above 2 kV. However, higher doping in JFET region also increases the electric field in the oxide, which causes a negative effect on the long-term reliability in MOSFET blocking mode as well discussed in section 2.3.2 [62, 73, 127]. The effects of the JFET width and the JFET doping concentration on the on-resistance are shown in Figure 2.21. The term "w/ JD" means with JFET doping, "w/o JD" means without JFET doping, L_j refers L_{JFET} .

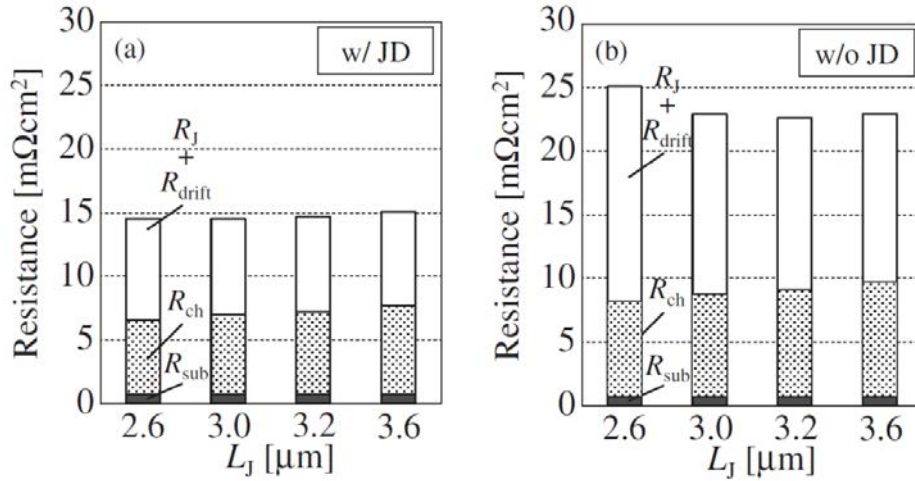


Figure 2.21. JFET length and doping dependence of specific on-resistance of 3.3 kV MOSFET [127]

R_{DRIFT} is the resistance of the N-drift region where the current from the JFET region spreads by an angle of 45° [48, 126], resulting in a trapezoidal shaped region of current flow as described in Figure 2.20. Since the spreading effect is not considered, the resistance of the N-drift layer is given simply by [7]:

$$R_{DRIFT} = \frac{X_D}{q \cdot \mu_e \cdot N_D} \quad (2-38)$$

where X_D is the thickness and N_D is N-drift region doping. Then, the current moves toward the drain end of device through a uniform area of N+ substrate.

The substrate resistance R_{SUB} is relatively high for medium voltage range SiC MOSFET rated 900 V - 1700 V, as shown in Figure 2.22. With planar DMOS structures, the new generation SiC MOSFET utilizing a small cell pitch (10 μm rating), has lower specific on-resistance by optimizing the N-drift doping and thickness of substrates (thinner) [59, 60, 128]. In this case, the resistances (R_{DRIFT} , R_{JFET} and R_{SUB}) are reduced, and then the channel resistance becomes dominant over the other $R_{DS(ON)}$ components. It is true for SiC MOSFET at medium voltage range. For higher voltage rating SiC MOSFET (3.3 kV), the thicker and light-doped drift layer makes R_{CH} negligible compared to R_{DRIFT} .

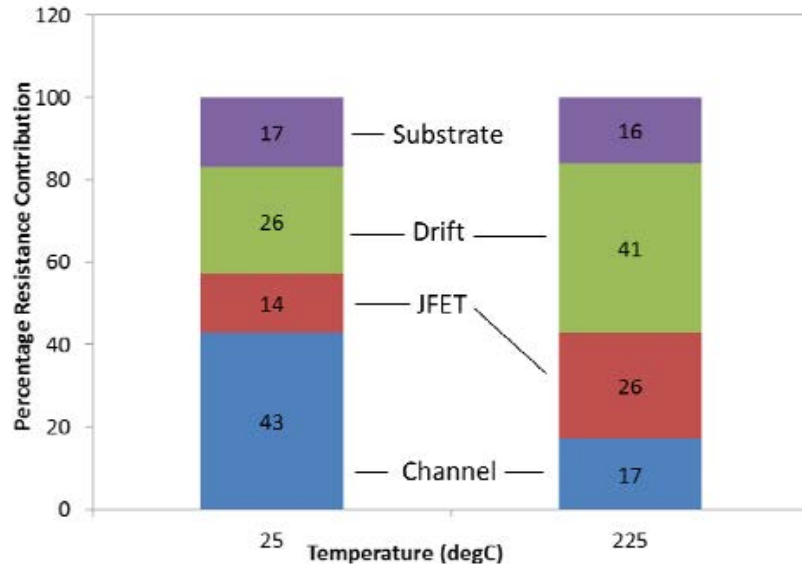


Figure 2.22. The shares of the particular parts of the resistance $R_{DS(ON)}$ of SiC MOSFET 1.7 kV [62]

2.5. Conclusion

This chapter systematically evaluates technical issues of the commercial SiC power MOSFETs which share the design, fabrication processes and operation principle with Si counterparts. The static operation of SiC MOSFET has been physically considered.

SiC MOSFETs take the advantages of thinner and higher doping of N-drift layers, offering low on-resistance. However, using planar gate with the presence of JFET resistance, there is trade-off for utilizing a compact cell and on-resistance. The N-drift doping needs to be optimized for minimizing the JFET resistance and improvement the reliability of device in the blocking mode.

The gate oxide is physically limited for both performance and long-term reliability of SiC MOSFET, particularly at high voltages and high temperatures. Due to high density of interface states appearing close to the conduction edge band of 4H-SiC as the traps for electrons, inversion channel mobility of 4H-SiC MOSFET is relatively low, thereby a high channel resistance percentage in on-resistance. Thus, SiC MOSFETs need a gate bias as high as +20 V to maximum performance. This requirement causes the gate reliability issues due to high density of the SiC-SiO₂ interface defects and low barrier height of 4H-SiC. Moreover, charging and discharging the oxide traps have an important effect on the threshold voltage instability.

Although SiC MOSFET's body diode has excellent reverse recovery characteristics, its relatively large forward voltage (V_F) results in high conduction loss in third quadrant operation. Thus, connecting an external anti-parallel SBD diode to SiC MOSFET is still recommended.

Chapter 3 SiC MOSFET on-state characterization

Interface traps are reported as the SiC MOSFET limitations (extremely low inversion mobility in the channel, tunneling effects...), they must be understood and overcome. Therefore, it is necessary to fully characterize the SiC MOSFET to provide an important foundation for its behaviors in a power electronics environment.

The device under test (DUT) is a 1.2 kV – 100 A SiC MOSFET half-bridge module manufactured by CREE. A 200 V – 250 A Si MOSFET from SEMIKRON is used as the Si counterpart for comparison. The forward operation (with a positive drain-source voltage V_{DS}) in terms of DC characteristics (I-V), threshold voltage V_{TH} and on-resistance $R_{DS(ON)}$ are studied. Due to the temperature dependence of the characteristics, all these characterization tests have been performed within a climatic chamber, under different temperatures from - 30 °C to 150 °C.

3.1. Pulsed DC measurement and self-heating constraint

The section highlights one of the precautionary measures to take when it comes to proceed to any characterization test, namely the self-heating and its consequences towards the length of the DC pulses. Due to the large power densities, the self-heating effects are accentuated with power devices, which results in significant temperature changes inside the component and modify the device parameters. Therefore, temperature is considered as the key factor that influences the power MOSFET static characterization. When MOSFET is in on-state, the junction temperature T_j can be estimated as:

$$T_j = T_a + P \cdot R_{th(j-a)} \quad (3-1)$$

$$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-a)} \quad (3-2)$$

where T_a is the ambient temperature. $R_{th(j-a)}$, $R_{th(j-c)}$ and $R_{th(c-a)}$ are the junction-to-ambient, junction-to-case and case-to-ambient thermal resistances, respectively. P is the power dissipation in the component.

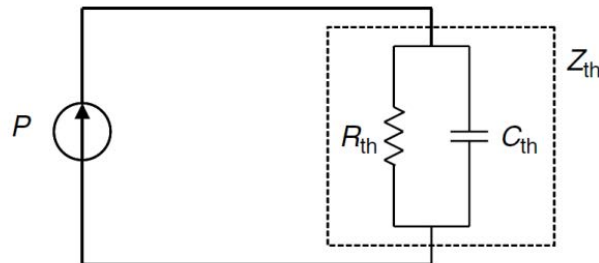


Figure 3.1. Electrical circuit equivalence thermal impedance

The thermal resistance R_{th} is sufficient to describe the relationship between temperature and power dissipated in steady-state conditions. However, in pulse power operation, dynamic behavior of self-heating can be described in terms of thermal capacitance C_{th} , which is usually estimated from the

measured time-dependent response of the junction temperature to the power dissipation. As shown in Figure 3.1, Z_{th} can be represented as a parallel combination of R_{th} and C_{th} in simple electrical circuit equivalence. Such a RC ladder is referred as the Foster network, it is easier to handle for mathematical computation, and nonetheless the Cauer network is more physically meaningful.

The device temperature response can be considered as the voltage increase across a RC circuit with the dissipated power P replacing a current pulse generator, which is expressed, for a P step, as:

$$T(t) = T_a + P \cdot R_{th(j-a)} \cdot \left[1 - \exp\left(-\frac{t_p}{R_{th(j-a)} \cdot C_{th(j-a)}}\right) \right] \quad (3-3)$$

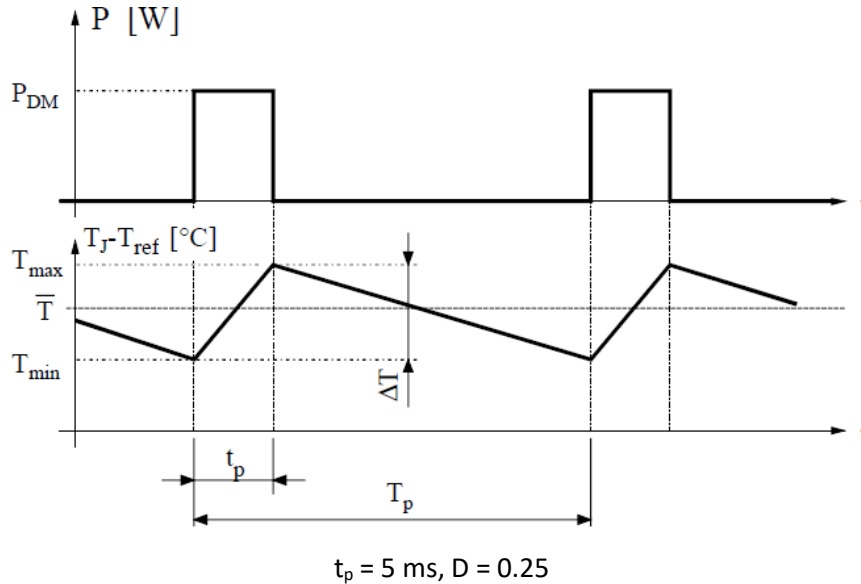
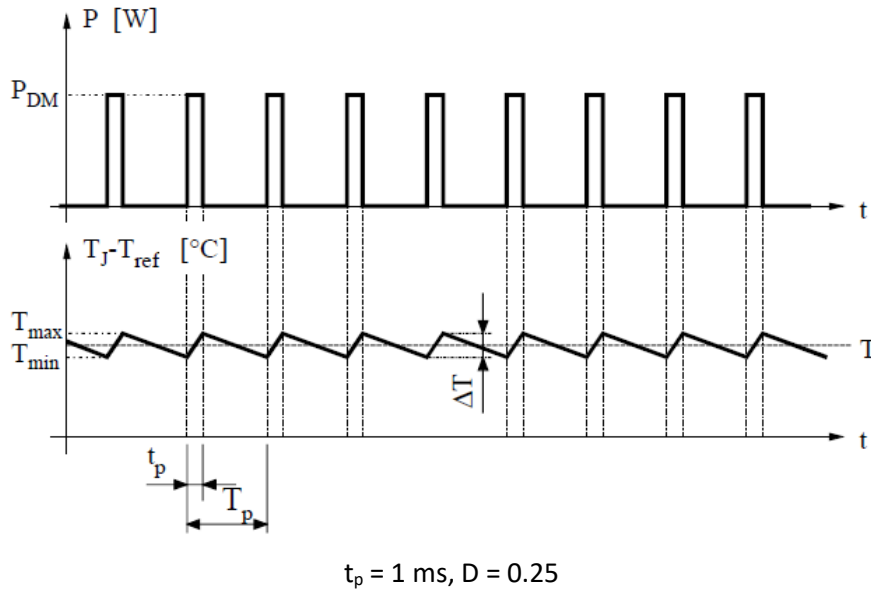


Figure 3.2. Device temperature T_j vs. time for periodic pulse operation

In the pulse operation, the device temperature responses are presented qualitatively in Figure 3.2. The T_j varies between T_{min} and T_{max} depending on the magnitude of the pulse power, the pulse duration (t_p) and duty cycle (D). Characterization tests are usually performed by means of the double

pulse method, during which the DUT may be prone to self-heating. To be free from the temperature dependence, the pulse should be as short as possible.

In the datasheets, the thermal impedance Z_{th} of a MOSFET is usually provided by means of a diagram as shown in Figure 3.3. It describes the relation between the junction-case thermal impedance $Z_{th(j-c)}$ and the pulsed duration (t_p) for different duty cycles. When the t_p is longer than 1 s, $Z_{th(j-c)}$ is nearly constant at any duty cycle value, about 0.25 K/W in the case of SiC MOSFET CAS100H12AM1. Particularly, at single pulse condition (t_p much smaller than T), when the t_p is shortened to 100 μ s, $Z_{th(j-c)}$ is about 0.0015 K/W. Under such conditions, the characterization can be carried out with a hundred times higher power dissipation than at continuous state. Hence, the commercial curve tracer is based on this principle to characterize the power devices.

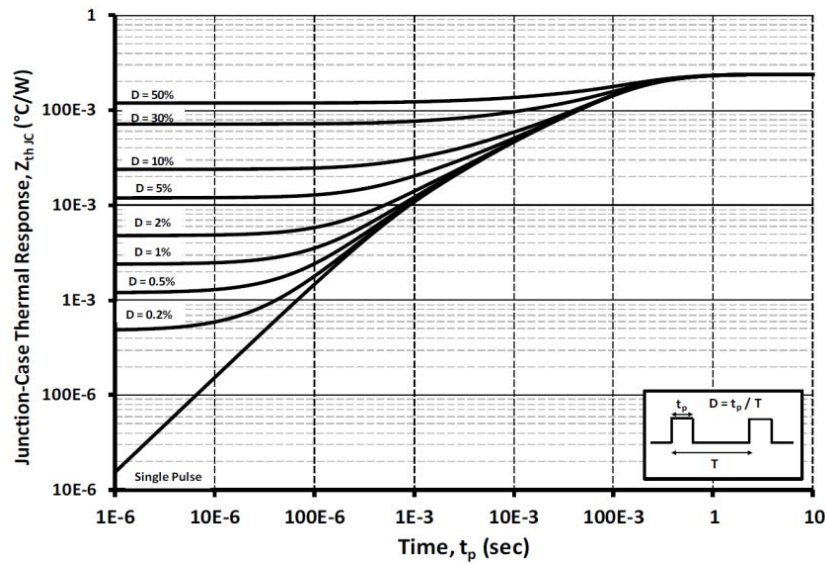


Figure 3.3. Transient thermal impedance of the SiC MOSFET CAS100H12AM1 (from datasheet)

When the transistor is characterized, power is continuously dissipated in the junction and the DUT is prone to self-heating. In this work, therefore, the drain current is measured using pulsed voltages as bias condition instead of static values. Since the thermal effects are delayed processes (lagging offset in respect to electrical stimuli) with specific time constants, drain current is in fact measured using pulse duration significantly smaller than the time constants of thermal effects. The pulse repetition time is much larger than the pulse width, i.e. the duty cycle is low, the heat produced by the current on each pulse cannot add up effectively to the next pulse.

3.2. Threshold voltage V_{TH}

The threshold voltage V_{TH} is an important scaling factor in circuit design for determining the on-state and the off-state of the MOSFET. For most applications, V_{TH} is expected high enough (above 1 V) to avoid unintended turn-on due to voltage spikes arising from noise. At the same time, the desired value of V_{TH} is about 3 V for the small channel resistance [48]. From a physical point of view, the V_{TH} is the minimum gate bias required for the formation of the channel in P-body to connect the source and drain terminals. The value of V_{TH} is calculated by equation (2-10) which requires many factors including oxide layer thickness, substrate doping, etc.

In practice, V_{TH} can be defined by measurement in many ways which are explained elsewhere in more detail [129]. Most often, manufacturers indicate a V_{GS} obtained by means of a constant current

method (CCM). Defined by this manner, V_{TH} is defined as soon as drain current I_D reaches a specific value (typically tens of mA), gate and drain being short-circuited ($V_{DS} = V_{GS}$) to ensure a full saturation regime. Value of V_{TH} measured in this way is often lower than this from the transfer curves estimation.

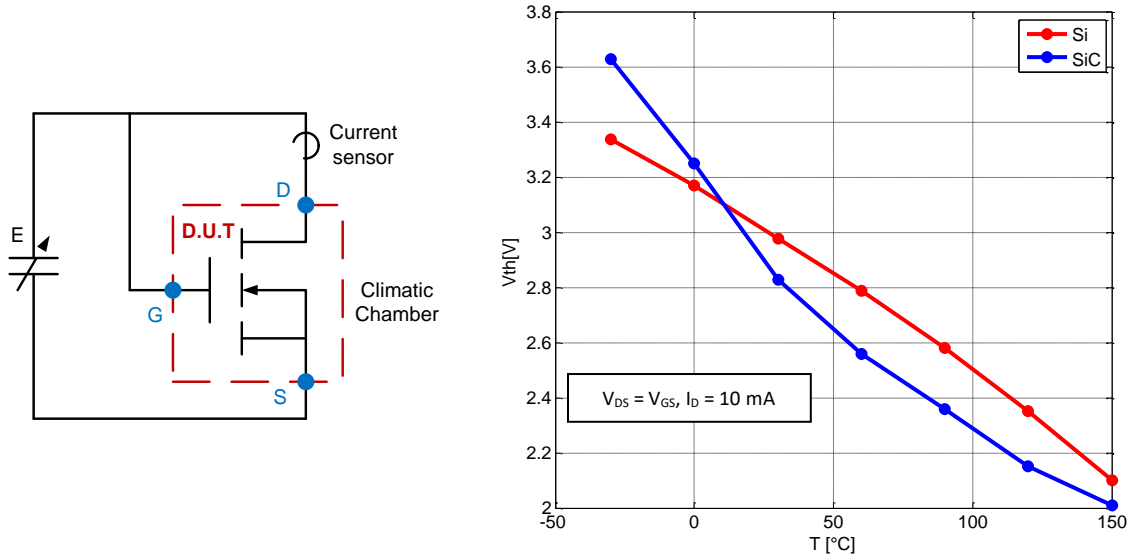


Figure 3.4. V_{TH} measurement circuit and results obtained

Figure 3.4 presents the experimental setup used for V_{TH} characterization, and experimental results obtained for a Si MOSFET (SKM253B020) and a SiC MOSFET (CAS100H12AM1). The test bench is based on the constant current method, with a value of 10 mA and 50 mA for the calibration drain current, which enables to avoid any risk of MOSFET self-heating during the test. The voltage source E is a programmable power supply HAMEG HM7044, whose output voltage is continuously variable between 0 - 32 V. A climatic chamber (Binder MK240) enables to carry out V_{TH} measurement at different temperatures. The DUT is kept in the climatic chamber for 12 hours to allow the temperature stabilization at each step of 30°C from - 30 °C to 150 °C. It is assumed that the junction temperature is equal to the ambient temperature in chamber.

Both Si MOSFET and SiC MOSFET V_{TH} have a negative temperature coefficient, meaning that V_{TH} decreases with temperature as shown in Figure 3.4. It is found that the fast reduction in SiC MOSFET V_{TH} with temperature (about - 9 mV.K⁻¹) is due to interface traps, which would be a challenge for the usage of SiC MOSFET in high temperature applications. Low V_{TH} causes the uncontrolled MOSFET turn-on when using an off-state gate voltage of zero volt. This situation could get more critical at high temperatures. Consequently, appropriate negative gate bias for high temperature applications should be taken into account to have reliable turn-off even in noisy environments.

The V_{TH} temperature behavior of Si MOSFET is quite linear, and so a proportionality coefficient can be used to calculate the junction temperature T_j from the amount of change in V_{TH} . Thus, V_{TH} can be employed as the indirect-measurement method to estimate T_j . However, V_{TH} of SiC MOSFET shows non-linear behavior with temperature. This means that SiC MOSFET V_{TH} cannot be used easily as a temperature indicator.

3.3. Output characteristics

3.3.1. Test bench

The output characterization consists in measuring I_D as the function of V_{DS} for different values of V_{GS} . To characterize a power MOSFET, the single-pulse method is applied, the principle is illustrated in Figure 3.5. It consists of a chopper converter loaded by the DUT and driven by short and low frequency pulses applied to the gate of a power pilot transistor M1. The DC link capacitance C_{bus} , composed of 10 capacitors (33000 μ F, $U_R = 63$ V) in parallel, is sized high enough to maintain a quite constant DC link voltage during the test, and to enable the use of a small power supply (such as the HAMEG HM7044, limited to 32 V and 3 A). A braking resistor R , manually connected to the DC bus, is used to discharge C_{bus} . An inductor L , in series with the DUT, enables to control the slope of the current flowing through the DUT at M1 turn-on. Inductance discharge at M1 turn-off is ensured by means of a freewheeling diode D . A trade-off must be found for L value. In effect, a small value for L is convenient to reduce turn-on duration and then avoid any DUT self-heating, but it may also induce too high di/dt , and then disturbances on the voltage measurement. On the other hand, a high inductance value facilitates voltage measurement, but requires long turn-on duration, which can lead to unacceptable self-heating.

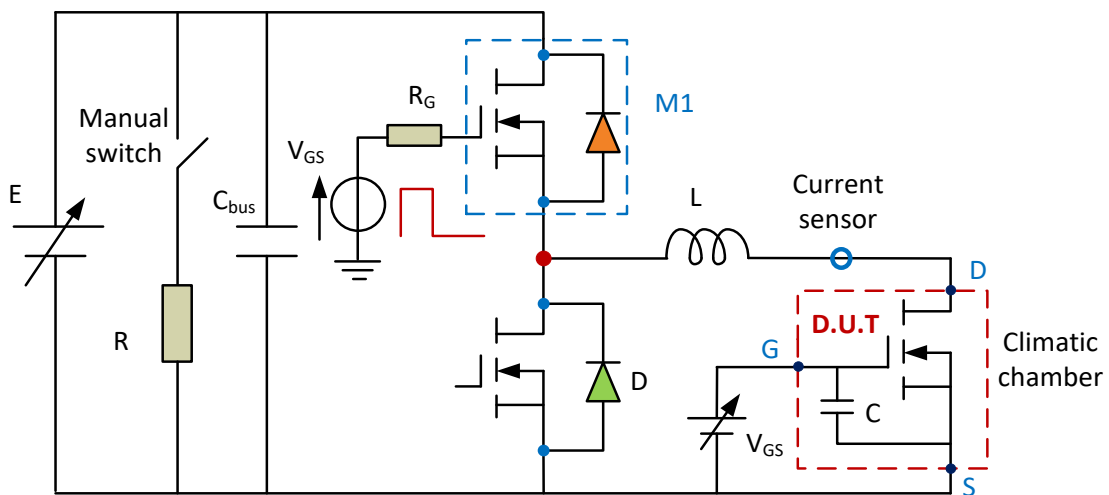


Figure 3.5. Schematic of output characterization test bench

Its gate is biased with a constant voltage above the V_{TH} (from 6 to 20 V with the step of 2 V). A tentacle capacitor C is closely inserted between the gate and the source of the DUT to maintain the gate voltage constant during transient. The power MOSFET M1 is controlled by means of a pulse signal, generated by means of function generator Tektronix AFG3021B. The DUT is soaked for 12 hours in the climatic chamber to allow the temperature stabilization at each temperature. All these characterizations have been performed under different temperatures from -30° to 150° C.

3.3.2. Principles of measurement

When M1 is switched on during t_p , the load composed of the DUT in series with the inductor L is subjected to the DC bus voltage E . Current from the bus capacitor C_{bus} increases through the DUT, with a slope that can be adjusted by means of L and E values. It reaches a maximum level I_{max} , which is determined whether by power pulse duration t_p , or by the DUT gate voltage. As previously mentioned, pulse duration must be short enough to avoid any significant self-heating of the DUT, but

also long enough to obtain whether high current level (at least the DUT rated current) or saturation regime.

When M1 is turned off, a freewheeling phase occurs through the diode D, which ensures the continuity of the current. Both drain current I_D and voltage V_{DS} decrease down to zero. This phase can be used, by comparing the curve $V_{DS}(I_D)$ with the one obtained during turn-on, to verify that no significant self-heating has occurred.

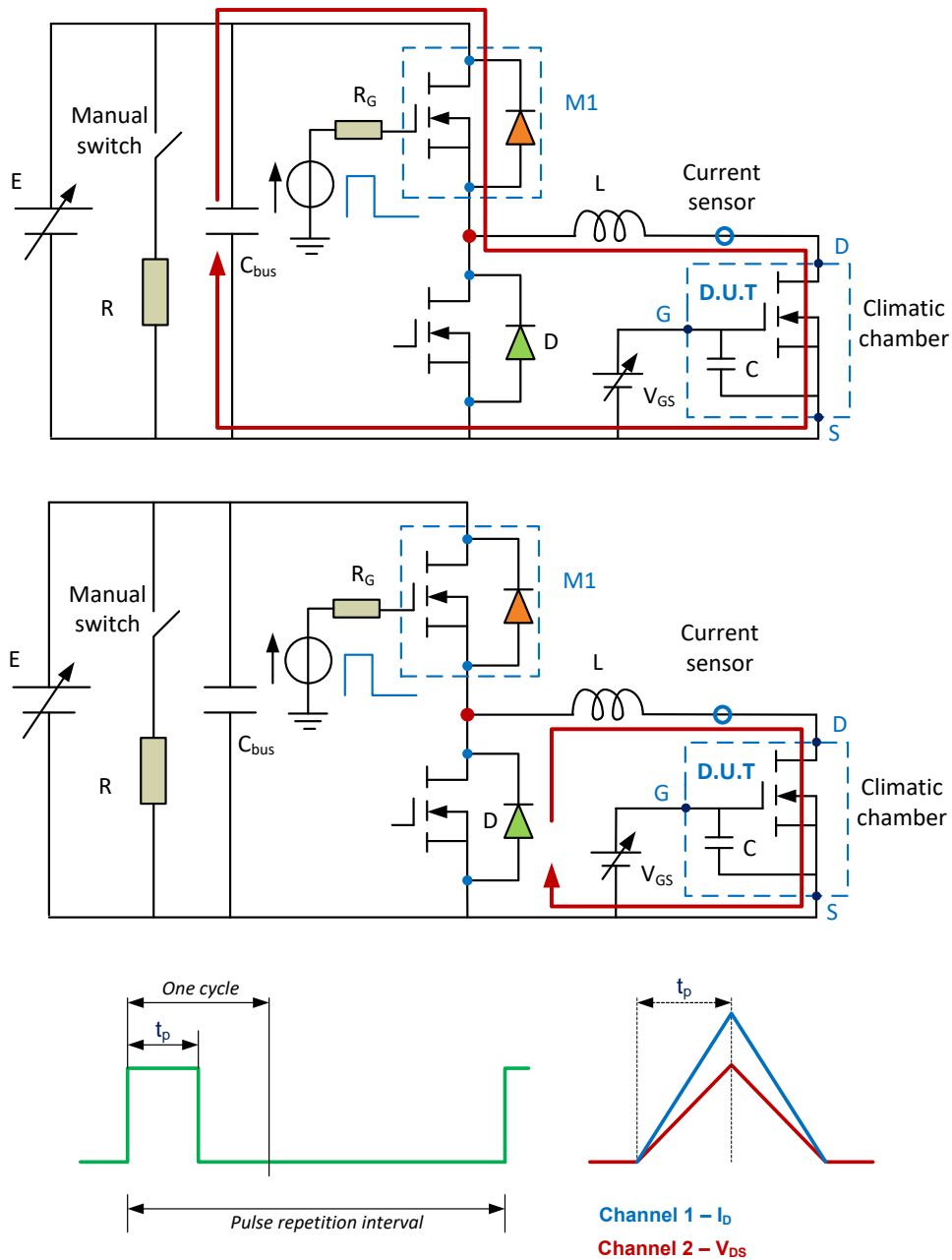


Figure 3.6. Operation of circuit and waveforms

At last, the characterization process can of course be conducted with a single pulse, but one can take advantage of repetitive pulses to decrease noise level by averaging data. In this case, the pulse repetition interval must be of several seconds, to avoid cumulating self-heating effects, which would

lead to a slow drift of the DUT temperature. Figure 3.6 summarizes the characterization principle, it depicts its two phases (M1 conduction during t_p , and D conduction during freewheeling phase), and presents current I_D and voltage V_{DS} ideal waveforms.

3.3.3. Results and discussions

Output characteristics are only observed in ohmic regime. Indeed, the experimental setup does not allow reaching properly saturation regime, because of disturbances and ripples which appear on current. We have chosen $t_p = 500 \mu s$, which theoretically limits, according to the thermal impedance curve given in Figure 3.3, the DUT self-warming to about $2^\circ C$ in the worst case (SiC MOSFET CAS100H12AM1, about 200 A for I_D and 4 V for V_{DS} obtained at $V_{GS} = 20 V$ and $T_j = 30^\circ C$). The pulse repetition interval is set to 10 s. Measurements are carried out with an oscilloscope TDS5034B, a current probe TCP303 (150 A - 15 MHz) coupled with an amplifier TCPA300 (bandwidth: 100 MHz). Voltage is directly measured.

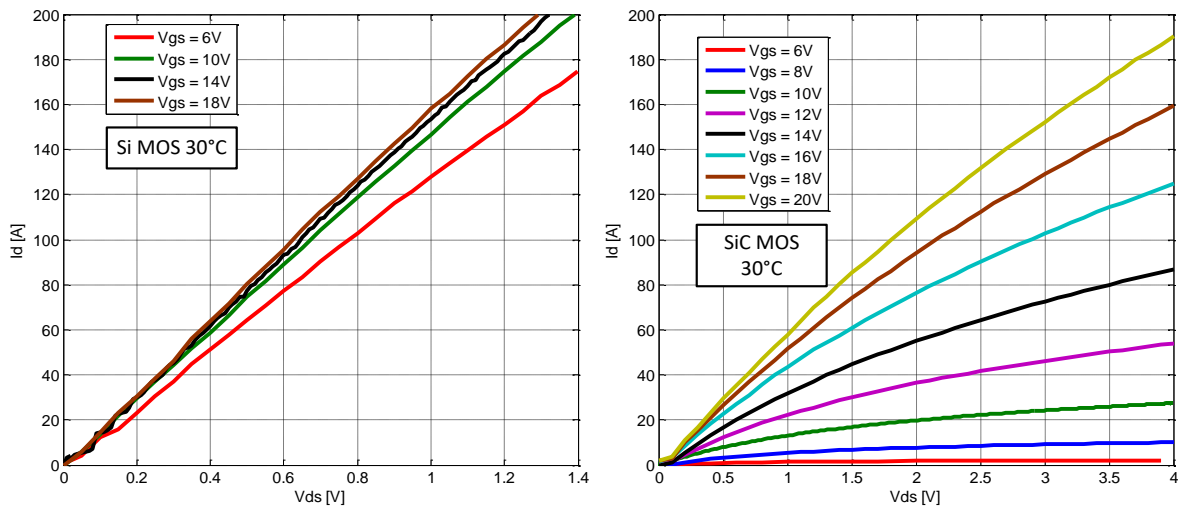


Figure 3.7. Output characteristics of MOSFETs at $30^\circ C$. On left: 200 V-250 A Si MOSFET (SKM253B020), on right 1200 V-100 A SiC MOSFET (CAS100H12AM1)

Figure 3.7 presents output characteristics obtained with a Si MOSFET (SKM253B020, ratings: 200 V-250 A) and a SiC MOSFET (CAS100H12AM1, ratings: 1200 V-100 A), at different gate voltages. As expected, MOSFETs operate in both cases as resistive elements. Since R_{CH} is inversely proportional to the V_{GS} as equation (2-36), slopes increase with V_{GS} increasing. It can be observed that the output characteristics of Si MOSFET are very steep and close from each other. This behavior is due to the weak contribution of R_{CH} within Si MOSFET on-resistance $R_{DS(ON)}$, which is typically dominated by the drift resistance R_{DRIFT} . Contrary to this tendency, SiC MOSFET curves have a large variation with V_{GS} , which results from a significant portion of R_{CH} within SiC MOSFET $R_{DS(ON)}$. Referring to previous arguments, this is due first to the small value of R_{DRIFT} , second to a relatively high R_{CH} because of the poor mobility in the SiC MOSFET inversion channel. For this reason, SiC MOSFETs are normally driven at a higher gate voltage than Si counterparts, typically 18 V to 20 V, to minimize $R_{DS(ON)}$.

Another difference between Si and SiC MOSFETs is the electro-thermal behavior in on-state regime. In Figure 3.8, output characteristics are plotted for two temperatures. Dotted curves and line curves refer to tests proceeded at $30^\circ C$ and $150^\circ C$, respectively. In the case of Si MOSFET, drain current

obviously decreases with temperature whatever the gate bias is, meaning that $R_{DS(ON)}$ is an increasing function of temperature. A well-known and beneficial consequence of this positive electro-thermal behavior is thermal stability in parallel operation. Conversely, the electro-thermal behavior of SiC MOSFET is highly dependent on the gate voltage.

At high gate voltage, for example at 20V, the current decreases with temperature. However, SiC MOSFET exhibits a negative temperature coefficient, at low gate voltage, 12 V for instance, which is known to be a disadvantage in system design aspects. The unique characteristics need to be kept in mind when considering current sharing and thermal stability. Hence, SiC MOSFETs require a gate voltage as high as 18 V to reduce on-state resistance and avoid thermal runaway.

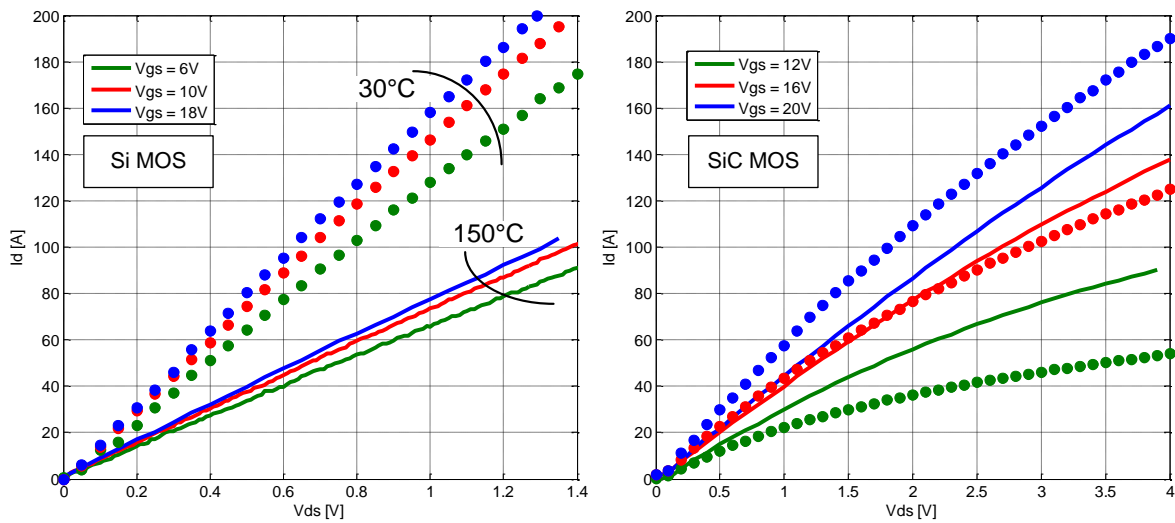


Figure 3.8. Output characteristics of MOSFETs at 30 °C (dotted lines) and 150 °C (solid lines) On left: 200 V-250 A Si MOSFET (SKM253B020), on right 1200 V-100 A SiC MOSFET (CAS100H12AM1)

The output characteristics of SiC MOSFET were also observed in Figure 3.9 for the same gate bias voltage, here 20 V, at different temperatures. For junction temperatures greater than 60 °C (curves on the right), an increase in on-resistance can be observed, but for lower junction temperatures (curves on the left), the tendency is clearly opposite. In other words, even under high gate voltage conditions, the electro-thermal behavior of SiC MOSFET can be negative. This unique I-V characteristics of SiC MOSFET versus temperature can be explained by the high contribution of R_{CH} in the total on-resistance $R_{DS(ON)}$. As aforementioned, the V_{TH} reduces with temperature. As a result, R_{CH} is a decreasing function of temperature, contrary to other resistances (R_{JFET} , R_{DRIFT}) that compose $R_{DS(ON)}$. Consequently, R_{CH} dominates at low junction temperature and dictates the on-state electro-thermal behavior, leading to the reduction of $R_{DS(ON)}$, up to 60 °C for the tested component. However, at higher temperatures, the increase of other resistances is faster than the reduction of R_{CH} , resulting in a slight increase of $R_{DS(ON)}$.

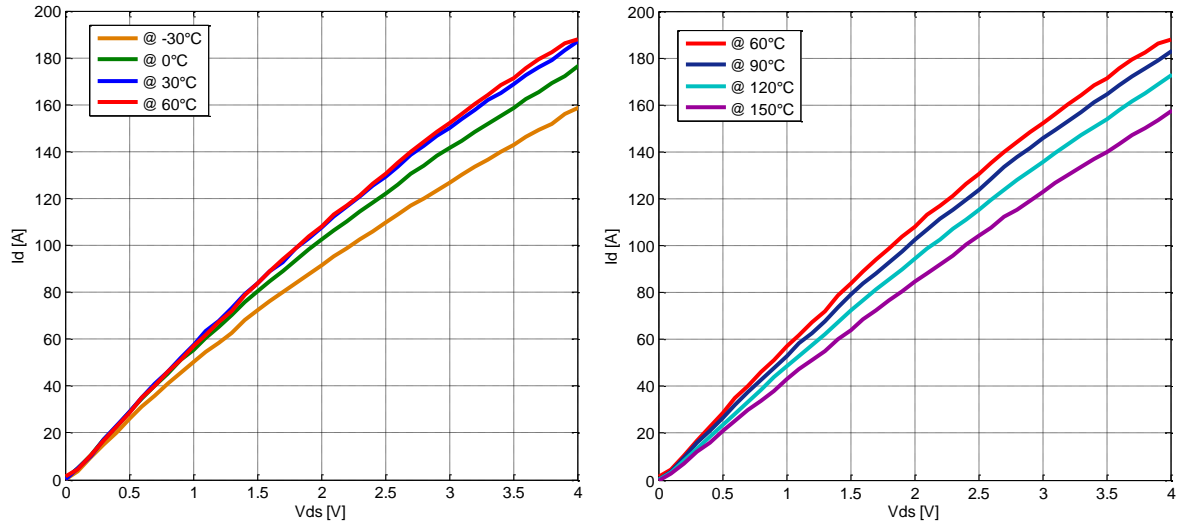


Figure 3.9. SiC MOSFET (CAS100H12AM1) output characteristics for different junction temperatures at $V_{GS} = 20$ V

With SiC MOSFET, the transition of drain current from ohmic to saturation region is not clearly observed. Let assume $V_{TH} = 3$ V and $V_{GS} = 10$ V, then the device should enter the saturation mode as soon as $V_{DS} > V_{GS} - V_{TH} = 7$ V. However, when considering Figure 3.10, it clearly appears that the saturation area is not that flat for $V_{DS} > 7$ V, I_D keeps on rising with drain-source voltage. In other words, the SiC MOSFET behaves more like a voltage-controlled resistor than a voltage controlled current source.

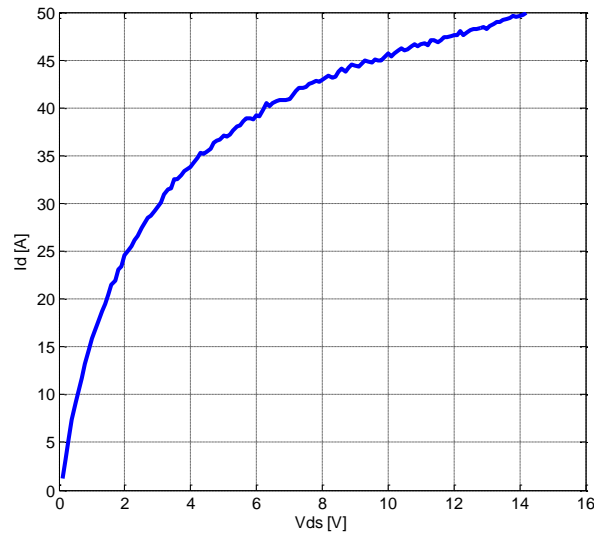


Figure 3.10. Output characteristics of SiC MOSFET (CAS100H12AM1) at $V_{GS} = 10$ V and $T_j = 60$ °C

3.4. Transfer characteristics

3.4.1. Test bench

As shown in Figure 3.11, two sources are required for measuring the transfer characteristics: one feeds the gate, and the second biases the drain-source terminals. This test approximates the device behavior in saturation regime. Therefore, it has to apply a voltage between drain and source sufficiently large to ensure that the MOSFET works correctly in desired region. Here, we applied

$V_{DS} = 20$ V. The voltage source E is provided by a power supply HM 7044. A braking resistor R is used to discharge the DC bus capacitor, using a manual switch. A function generator Tektronix AFG3021B is used to drive the gate of the DUT. As previously, a large capacitance ($C_{bus}=330$ mF), composed of 10 capacitors in parallel, is used to maintain a constant voltage V_{DS} during the test.

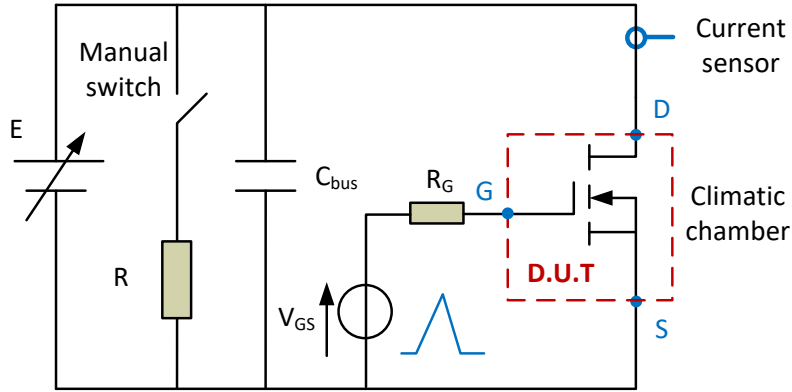


Figure 3.11. Schematic of the transfer characterization test bench

As shown in Figure 3.12, the function generator is set to supply triangle pulses. Rise time and fall time were set at $400 \mu s$ (to avoid significant self-heating), and the interval between pulses was 10 s. As the voltage range of the generator was ± 10 V, a 10 V battery was added in series within the gate circuit, in order to cover a gate bias range of 0 - 20 V.

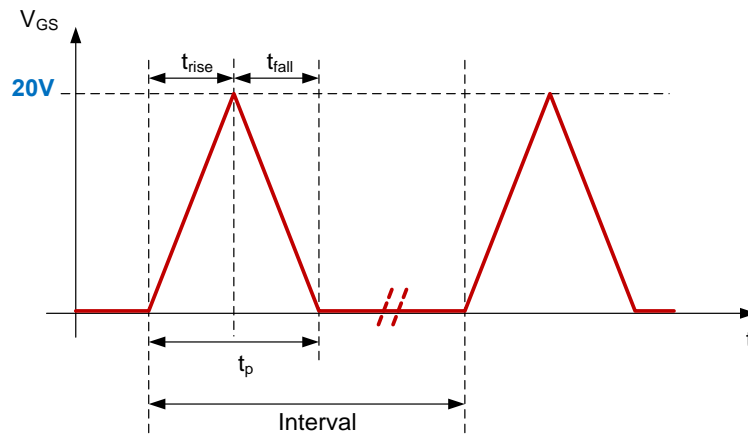


Figure 3.12. Gate bias V_{GS} waveform

Drain current is measured by means of a current probe TCP303 associated with an amplifier TPCA300, and recorded by an oscilloscope TDS5034B. As previously, the DUT is kept in the climatic chamber, to survey the temperature effect on the current handling capability.

3.4.2. Principle of measurement

The transfer measurement of a MOSFET is similar to short-circuit test which is studied at the desired DC link voltage ($V_{DS} = 20$ V). Within the duration t_p , the device is switched-on during the rise time. As soon as the gate bias reaches V_{TH} , the current from the C_{bus} flows to the device. The I_D rise is controlled by the device characteristics (internal gate resistance R_{Gin} , V_{TH} , g_m), external gate resistance R_G of the function generator and the stray inductance that exists in the circuit. During the fall time, I_D goes down to zero in the reverse manner.

As previously mentioned, the duration of conduction t_p is set up long enough to avoid the ripples on the power after the power control interaction. In the same time, the t_p needs to be fast enough to prevent power dissipation.

3.4.3. Results and discussions

Both Si and SiC MOSFET transfer curves are shown in Figure 3.13, where I_D is a function of the V_{GS} at certain V_{DS} and fixed junction temperature. For the Si MOSFET case, the current through the device is kept at zero until the gate bias reaches V_{TH} . In theory, almost all of carriers induced by V_{GS} are free to conduct the current; the channel turns on very quickly as soon as $V_{GS} > V_{TH}$. Thus, Si MOSFET transfer characteristics are the family of curves with high slope.

In comparison, the SiC MOSFET displays a smoother slope, this is due to the poor interface quality in the channel regions [20, 94]. At low positive gate voltage, induced carriers in the inversion layer are not free because many of them are trapped in the interface states. When the gate voltage is increased, all the trap states are filled. Consequently, additional charge can move freely in conduction band, leading to a gradual increasing of the current.

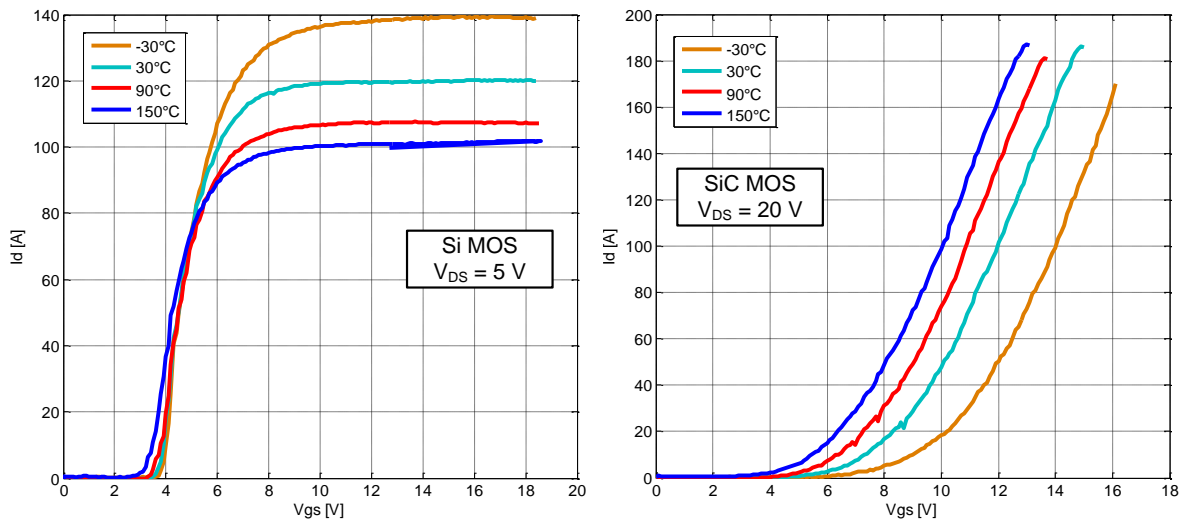


Figure 3.13. MOSFET transfer characteristics for different temperatures. On left: 200 V-250 A Si MOSFET (SKM253B020), on right 1200 V-100 A SiC MOSFET (CAS100H12AM1)

Based on these curves, the dependency towards temperature should also be addressed. Si MOSFET curves show the three possible regimes for such a power electronics switch: off, saturated, ohmic. In saturation mode (for V_{GS} between V_{TH} and a little more than 5 V), it clearly appears that current increases with temperature, as a consequence of the opposite trend for threshold voltage. As soon as the Si MOSFET enters the ohmic mode, it is obvious that current decreases with temperature, because of the positive temperature coefficient of $R_{DS(ON)}$. These quite usual results for Si MOSFET can hardly be applied to distinguish saturation mode and ohmic mode through SiC MOSFET transfer characteristics of Figure 3.13; indeed the currents always exhibit an increase versus temperature.

Traditionally, the device transconductance g_m is determined in saturation region, where the device acts as a current source. Si power MOSFET generally saturates at reasonably low values of V_{GS} and V_{DS} , and as illustrated in Figure 3.14, its transfer characteristic has a steep slope which enables to determine easily g_m and V_{TH} , by means of a line tangent to the transfer curve. For example, a linear

extrapolation of V_{TH} from SKM253B020 transfer curve indicates that V_{TH} of this power device is about 3.8 V at 30 °C, providing a satisfying fit to the experimental data [129, 130].

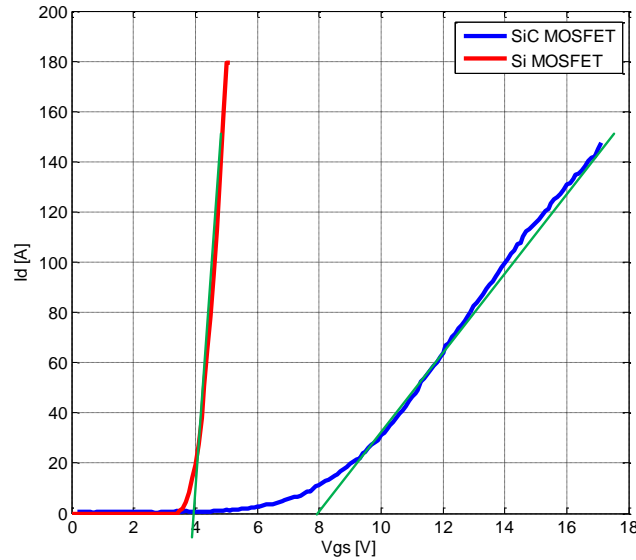


Figure 3.14. Transfer characteristics of Si (SKM253B020) and SiC (CAS100H12AM1) MOSFETs at $V_{DS} = 10$ V and $T_J = 30$ °C

In saturation, the current is independent to drain voltage. However, the SiC MOSFET channel hardly attains current saturation at $V_{DS} = 20$ V since the current still changes with V_{DS} . Therefore, the MOSFET still behaves as a voltage-controlled resistor. The current increases with the temperature as seen in Figure 3.13 because of the R_{CH} which has a negative temperature coefficient. Furthermore, the transfer characteristic of SiC MOSFET is fairly smooth, as a result of interface traps at the SiC-SiO₂. Hence, value of g_m reported in the datasheet in near saturation regions ($V_{DS} = 10$ V or 20 V) is not much meaningful. So that following the same computation of V_{TH} as previously for Si component (see Figure 3.14), the SiC MOSFET would exhibit a threshold voltage of 8 V at 30 °C, which is quite far from the nominal value mentioned on the datasheet, namely 3.1 V.

3.5. Zero-amp on-resistance

In the context of a switch, when the power MOSFET is completely switched-on, it behaves like a resistor. So, the total drain-to-source resistance in its fully conducting state, abbreviated as $R_{DS(ON)}$ is the key parameter for determining the conduction loss and the current sharing between the paralleled MOSFETs. Since $R_{DS(ON)}$ is a temperature-dependent parameter, it can be used as a temperature sensitive electrical parameter (TSEP) to identify the junction temperature of device and is therefore of special interest [131, 132].

In the ohmic region, $R_{DS(ON)}$ is defined as the inverse of the slope of the output characteristic curve. In this situation of Si MOSFET, the output curves are linear, as seen in Figure 3.15. Therefore, $R_{DS(ON)}$ does stay constant across the whole V_{DS} range. In case of SiC MOSFET, with a large discrepancy between the curves with different amplitudes of gate bias, the slope is much steeper and linear near the origin. Hence, the value of the $R_{DS(ON)}$ strongly depends on the static bias points. For example, drawn from Figure 3.15, drain voltage of SiC MOSFET CAS100H12AM1 at $(V_{GS}, T_J, I_D) = (12$ V, 30 °C, 20 A) is about 0.8 V. For the double current, i.e. $I_D = 40$ A, drain voltage is about three times higher, so much more than the double. Thus, for a given gate voltage, $R_{DS(ON)}$ is defined as the slope of the

output characteristic at specified drain voltage (or specified drain current). Moreover, TSEP method based using $R_{DS(ON)}$ is often performed at small current ranges. For that reason, $R_{DS(ON)}$ in most commercialized MOSFET datasheets with the typical and maximal value at specific turn-on gate voltage and high drain current is not satisfied.

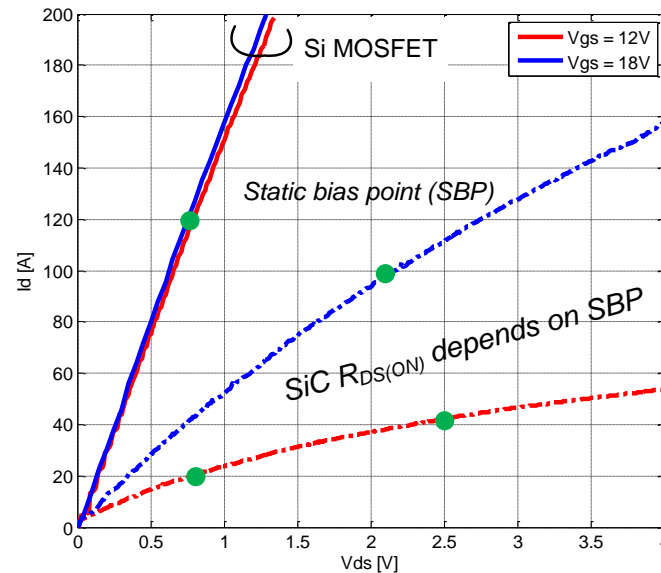


Figure 3.15. $R_{DS(ON)}$ and static bias points at 30°C. Solid lines: 200 V-250 A Si MOSFET (SKM253B020), dashed lines: 1200 V-100 A SiC MOSFET (CAS100H12AM1)

3.5.1. Measurement methods

The traditional method to characterize on-resistance is the pulse I-V step measurement, which is shown in Figure 3.16. This technique requires specific equipment, notably a powerful voltage source to provide high current under the required V_{DS} . Moreover, the SiC MOSFET exhibits a very small $R_{DS(ON)}$ (from few milliohms to tens of milliohms), consequently a very sensitive sensor is mandatory to monitor V_{DS} .

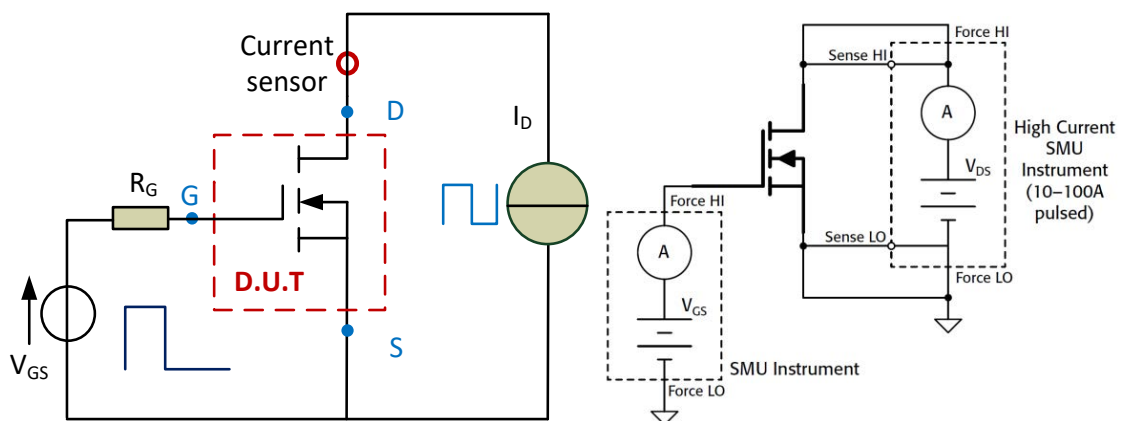


Figure 3.16. Pulse method to measure on-state resistance

As illustrated in Figure 3.16, the on-resistance survey is often carried out by means of two source measure units (SMU), which integrate a highly stable DC power source with high precision multimeter. The gate MOSFET is driven by a SMU, another high current SMU generates a pulsed current I_D and measures the resulting voltage V_{DS} . The pulsed test method is often coordinated by a

computer program. Since the $R_{DS(ON)}$ is strongly affected by temperature, it is important to minimize the device self-heating during the test. Therefore, the length of the pulse test must be carefully calibrated. The pulse method is a dynamic method; it requires quite high bandwidth sensors and may lead to measurement uncertainties due to parasitic inductances and capacitances.

We propose hereafter another way to reach steady state a specific value for $R_{DS(ON)}$: the zero-amp on-resistance, $R_{DS(ON)}(0)$, i.e. the reciprocal slope at the origin of the output characteristic. For this purpose, we made use of the impedance spectroscopy technique which is based on the linear interdependence between AC sinusoidal current excitation and voltage response.

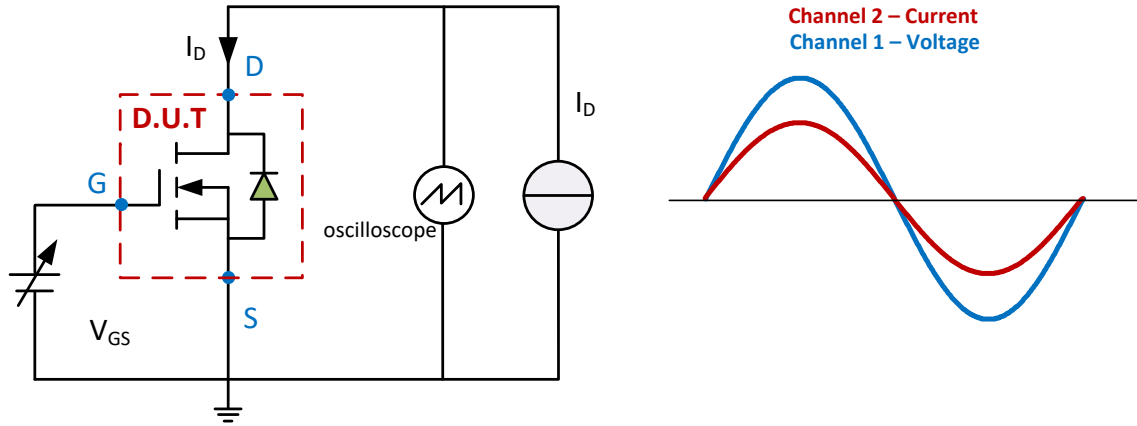


Figure 3.17. Method to measure zero-amp on-state resistance

As depicted in Figure 3.17, the AC sinusoidal current excitation is applied through the component; in return, an AC sinusoidal voltage is induced between drain and source at the same frequency (ω) with a null phase (φ) with respect to the excitation. Hence, the impedance of the device is equal to its resistance which was defined according to the Ohm law.

$$\bar{Z} = \frac{V}{I} \cdot \exp(j \cdot \varphi) = \frac{V}{I} = R \quad (3-4)$$

Even if a resistance measurement does not depend on the frequency, the excitation frequency is chosen appropriately to prevent thermal transfer dynamics and disturbing inductive response. By keeping the amplitude of $V_{DS}(t)$ small enough, some tens of millivolts, power dissipation within the component can be controlled and held to weak levels. The tests were performed at different temperatures from - 30 °C to 150 °C with a 10 °C step, and at various gate bias voltages from 6 V to 20 V.

3.5.2. Test bench

In our work, the zero-amp on-resistance is measured regarding two parameters, namely the gate voltage and the temperature. The DUT is soaked in the climatic chamber. The gate of the DUT is fed by a voltage source HM7044. A bidirectional NL1V8C80 source-sink (voltage range: - 1 V to 8 V, current range: ± 80 A) operates in controlled current mode to supply drain and source terminals. In the selected operating mode, the output current is driven by an external AC sinusoidal signal (supplied by a function generator AFG3021B), whose amplitude is adjusted in order to keep the amplitude of V_{DS} under 100 mV. Tests are performed at 100 Hz. Current and voltage measurements

are carried out on an oscilloscope TDS5034B, by means of a current probe TCP0030A (30 A, 120 MHz) associated with an amplifier T CPA300, and a voltage probe ADA400 (bandwidth: 1 MHz).

Drain voltage amplitude is kept small, first to prevent from the effect of V_{DS} on threshold voltage and mobility. Second, it enables to limit drastically losses within the component far below its power dissipation capability, and then to avoid any significant self-heating which would leads to measurement inaccuracies. For example, the lowest value for on-resistance of the SiC MOSFET CAS100H12AM1 is about 16 m Ω (obtained at $V_{GS} = 20$ V and $T_j = 25$ °C, see Figure 3.19), so that keeping V_{DS} amplitude under 100 mV leads to losses lower than 0.3 W.

3.5.3. Results and discussions

Figure 3.18 presents the variation of $R_{DS(ON)}(0)$ versus gate bias, obtained at different temperatures with a Si MOSFET (SKM253B020, ratings: 200 V-250 A) and a SiC MOSFET (CAS100H12AM1, ratings: 1200 V-100 A).

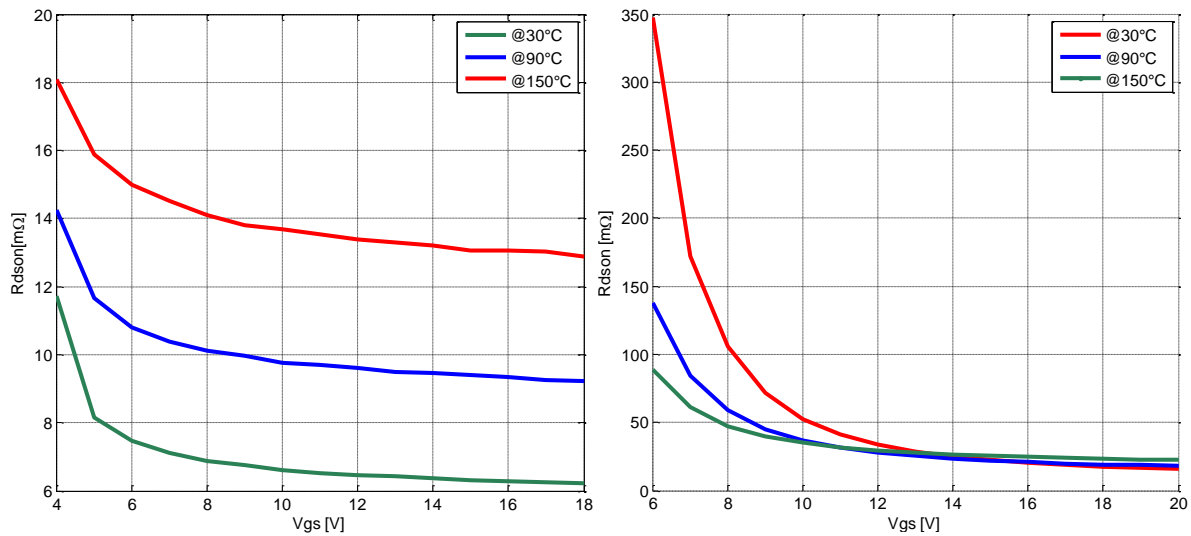


Figure 3.18. Zero-amp on-resistance vs V_{GS} . On left: 200 V-250 A Si MOSFET (SKM253B020), on right 1200 V-100 A SiC MOSFET (CAS100H12AM1)

Since the channel resistance R_{CH} has a nearly reciprocal dependence versus gate bias voltage, it is obvious that $R_{DS(ON)}(0)$ decreases with V_{GS} in both cases. But what can be observed is that this variation is far more important for SiC MOSFET than for Si MOSFET. The root causes of this matter of fact is first the important proportion taken by both drift and JFET resistances in $R_{DS(ON)}$ for Si MOSFET, whereas a SiC MOSFET is structured with a much thinner and much highly doped N-drift region that reduces the importance of R_{DRIFT} in the overall on-resistance. Secondly, it appears clearly that the contribution of R_{CH} within on-resistance is not only higher for SiC MOSFET, it is the highest. Conductivity of inversion channel is determined by two factors: the concentration of free carriers available to conduct current, and carrier mobility. With an extremely high density of interface traps (D_{it}), spatially located at or near the SiO_2 -SiC interface and energetically located near the conduction band-edge of 4H-SiC, electron mobility and free carrier density have been found to be smaller than for Si MOSFET [62, 133]. As a result, SiC MOSFET is limited by channel resistance for the 900 V to 1700 V ratings.

In system design aspects, the resistance temperature coefficient needs to be kept in mind when considering current sharing and lateral thermal stability. To this point of view, Figure 3.19 points out another major difference between Si and SiC MOSFETs. On-resistance of Si MOSFET is dominated by R_{DRIFT} and R_{JFET} , whose temperature coefficients are positive. Hence Si MOSFET $R_{\text{DS(ON)}}$ increases with temperature at any gate bias. Conversely, the behavior of SiC MOSFET $R_{\text{DS(ON)}}$ is rather complex because of the weight of R_{CH} , which varies with temperature according to either a decreasing function, or a non-monotonic function, depending on the gate voltage. This phenomenon also appear in Figure 3.18, the green curve is the lowest one for $V_{\text{GS}} < 14$ V and is the highest one for $V_{\text{GS}} > 14$ V.

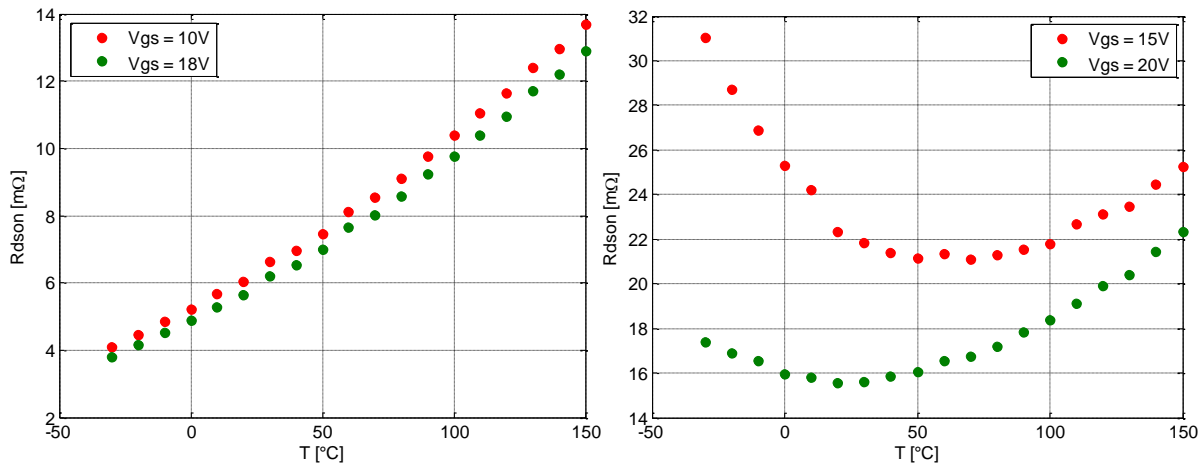


Figure 3.19. Zero-amp on-resistance versus temperature at low gate bias. On left: 200 V-250 A Si MOSFET (SKM253B020), on right 1200 V-100 A SiC MOSFET (CAS100H12AM1)

Thus, at low gate bias, as depicted in Figure 3.20, channel resistance, and consequently zero-amp on-resistance, dramatically decrease with temperature, because of the reduction in V_{TH} on one hand, of the channel mobility enhancement on the other hand. Indeed, it is widely accepted that electrons trapped in interface states are emitted into the conduction band with increasing temperature. Thus, more free carriers available in the MOS channel can contribute to the current conduction. Due to the dominant of Coulomb scattering at low gate bias, the channel mobility increases with temperature [133, 134], so leading to further reduction of R_{CH} .

At high gate bias, R_{CH} is still the dominant resistance at low temperatures, resulting in the decreasing of $R_{\text{DS(ON)}}$. However, with further increase in temperature, other scattering mechanisms such as phonon scattering become dominant over Coulomb scattering, resulting in a slight decline of the channel mobility. It partially results in R_{CH} reduction at smaller rates. On the other hand, this trend is mitigated by the increase of others resistances due to the reduction in bulk mobility, resulting finally in an increase of $R_{\text{DS(ON)}}$ at high temperature, as can be observed in Figure 3.19. Thereby, at $V_{\text{GS}} = 20$ V, the total raise of SiC MOSFET on-resistance is about 40 % over the temperature interval [20 °C, 150 °C]. In contrast, The Si MOSFET on-resistance increases by more than 120 % over the same interval.

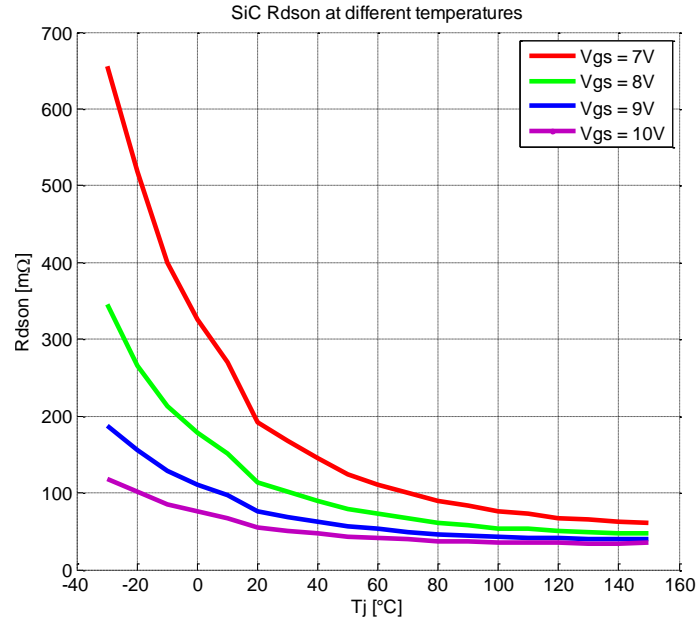


Figure 3.20. SiC MOSFET zero-amp on resistance versus temperature at low gate bias

3.6. Conclusion

The chapter highlights the static characterization of SiC MOSFETs. The SiC MOSFET characteristics are compared to those of Si counterpart, resulting in some recommendations in design.

Using the constant current method, the threshold is measured at defined small value of I_D . A shift of the SiC threshold voltage with temperatures seemingly occurred at higher rate than that of Si MOSFET. Therefore, being a reliability problem, a negative gate-source voltage should be applied in the off-state of the SiC MOSFET to prevent undesired turn-on.

To avoid the self-heating, single-pulsed method is conducted to measure the I-V forward characteristics. The output characteristics and transfer characteristics of SiC MOSFET are family of curves with smooth slope due to the interface traps. A large variation with V_{GS} of SiC MOSFET output curves is due to the domination of R_{CH} within SiC MOSFET on-resistance $R_{DS(ON)}$. Because of high R_{CH} contribution in $R_{DS(ON)}$, the electro-thermal behaviors of SiC MOSFET is far different from those of Si counterparts. Therefore, a higher driving voltage is recommended for the SiC MOSFET to minimize $R_{DS(ON)}$ and avoid the thermal runaway.

In steady state, a specific value for $R_{DS(ON)}$, the zero-amp on-resistance has been investigated by the impedance spectroscopy technique. Not only interesting to compare the losses but also, in certain applications, the zero-amp on-resistance plays a key role in consideration of the electro-thermal behavior of the device. The non-monotonic characteristic with temperature of SiC MOSFET $R_{DS(ON)}$ needs to be kept in mind for thermal management. For using the $R_{DS(ON)}$ as TSEP, an appropriate small gate voltage should be selected for improving the temperature sensitivity.

Chapter 4 SiC MOSFET on-state modeling

4.1. The MOSFET model overview

4.1.1. The MOSFET model classification

Despite the complexity, the existing MOSFET models are sorted:

a. Physical models: Physical models, commonly called as analytical models, are achieved by the analysis of the physical phenomena within a semiconductor device to reflect its characteristics. These models are based on physical laws and interrelationships which are represented by the equivalent mathematic expressions, as shown for example in Figure 4.1 [122, 135, 136].

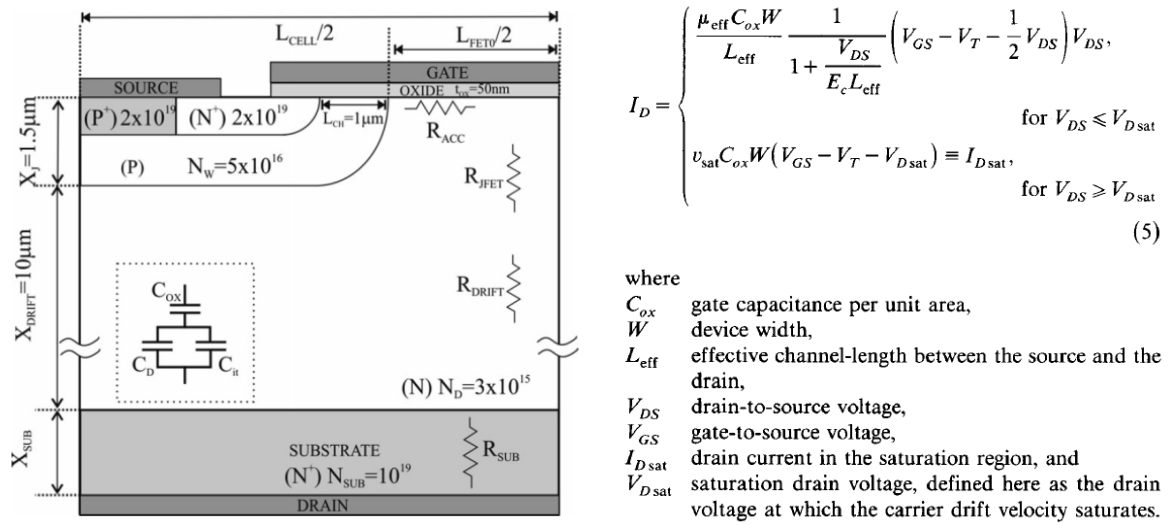


Figure 4.1. Half structure of the reference device and analytical model for short channel MOSFET (after [137-139])

Physical models can well represent the device characteristics with high accuracy over a wide range of operating conditions. Nevertheless, the parameters of the model relate to the device fabrication process such as oxide thicknesses, carrier mobility, etc, which are hardly available for commercial datasheet. Moreover, the designers are also required having an excellent knowledge in semiconductor structures and using analytical method to well implement the model [30, 139]. Thus, physical models are generally too complicated to be developed by users.

b. Behavioral models: By simplifying physical effects inside the component to reproduce the device characteristics, the behavioral models are achieved based on measurements or datasheets. The fitting programs can be used to build models that can be classified in:

- macro models use pre-defined components (controlled sources, resistors, capacitors, etc.) to describe the device behavior, as depicted in Figure 4.2.
- micro models, known as compact models, are based on equations with certain parameters.
- look-up table models, which represent the device behaviors using sampling points within measured data tables.

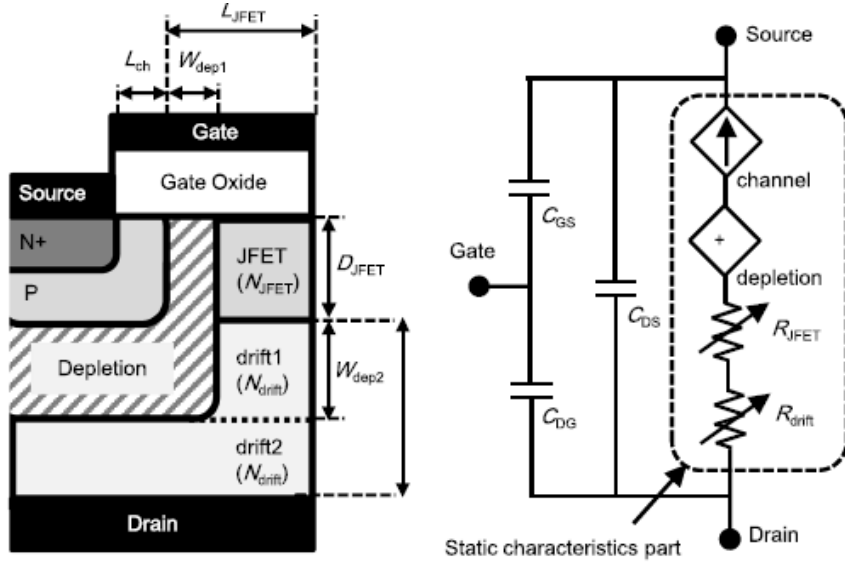


Figure 4.2. Macro behavioral MOSFET model [140]

Behavioral models are entirely based on measured data. Thus, the accuracy of such models depends on the measurement and the adequacy of the formulation implemented in the model. Moreover, large amounts of measurement sets need to be taken to cover the desired operation range of device. Generally, these models represent well the devices behaviors and valid only for a narrow range of operating conditions [135, 136, 140].

c. Physic-based compact model: To keep the advantage of physics-based models in precision and of behavioral models in determining parameters, physic-based compact models are developed. They are based on equations with certain parameters that are found by fitting the model equations to measured data with mathematical optimization. These models can reproduce the behaviors with accuracy, computational efficiency, and ease of parameter extraction.

4.1.2. Parameter extraction

The parameter extraction of the physic-based compact model from the device characterization or datasheets is a crucial issue. By using mathematical optimization, the model parameters can be identified even in very complex models; with constraints imposed, the physical meaning of the parameters can be conserved.

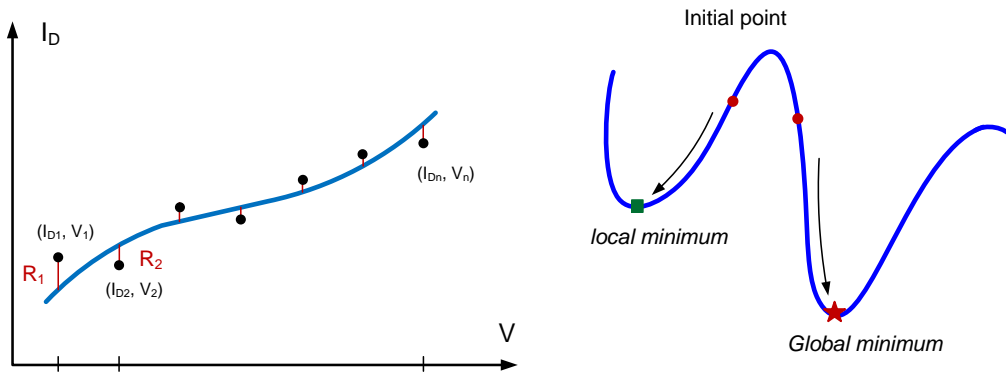


Figure 4.3. Parameters extraction using the minimum sum of least square deviations

In on-state modeling, the I-V characteristic curves are used as a tool to determine the model parameters. The parameter extraction is that the unknown parameter vector k is found to fit the model function $I_D = f(V_i, k)$ to a set of n measurement points $(I_{D1}, V_1), (I_{D2}, V_2) \dots (I_{Dn}, V_n)$. Here, $V_i = (V_1, V_2, \dots V_n)$ is the vector of bias voltages (usually it consists of V_{GS} or V_{DS}). As illustrated in Figure 4.3, a residual R_i is the difference from the measurement value I_{Di} and the value obtained by plugging the V_i into the model function. Mathematically, the curve fitting approximating a given data proceeds by finding the sum of the square deviations R^2 from each point of a set of n data points to the model:

$$R^2 = R_1^2 + R_2^2 + R_3^2 + \dots + R_n^2 = \sum_{i=1}^n [I_{Di} - f(V_i, k)]^2 \quad (4-1)$$

The squares of the residuals are used instead of their absolute values where the residuals are treated as a continuous differentiable quantity. The parameter vector k is determined using least-squares method where the model function fits best the given data.

The extraction procedure strongly depends on the model linearity, number of operating points and number of unknown parameters. Typically, depending on the initial parameters chosen, the fitting deals with the time-consuming and the convergences when the iteration of finding the sum of R^2 can end up converging to local minimum instead of global minimum, as shown in Figure 4.3. Furthermore, mutual relationships between parameters may lead to convergence issues or to non-physical values of the extracted parameters.

4.2. Power SiC MOSFET modeling

4.2.1. Shichman-Hodges model

A piecewise model, referred as Shichman Hodges model, is used widely for the simulation to represent the DC behavior of power MOSFET. Based on threshold voltage, the MOSFET behavior can be described with different physic equations. The drain current (I_D) depends on the region of device operation, as [141]:

$$I_D = I_{CH} = 0 \quad \text{when } V_{GS} < V_{TH} \quad (4-2)$$

$$I_D = I_{CH} = k_p \times (V_{GS} - V_{TH} - \frac{V_{CH}}{2}) \times V_{CH} \quad \text{when } 0 < V_{CH} \leq (V_{GS} - V_{TH}) \quad (4-3)$$

$$I_{Dsat} = I_{CHsat} = \frac{k_p}{2} \times (V_{GS} - V_{TH})^2 \times (1 + \lambda \cdot V_{DS}) \quad \text{when } 0 < (V_{GS} - V_{TH}) < V_{CH} \quad (4-4)$$

$$k_p = \frac{W}{L} \times C_{ox} \times \mu_{inv} \quad (4-5)$$

where k_p is the transistor gain, L is the channel length, W is the width of the transistor, C_{ox} is the oxide capacitance, μ_{inv} is the channel mobility and λ represents the channel length modulation factor. V_{CH} is the dropped voltage along the channel. In on-state, electrons flow from channel through the accumulation layer, then, travel along a narrow vertical path of the parasitic JFET to N-drift layer. Thus, the voltage applied at the terminals of the device is divided into 4 separate parts by the current flow, as shown in Figure 4.4.

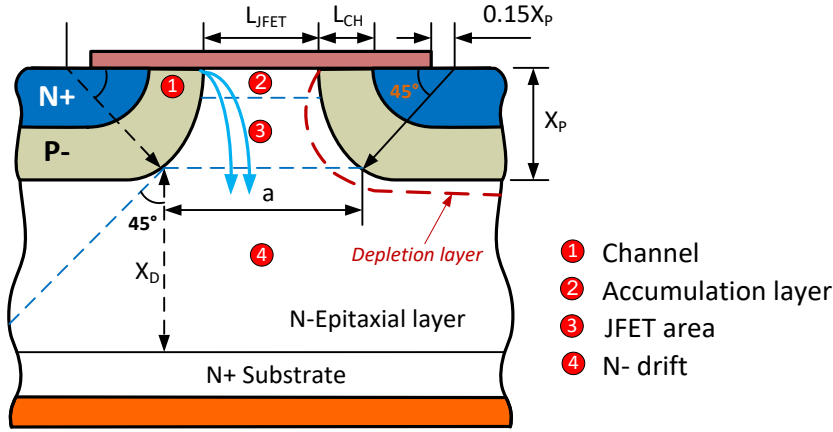


Figure 4.4. Four series components of voltage drop in VDMOSFET (after [7, 126, 142])

The dropped voltage V_{CH} along the channel is function of the channel resistance R_{CH} :

$$V_{CH} = I_{CH} \times R_{CH} \quad (4-6)$$

and is therefore highly nonlinear, depending on both V_{GS} and V_{DS} . The voltage V_{JFET} corresponds to the resistance in JFET region including R_{JFET} and R_{ACC} :

$$V_{JFET} = I_D \times (R_{JFET} + R_{ACC}) + V_{SCL} \quad (4-7)$$

The voltage V_{DRIFT} is caused by the ohmic resistance of the N-epitaxial layer (R_{DRIFT}):

$$V_{DRIFT} = I_D \times R_{DRIFT} \quad (4-8)$$

$$V_{DS} = V_{DRIFT} + V_{JFET} + V_{CH} = V_D + V_{CH} \quad (4-9)$$

V_D is the total voltage drop in drain region. The V_{SCL} is the voltage drop across depletion region. In the ohmic region, the gate bias is much higher than the drain voltage; a small reverse voltage V_{SCL} applied to the P-N junction results in a narrow depletion layers width and V_{SCL} is small enough to not be taken into consideration. The drain current (I_D) is equal to the channel current I_{CH} , thereby:

$$V_{DS} = I_D \times (R_{CH} + R_{ACC} + R_{JFET} + R_{DRIFT}) = I_D \times (R_{CH} + R_D) \quad (4-10)$$

Typically, R_D is approximately constant. Hence, for the ohmic region, the channel voltage in the equation (4-3) is implicitly related

$$V_{CH} = V_{DS} - I_D \times R_D \quad (4-11)$$

With drain voltage increasing, at the channel pinches-off, the quadratic function described by the equation (4-3) reaches a maximum point at:

$$V_{CH} = \frac{(V_{GS} - V_{TH})^2}{2 \times 0.5} = (V_{GS} - V_{TH}) = V_{CHsat} \quad (4-12)$$

The output curve flattens out at the onset of the saturation point. However, drain current increases slightly with V_{DS} , called short-channel effect. It is indicated in the equations (4-3) and (4-4) that the

ohmic region has a larger k_p than does the saturation region due to the non-uniformly shape of the channel. The separation between the ohmic and the saturation is usually verified for a power MOSFET; thereby two equivalent circuits exist. As shown in Figure 4.5, the current source driven by the gate voltage is valid for the saturation region. The other one is replaced in the equivalent circuit by a resistor, which is used for the ohmic region [6, 10, 47, 64].

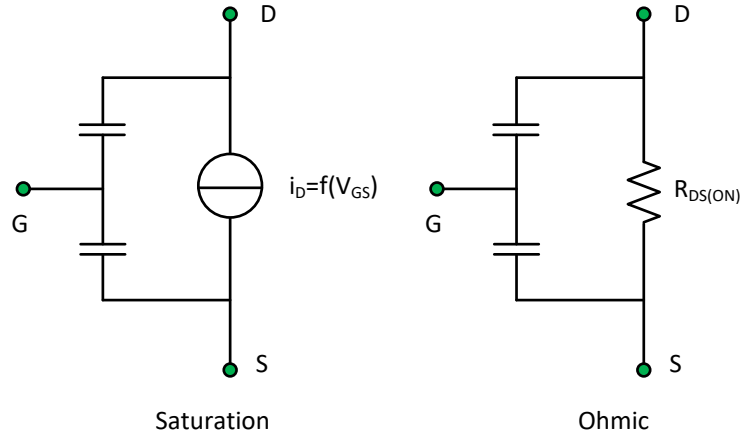


Figure 4.5. The models for a power MOSFET

The Shichman Hodges model takes the advantages of the simplicity and the acceptable accuracy. However, the model lacks some important effects such as velocity saturation or thermal effects.

4.2.2. Interface traps and their effects in SiC modeling

The SiC-SiO₂ interface states affect the device characteristics in a dramatic way, as analyzed in previous sections. In the on-state, the interface traps below the Fermi level E_F are negatively charged, also called acceptor-like states as shown in Figure 4.6.

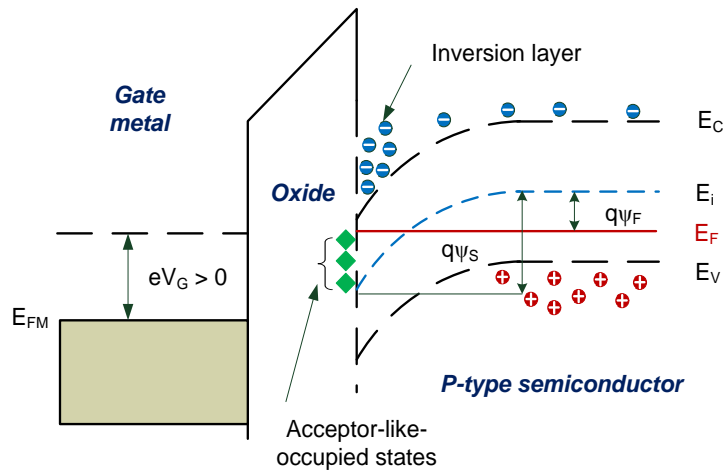


Figure 4.6. Electrons trapping in acceptor-like states in N-channel SiC MOSFET (after [3, 27])

The acceptor-like traps degrade the device performance in 3 ways:

1. Interface charges create a field that bends the bands and varies the flat-band voltage, V_{FB} , leading to a shift of the threshold voltage.

2. Traps near the band edges can confine and release carriers under different gate bias, temperature, thereby effect on the number of free carriers from the inversion layer.
3. By creating a localized coulomb field, the charges contribute to the scattering of carriers in the inversion channel, which reduces mobility.

The effects of interface traps on the charge and field distributions make the device characteristic complex and unpredictable, leading to difficulties in modeling [3, 20].

a. Interface traps effect on the number of free carriers

Typically, charges in the inversion layer are assumed to be the same as the total charges induced by the gate bias V_{GS} . The quantity of electron surface charge is given by the product:

$$Q_{inv} = -q \times N_{inv(total)} = -C_{ox} \times (V_{GS} - V_{TH}) \quad (4-13)$$

where $N_{inv(total)}$ is the total density of induced electrons in the MOSFET inversion layer. However, due to the electrons trapped at the SiC-SiO₂ interface, the number of free electrons in 4H-SiC MOSFET channel is reduced, which had been observed in previous studies [40, 133, 143]. Thus, the total charges induced by gate voltage are:

$$Q_{inv} + Q_{it} = -q \times (N_{inv} + N_{it}) = -C_{ox} \times (V_{GS} - V_{TH}) \quad (4-14)$$

$$Q_{inv} = -q \times N_{inv} = -[C_{ox} \times (V_{GS} - V_{TH}) - q \times N_{it}] \quad (4-15)$$

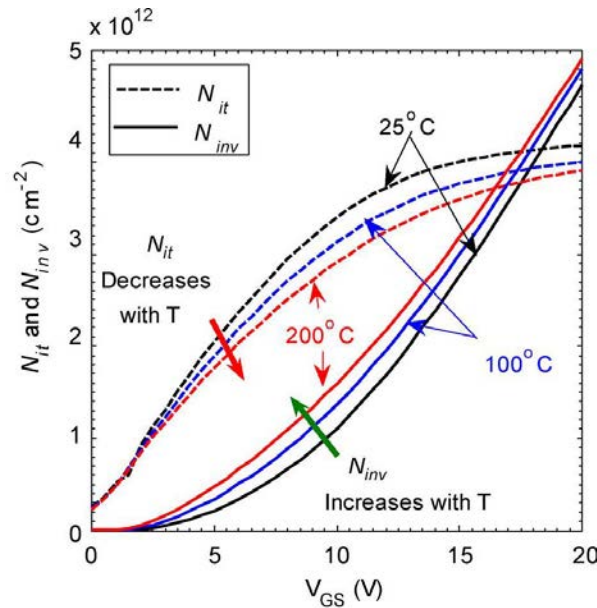


Figure 4.7. N_{inv} and N_{it} as a function of gate voltage and temperatures [122]

In theory, the occupied trap density (N_{it}) depends on the density of interface states (D_{it}) and the Fermi level at the interface. As depicted in Figure 4.7, the relation of inversion charge density (N_{inv}) versus gate bias and temperature was obtained by Potbhare [122, 144]. It is evident that N_{it} and N_{inv} increase with gate voltage V_{GS} . When almost all interface states are filled, N_{it} reaches a saturation level and N_{inv} rises further. The temperature behavior of N_{it} is opposite to N_{inv} one. The N_{it} reduces at higher temperature, resulting in a net increase of N_{inv} [3, 40, 122, 133, 145, 146].

Due to the interface states, the linear dependence of N_{inv} to gate voltage as described by equation (4-13) has been changed to:

$$Q_{inv} = -q \times N_{inv(V_{GS}, T)} = -C_{ox} \times k_{it(V_{GS}, T)} \times (V_{GS} - V_{TH}) \quad (4-16)$$

A factor k_{it} is introduced to compensate for the free electron reduction at inversion layer because of electron trapping at interface of SiC MOSFET. Then, the factor k_{it} is expressed as a function of gate bias and temperature.

b. Interface traps effect on mobility

As well introduced in 2.4.2, under high transverse (vertical) electric field E_x (controlled by gate bias) and high temperature, the carriers interact strongly with the oxide interface. In the presence of interface trap charges, the overall channel mobility of SiC MOSFET depends on the contribution of Coulomb mobility μ_C and other scattering mechanisms.

In a Si MOSFET, without interface traps, the channel mobility μ_{inv} reduces with gate bias due to the degrading of the surface acoustic phonon mobility μ_{AC} and the surface roughness mobility μ_{SR} [3, 7, 116, 147]. As the main scattering mechanism limiting electron mobility in SiC MOSFETs, increasing of μ_C with gate bias results in the rise of μ_{inv} . However, the N_{inv} keeps increasing with gate voltage, resulting in higher μ_C that is known as the screening effect of inversion electrons, as expressed in equation (2-32). Then, the dominant scattering mechanism changes from μ_C to μ_{SR} at high V_{GS} [3, 115]. Generally, with the increase of gate bias, the mobility in N-channel SiC MOSFETs tends to increase related to μ_C , then to decrease due to μ_{SR} , as shown in Figure 4.8.

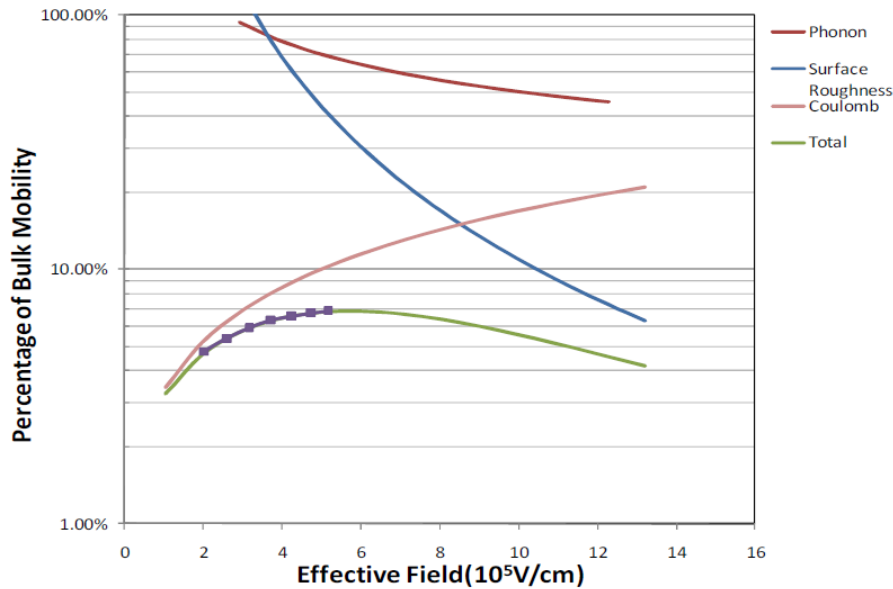


Figure 4.8. Mobility and field for 4H-SiC sample [115]

As aforementioned, the higher temperature results in higher phonon activity, higher scattering rates and thus lower mobility μ_{AC} . Once the electrons are deeper into the channel and away from the rough surface at higher temperature, μ_{SR} does not have a strong explicit temperature dependence [3, 122]. The N_{it} reduces with temperature increasing while the N_{inv} and the screening effect increase. The combined effect of these terms leads to an increase of μ_C with temperature.

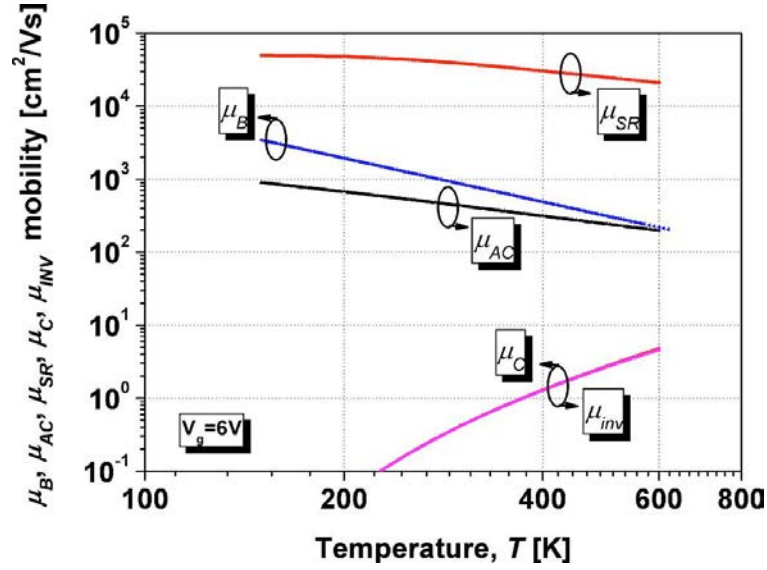


Figure 4.9. Mobility scattering vs the temperature at small gate bias [117]

In the absence of interface traps and the dominant of other scattering mechanisms (μ_{SR} and μ_{AC}), the Si MOSFET inversion channel mobility μ_{inv} decreases with temperature. It needs to be highlighted that the temperature dependence SiC MOSFET channel mobility is more complex due to the presence of μ_C . As shown in Figure 4.9, the total mobility μ_{inv} increases with temperature at small gate bias due to the dominant limiting mechanism of μ_C [102, 117]. However, as the gate keeps increasing, the surface roughness μ_{SR} becomes the dominant scattering mechanism when the μ_C mobility increases [3, 115, 122]. Then, the mobility μ_{inv} reduces with temperature at high gate bias. Hence, the transistor gain k_p depends on both temperature and gate bias, as:

$$k_{p(V_{GS}, T)} = \frac{W}{L} \times C_{ox} \times \mu_{inv(V_{GS}, T)} \quad (4-17)$$

4.2.3. Survey of related works in SiC MOSFET modeling

From the different behaviour, the existing Si models cannot be directly applied to predict the SiC device behavior. A lot of efforts have been carried out on development of SiC power MOSFET models in recent years. A review of various models for SiC MOSFETs reported in literatures thus far can be found in [110, 148, 149].

At an early stage of SiC modeling, a physic-based SiC MOSFET model implemented by Mc Nutt et al in [150] made a significant contribution for development of existing models. The model exhibits good descriptions but requires proprietary software for parameter extraction. The drift region with three separate parts was investigated in model of Hasanuzzaman [151]. Another physics-based model for a SiC DMOSFET accounting for non-uniform current distribution in JFET region was proposed in [152]. The n^{th} power law MOSFET model was used to simulate high voltage SiC power MOSFETs in [153, 154]. Then, a version of Mc Nutt were developed for simplified parameter extraction using datasheet [155]. A simple physical model of 4H-SiC devices was presented in [156, 157] without explicitly accounting for the effects of traps on DC characteristics.

In regard to the temperature effects, temperature-dependent current for 6H-SiC MOSFET was modeled in [158]. A simple behavioral SPICE model for 10 kV SiC MOSFETs with the consideration of the temperature dependence on gate threshold voltage, transconductance and on-state resistance was developed by Wang in [159]. On the basis of the model of Wang, Sun et al. modified the model that reflects accurately the characteristics of SiC MOSFET at low temperature [160]. The simulation of SiC MOSFET with the gate threshold voltage variation, carrier mobility and avalanche effect is included in the models in [161, 162]. A compact model for a discrete SiC MOSFET with channel mobility as an adjustable parameter was presented by Mukunoki [110]. Most of them are developed for single die MOSFETs with power ratings of 5–30 A. The SiC MOSFET model for 120 A power module is developed in PSPICE [163, 164].

Unlike the model mentioned above, the special physical phenomena occurring in SiC MOSFETs have been considered in some models. The large number of interface defects during the MOS thermal oxidation process reduces the inversion layer mobility due to Coulomb interface trap scattering. A based physical model for SiC MOSFETs considering carrier mobility and interface states was introduced in 2002 [165]. A comprehensive physical model was given in [122], incorporating interface trap densities, surface scattering, velocity saturation, and their dependences on temperature and bias. The influence of traps is taken into account in modeling with the variation of the electron mobility, the threshold voltage in [139, 149, 161, 162]. A model was developed with a good description of $R_{DS(ON)}$ behaviors in connection with the carrier mobility and interface traps [166].

4.3. Interface traps effect on threshold voltage

As mentioned in previous chapter, the threshold voltage is defined as

$$V_{TH} = V_{FB} + 2 \frac{kT}{q} \ln \frac{N_A}{n_i} + \frac{\sqrt{4 \cdot q \cdot N_A \cdot \epsilon_s \cdot \phi_B}}{C_{OX}} \quad (4-18)$$

It can be seen in the equation (2-27), the calculation of the V_{FB} is further complicated by gate charges. Among them, the Q_f and Q_{it} have strong effect to V_{FB} , which is typically described as:

$$V_{FB} = \frac{\Phi_{GS}}{q} - \frac{Q_{it}}{C_{OX}} - \frac{Q_f}{C_{OX}} \quad (4-19)$$

Q_f is positive charge while the change in Q_{it} is determined by the movement of E_f at the surface [40]. The effect of the total interface trapped charge $Q_{it}(\phi_s)$ on the observed gate voltage shift is:

$$\Delta V_{FB} = - \frac{Q_{it}(\phi_s)}{C_{OX}} \quad (4-20)$$

Q_{it} varies with ϕ_s , which makes the shift of ΔV_{FB} unstable and hard to predict. As mentioned earlier, the D_{it} of Si-SiO₂ based device remains at an acceptable level. Therefore, the variance of $Q_{it}(\phi_s)$ is small enough so that V_{TH} is constant. However, in case of SiC MOS, higher D_{it} translates into a larger $Q_{it}(\phi_s)$. With the gate bias, the increase of N_{it} results in more negative interface charge ($Q_{it} = qN_{it}$) in magnitude. A more negative Q_{it} requires a more positive threshold voltage [3, 41, 167]. The ΔV_{FB} with gate bias is no longer negligible.

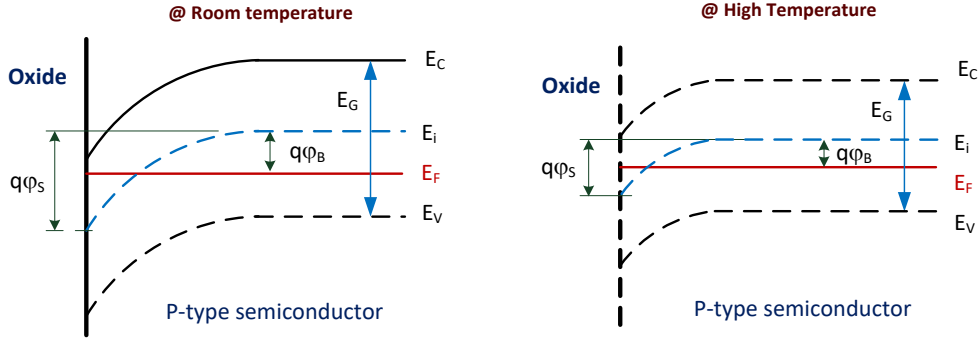


Figure 4.10. Energy-band diagram of a MOS structure in the inversion condition

Since the band gap E_G is narrowed with temperature, the band bending ($\phi_s = 2\phi_B$) also decreases as shown in Figure 4.10. Therefore, V_{TH} is reduced at higher temperature. The V_{TH} temperature dependence is clearly expressed by the equation (4-18). The rapid raise of n_i is partially offset by factor k with the increasing of N_A , thereby a reduction of ϕ_B . At the same time, depletion charge Q_D tends to decrease with temperature. V_{FB} decreases with temperature due to the Φ_s reduction for a P-type substrate in N-channel MOSFET. Moreover, the density of occupied traps N_{it} reduces at high temperature. Therefore, less interface states are occupied, less positive gate voltage is required. These phenomena can explain the negative shift of V_{TH} with temperature in the experiments.

The analytical model of V_{TH} , given by equation (4-18) is often used for theoretical analysis where design parameters are usually hard to obtain. Generally, the V_{TH} decrease with temperature is fitted by the linear expression:

$$V_{TH} = V_{TH0} \times [1 - \gamma(T - T_0)] \quad (4-21)$$

where V_{TH0} is the threshold voltage at the reference temperature T_0 , and γ is a coefficient.

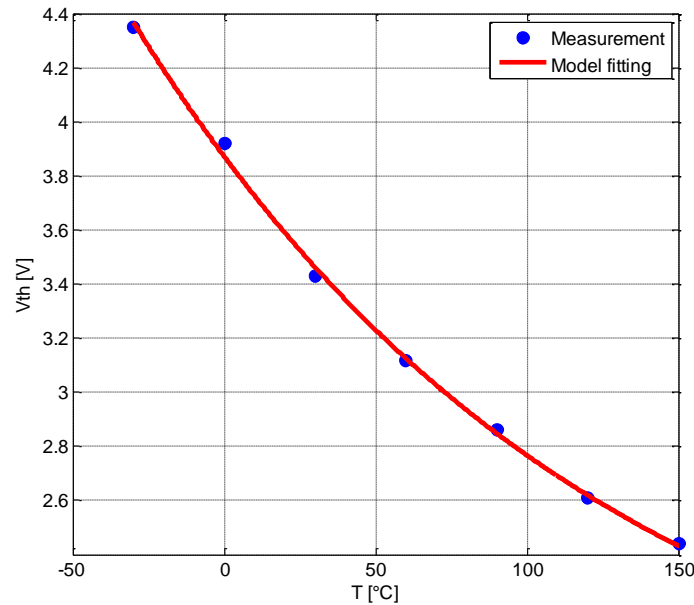


Figure 4.11. SiC MOSFET V_{TH} measurement and simulation comparison ($I_D = 50$ mA)

According to the previous analysis, the SiC MOSFET V_{TH} is primarily affected by interface traps charge. However, V_{TH} is expressed as the gate bias-independent parameter for the simplicity of modeling. From the measured curve, the SiC MOSFET V_{TH} cannot be expressed using the linear equation (4-21). The temperature dependence of SiC MOSFET V_{TH} can be explained by the interface states distribution toward temperature. Moreover, the density of interface trap (D_{it}) exponentially increases towards the conduction band edge (E_c) [143]. Therefore, the following polynomial expression for SiC MOSFET has been developed to obtain a fitted curve of V_{TH} with temperature [168]:

$$V_{TH(T)} = V_{TH1} \cdot e^{k_{t1} \cdot T} + V_{TH2} \cdot e^{k_{t2} \cdot T} \quad (4-22)$$

where V_{TH1} is the threshold voltage at the reference temperature ($T_0 = 30^\circ\text{C}$), V_{TH2} is a fitting parameter, k_{t1} and k_{t2} are the temperature coefficients.

V_{TH1} (V)	V_{TH2} (V)	$k_{t1} (^\circ\text{C}^{-1})$	$k_{t2} (^\circ\text{C}^{-1})$
3.618	0.26	-0.0045	0.0056

Table 4.1. Threshold voltage parameters

The proposed model is in good agreement with the experimental data as shown in Figure 4.11. V_{TH} can be calculated accurately with temperature changes. Using MATLAB, parameters of the model are extracted in Table 4.1.

4.4. Current gain and $R_{DS(ON)}$ modeling

The interface traps effects on the mobility and free carrier concentration in 4H-SiC MOSFETs have been discussed in section 4.2.2. Thus, the relationship between I_D , channel voltage V_{CH} and gate bias can be expressed by:

$$I_D = k_{p(V_{GS}, T)} \times k_{it(V_{GS}, T)} \times \left[(V_{GS} - V_{TH}) - \frac{1}{2} V_{CH} \right] \times V_{CH} \quad (4-23)$$

$$I_D = k_{(V_{GS}, T)} \times \left[(V_{GS} - V_{TH}) - \frac{1}{2} V_{CH} \right] \times V_{CH} \quad (4-24)$$

From the analyses with the gate bias and temperature, the interface traps and their occupation have strong influences on the device behavior. The combination of 2 factors k_{it} and k_p gives a new current gain parameter regarding the dependence of gate bias and temperature on current characteristics.

Typically, the ohmic region is described not by a mere resistance but by a rather complicated equation (4-24). However, at low drain current nearly zero, the term $0.5 \times V_{CH}$ is relatively small compared with the factor $(V_{GS} - V_{TH})$, thus it is ignored. The equation can be simplified as follows:

$$\begin{cases} I_D \cong k_{(V_{GS}, T)} \times (V_{GS} - V_{TH}) \cdot V_{CH} \\ V_{CH} = V_{DS} - I_D \times R_D \end{cases} \quad (4-25)$$

$R_{DS(ON)}$ derived from the inverse of the slope of output curve:

$$R_{DS(ON)} = \left. \frac{\partial V_{DS}}{\partial I_D} \right|_{V_{GS}=\text{const}} = \frac{1}{k_{(V_{GS}, T)} \times (V_{GS} - V_{TH})} + R_D \quad (4-26)$$

$$R_{DS(ON)} = \left. \frac{\partial V_{DS}}{\partial I_D} \right|_{V_{GS}=\text{const}} = R_{CH} + R_D \quad (4-27)$$

where R_D is the sum of resistance components except the channel one, which mainly consists of:

$$R_D = R_{JFET} + R_{DRIFT} \quad (4-28)$$

R_{JFET} is described in terms of the current flow in a narrow JFET channel in N-drift. Since V_{GS} is much higher than V_{DS} , the depletion layers around P-base can be neglected. R_{JFET} is implicitly assumed as constant. Moreover, the N-drift layer resistance R_{DRIFT} is expressed as a uniform layer by equation (4-29). The influence of the interface trap charges on the on-resistance is explained by the variation of R_{CH} with gate bias and temperature through factor k . Thus, $R_{DS(ON)}$ is modeled as the nonlinear resistive element of R_{CH} in series with the fixed drain resistance R_D .

4.4.1. $R_{DS(ON)}$ modeling with temperature

For a given gate bias, V_{TH} is derived from previous section. So, the on-resistance model for SiC MOSFET using equation (4-26) includes 2 unknown factors (k and R_D).

Specific information about the cellular design of the 1.2 kV 4H-SiC DMOSFET can be found elsewhere [55-58]. The thickness of N-type drift layer with (X_D) is 10 μm with the ionized dopant concentration (N_D) of $6 \times 10^{15} \text{ cm}^{-3}$. The channel length is 0.5-0.7 μm . The currentt state-of-the-art device is a 1.2 kV-20 A DMOSFET chip with die size of 4.09 mm \times 4.09 mm and an active conducting area of 0.101 cm^2 [58, 63]. The R_{DRIFT} arises primarily from the resistance of the lightly-doped N region:

$$R_{DRIFT} = \frac{X_D}{q \times \mu_N \times N_D \times A} \quad (4-29)$$

μ_N is the electron mobility in the direction of current flow in the N-drift which can be calculated by Caughey–Thomas empirical equation [3, 6]:

$$\mu_{N(4H-SiC)} \approx \frac{1020}{1 + \left(\frac{N_D + N_A}{1.8 \times 10^{17}} \right)^{0.6}} = 902.71 (\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}) \quad (4-30)$$

From the previous considerations, the drift layer resistance at 300 K for a chip can be estimated as:

$$R_{DRIFT} = \frac{X_N}{q \times \mu_N \times N_D \times A} = \frac{10 \times 10^{-4}}{1.602 \times 10^{-19} \times 900 \times 6 \times 10^{15} \times 0.101} \times 10^3 \quad (4-31)$$

$$R_{DRIFT} = 11.45 (\text{m}\Omega)$$

The N-drift layer of the vertical SiC MOSFET is built on a highly doped N^+ layer substrate. The substrate resistance (R_{SUB}) mainly depends on the thickness of the substrate, which is about 180 μm

at the 1.2 kV-rated MOSFETs [59]. The resistivity of SiC substrate is in the range of 0.015-0.028 $\Omega\cdot\text{cm}$ provided by manufacturer (CREE Inc). Therefore, the resistance of substrate R_{SUB} for a chip is:

$$R_{\text{SUB}} \approx 0.02 \times 0.101 \times 10^3 = 2.202 (\text{m}\Omega) \quad (4-32)$$

Hence, the estimated value of R_{DRIFT} (included the contribution of the substrate) for a module (within 5 paralleled chips) has a fairly small contribution to $R_{\text{DS(ON)}}$ which is estimated as:

$$\frac{R_{\text{DRIFT}} + R_{\text{SUB}}}{5} \approx 2.729 (\text{m}\Omega) \quad (4-33)$$

In general, the temperature dependence of mobility is expressed by a power law [112]:

$$\mu_{(T)} = \mu_0 \times \left(\frac{T}{300} \right)^{-n} (\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}) \quad (4-34)$$

T is the temperature; μ_0 is the value of the parameter at 300 K. The exponent n strongly depends on the doping. Its value is within 2.2 to 3.0 for lightly-doped, and 1.5 for highly-doped N-type 4H-SiC [3, 113, 114]. Thus, the temperature dependence of R_{D} can be merely expressed in the following form:

$$R_{\text{D}(T)} \approx R_{\text{D0}} \left(\frac{T + 273}{300} \right)^{k_R} (\text{m}\Omega) \quad (4-35)$$

here, R_{D0} is the value of drain region resistance at 30 °C, k_R is temperature coefficient of R_{D} .

From the data obtained by the 1.2 kV SiC DMOSFET characterization, $R_{\text{DS(ON)}}$ shows a non-monotonic behavior with temperature as shown in Figure 3.19 and Figure 3.20. As analyses above, this behavior comes from the interaction between the R_{CH} and R_{D} . Due to the lattice scattering increase, the drift region mobility reduces which results in a monotonic increase in R_{D} with temperature. Therefore, the non-monotonic behavior of SiC MOSFET $R_{\text{DS(ON)}}$ with temperature is determined by R_{CH} .

For a given gate bias V_{GS} , R_{D} is gate-independent parameter, expressed by equation (4-35). The V_{TH} displays a negative temperature coefficient which decreases with temperature using equation (4-22). So, R_{CH} behavior with temperature will be determined by the factor k which is not monotonic function of temperature. In our model, the model of k is proposed using the following form:

$$k^{V_{\text{GS}}(T)} = k_1^{V_{\text{GS}}} \left(\frac{T + 273}{300} \right)^2 + k_2^{V_{\text{GS}}} \left(\frac{T + 273}{300} \right) + k_3^{V_{\text{GS}}} \quad (4-36)$$

where the index " V_{GS} " is 2 V-step of gate bias, from 6 V to 20 V; for example, at gate bias $V_{\text{GS}} = 16\text{V}$, the model of $R_{\text{DS(ON)}}$ using the equations (4-22), (4-26), (4-35) and (4-36) can be described as:

$$\left. \frac{\partial R_{\text{DS(ON)}}}{\partial T} \right|_{V_{\text{GS}}=16\text{V}} = \frac{1}{k_{16(T)} \times (V_{\text{GS}} - V_{\text{TH}(T)})} + R_{\text{D}(T)} \quad (4-37)$$

$$= \frac{1}{\left[k_1^{16} \left(\frac{T+273}{300} \right)^2 + k_2^{16} \left(\frac{T+273}{300} \right) + k_3^{16} \right] \times (V_{GS} - V_{TH(T)})} + R_{D0} \left(\frac{T+273}{300} \right)^{k_R}$$

For parameter extraction, the nonlinear curve fitting techniques in MATLAB procedure determines unknown parameters k_1^{16} , k_2^{16} , k_3^{16} , k_R and R_{D0} . The following constraints is set for the curve fitting techniques

- the values of k and R_D are positive
- the lower bound of R_D is 2.729 m Ω , the upper bound could be the value of $R_{DS(ON)}$ at particular gate bias for each temperature.

The factor k is described as a quadratic function with temperature. The curve $R_{DS(ON)} = f(T)$ is well performed, for example at given gate bias $V_{GS} = 16$ V in Figure 4.12. The value of R_D is determined as:

$$R_D = 5 \times \left(\frac{T+273}{300} \right)^3 \text{ (m}\Omega\text{)} \quad (4-38)$$

R_{D0} from the calculation is higher than the lower bound of 2.729 m Ω . It can be explained by the spreading of the current in a trapezoidal shaped region, thereby the narrowing of N-drift layer, as mentioned in section 2.4.3. Besides the inherent structural resistances (R_{DRFIT} and R_{JFET}), the imperfect contact between the source and drain metal and the wiring (to connect parts inside the component) can also contribute to R_{D0} .

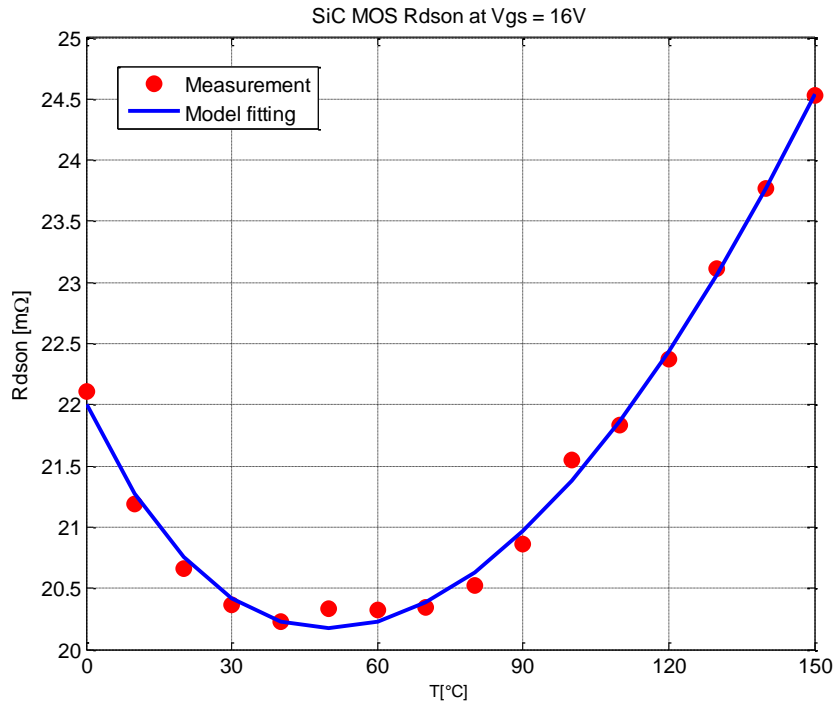


Figure 4.12. The curve fitting to measurement at $V_{GS}=16V$

In each step of 2 V from 6 to 20 V, with the R_D given by equation (4-38), the factor k is obtained from the calculation $R_{DS(ON)}$ at temperatures, many gate bias points. Values of k are listed in Table 4.2.

k								
V _{GS} /T°C	6V	8V	10V	12V	14V	16V	18V	20V
0°C	0.6956	1.4459	2.3683	3.2648	3.9945	4.5305	4.8455	5.0813
10°C	0.8411	1.6909	2.6649	3.5613	4.2617	4.7696	5.045	5.2366
20°C	0.9946	1.9376	2.9564	3.849	4.519	4.9978	5.2354	5.3856
30°C	1.1559	2.1858	3.2427	4.128	4.7664	5.2153	5.4169	5.5282
40°C	1.3252	2.4356	3.5239	4.3982	5.0039	5.4219	5.5894	5.6644
50°C	1.5024	2.687	3.7999	4.6596	5.2315	5.6177	5.753	5.7943
60°C	1.6875	2.94	4.0709	4.9122	5.4491	5.8026	5.9076	5.9178
70°C	1.8806	3.1946	4.3367	5.156	5.6568	5.9768	6.0532	6.0348
80°C	2.0815	3.4508	4.5974	5.3911	5.8546	6.1401	6.1898	6.1456
90°C	2.2904	3.7085	4.853	5.6174	6.0425	6.2926	6.3175	6.2499
100°C	2.5072	3.9679	5.1034	5.8349	6.2205	6.4343	6.4362	6.3478
110°C	2.732	4.2289	5.3487	6.0436	6.3885	6.5651	6.5459	6.4394
120°C	2.9646	4.4914	5.5889	6.2436	6.5467	6.6851	6.6467	6.5246
130°C	3.2052	4.7556	5.824	6.4348	6.6949	6.7943	6.7385	6.6034
140°C	3.4537	5.0213	6.0539	6.6172	6.8331	6.8927	6.8214	6.6759
150°C	3.7101	5.2887	6.2788	6.7908	6.9615	6.9802	6.8952	6.7419

Table 4.2. Extracted value of k

4.4.2. K determination and R_{DS(ON)} validation

Based on the results in Table 4.2, k is no longer modeled as a two-variable function of both V_{GS} and T.

At a given temperature, with the increasing of V_{GS}, k goes up. Thus, the gate-dependent-model of k is built using the form:

$$k^T_{(V_{GS})} = k_a^T \times V_{GS}^3 + k_b^T \times V_{GS}^2 + k_c^T \times V_{GS} + k_d^T \quad (4-39)$$

For instance, at 30 °C, the unknown factors k_a^{30} , k_b^{30} , k_c^{30} , k_d^{30} are extracted from Table 4.2. R_D is calculated by equation (4-38). With k described by (4-39), the R_{DS(ON)} can be well represented with the change of gate bias, as predicted in Figure 4.13.

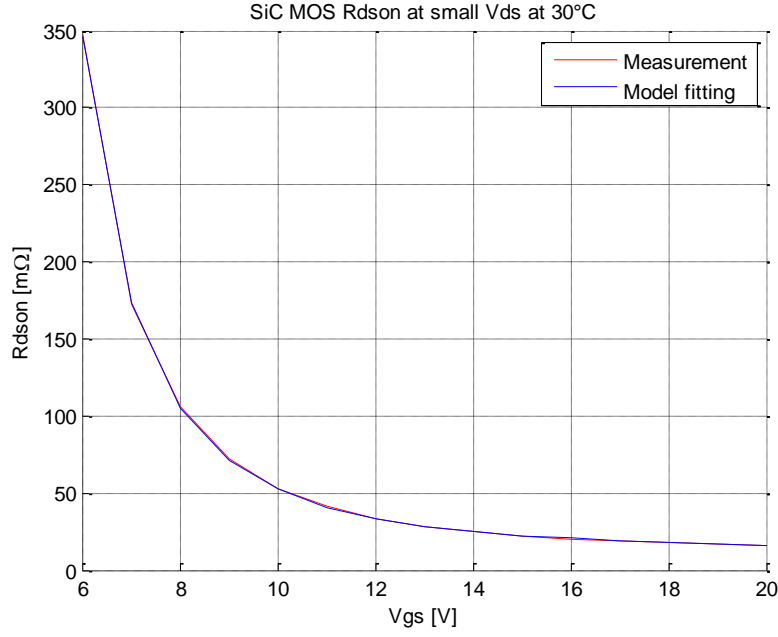


Figure 4.13. The curve fitting to measurement at 30°C

Each step of 10 °C from 0 °C to 150 °C, the factors of k namely k_a^{10} , k_a^{20} , k_a^{30} , ..., k_a^{150} , k_b^{10} , k_b^{20} , k_b^{30} , ..., k_b^{150} are obtained. As a temperature dependent factor, these values change as function of the temperature. The following polynomial fitting function is used to obtain the fitted curve of k :

$$k_a^T = ka_1 \left(\frac{T+273}{300} \right)^2 + ka_2 \left(\frac{T+273}{300} \right) + ka_3 \quad (4-40)$$

$$k_b^T = kb_1 \left(\frac{T+273}{300} \right)^2 + kb_2 \left(\frac{T+273}{300} \right) + kb_3 \quad (4-41)$$

$$k_c^T = kc_1 \left(\frac{T+273}{300} \right)^2 + kc_2 \left(\frac{T+273}{300} \right) + kc_3 \quad (4-42)$$

$$k_d^T = kd_1 \left(\frac{T+273}{300} \right)^2 + kd_2 \left(\frac{T+273}{300} \right) + kd_3 \quad (4-43)$$

The k can be modeled as the function of gate bias and temperature by equation (4-39). The sub-parameters are given by equations (4-40), (4-41), (4-42) and (4-43). The modeling is in good agreement with the measurement as shown in Figure 4.14, dots referring to data extracted in Table 4.2 and line curves referring to model of k using equation (4-39).

Combining all of these equations, the final $R_{DS(ON)}$ expression ends up being:

$$R_{DS(ON)} = \frac{1}{(k_a^T \times V_{GS}^3 + k_b^T \times V_{GS}^2 + k_c^T \times V_{GS} + k_d^T) \times (V_{GS} - V_{TH(T)})} + R_{D0} \left(\frac{T+273}{300} \right)^{k_R} \quad (4-44)$$

A unique behavior of the $R_{DS(ON)}$ of 1.2 kV SiC MOSFET with temperature has been modeled. It arises from the interface trap effects which are described by factor k in a simple empirical model. There is a good agreement between the modeling results and experimental measurements over the whole temperature range as shown in Figure 4.15 and Figure 4.16.

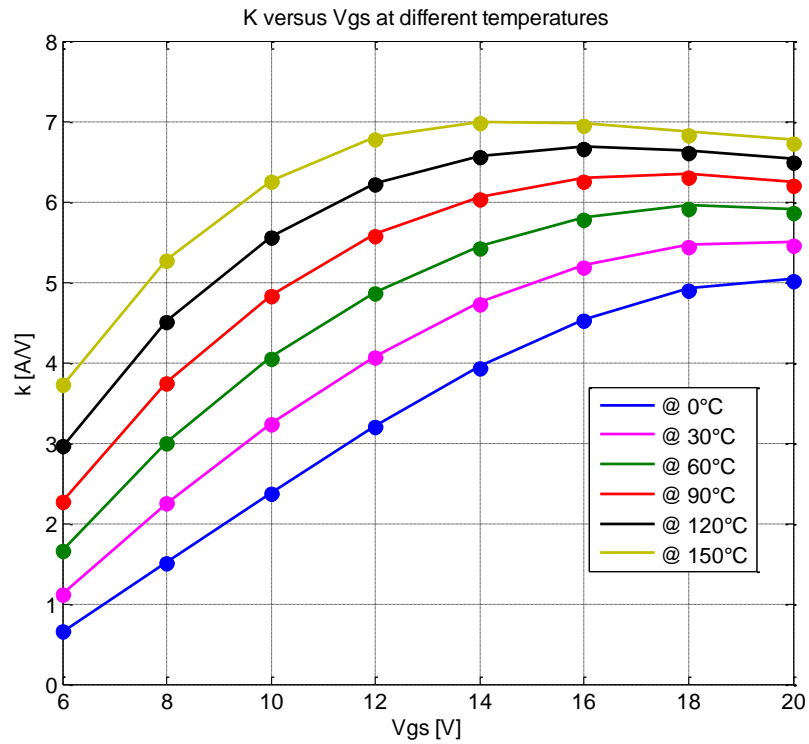


Figure 4.14. Model for k with gate bias and temperatures

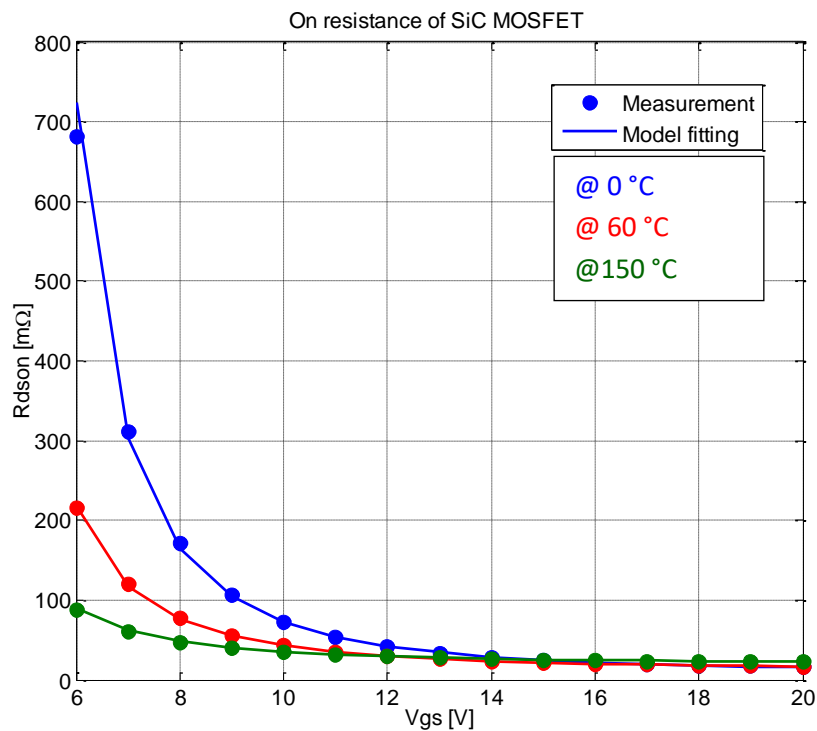


Figure 4.15. The curve fitting to measurement at different temperatures

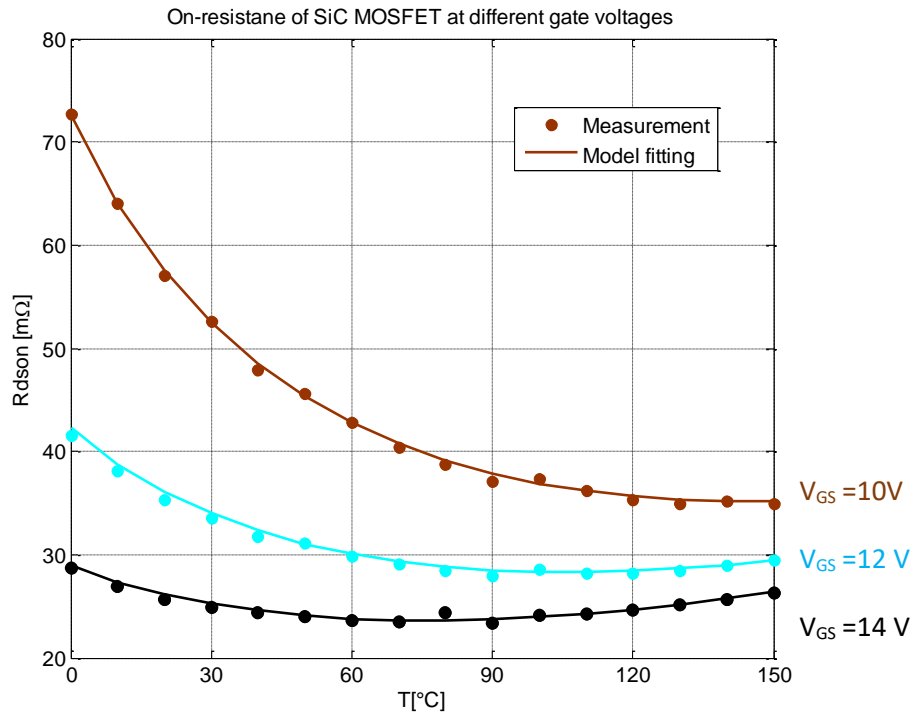
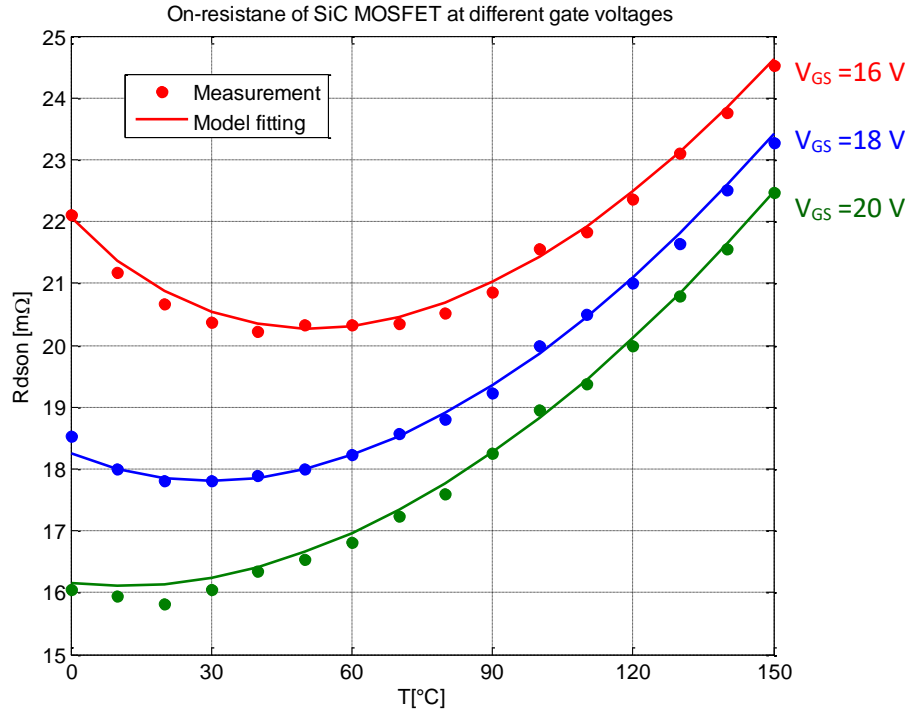


Figure 4.16. The curve fitting to measurement at different gate bias

4.5. SiC MOSFET DC modeling

4H-SiC MOSFETs have been structured with very short channel length, approximately of 0.5 - 0.7 μm . The overlap of depletion regions within P-base gets the channel length shortened. Since the depletion widths are comparable to the channel length, new phenomena take place, called short-channel effects. However, with high doping density of P-base, the SiC DMOSFET model does not consider the effects of the channel length modulation (λ) and drain induced barrier lowering in

modeling [169]. Consuming the power on the order of hundred watts, SiC MOSFETs do self-heat. Therefore, the thermal aspect should be addressed.

4.5.1. The coefficient α and short-channel problem

In the strong inversion mode, the depletion charge is no longer controlled by the gate bias V_{GS} . The incremental gate charge is balanced by the increase of inversion layer charge. Thus, the depletion capacitance C_D does not participate in the process of balancing the charge neutrality. So the inversion charge Q_{inv} is approximated by C_{OX} , using equation (4-13).

The V_{TH} calculation in equation (4-18) assumes that depletion charge Q_D is constant at any point in the y direction. However, the channel narrows toward the drain side [30]. In such a way, the V_{TH} effectively changes along the channel due to the non-uniformity of depletion thickness. Moreover, the SiC-SiO₂ interface trap density is high, so the capacitance associated with the interface traps can be considered in parallel with the C_D . Thus, the effects of depletion charge and interface traps on Q_{inv} are considered with a parameter alpha α [6, 27, 138]. The equation (4-16) now is expressed as:

$$Q_{inv(y)} = -C_{ox} \times k_{it(V_{GS}, T)} \times (V_{GS} - V_{TH} - \alpha \times V_{CH(y)}) \quad (4-45)$$

$$\alpha = 1 + \frac{C_D}{C_{OX}} \quad (4-46)$$

Hence, the depletion charge has been taken into account in modeling. The current in ohmic region is mathematically described by:

$$I_D = k_{(V_{GS}, T)} \times \left[(V_{GS} - V_{TH}) - \frac{\alpha}{2} \cdot V_{CH} \right] \times V_{CH} \quad (4-47)$$

As expressed by equation (4-47), the shape of I-V curve depends on the values of k and the coefficient α . The parameter α can be used to change the simulation curve for accurate estimation of the SiC MOSFET operating with the gradual transition between ohmic and saturation region. When V_{DS} reaches the onset of saturation, the lateral electric field in the channel reaches the critical field E_c , carriers travel with the saturated velocity. In short-channel device, the current saturates prematurely mainly due to velocity saturation occurring before pinch-off condition [30, 149, 170-172]. With parameter α , the saturation voltage can be calculated as:

$$V_{CHsat} = \frac{(V_{GS} - V_{TH})}{\alpha} \quad (4-48)$$

Thus, the value of alpha is chosen to obtain better accuracy when fitting the experimental curve. It can be optimized with gate biases and temperature but is higher than 1.

4.5.2. JFET effect in SiC MOSFET

It is worth mentioning that the SiC MOSFET current is spread over a range of V_{DS} for a given gate bias. From our experimental tests, the SiC MOSFET output curves are not flat at high V_{DS} up to 20 V, with relatively small gate voltage (i.e, $V_{GS} = 6$ V). Thus, the boundary between ohmic and saturation regions is not clearly defined in SiC MOSFET, which needs for more attention in modeling.

Typically, when the device operates in saturation regime, the factor λ is used in equation (4-4) to explain a slight increase of current with V_{DS} . In such a way, a further increase of I_D with V_{DS} can give a higher λ ($0.046 - 0.15 \text{ V}^{-1}$) for SiC MOSFET modeling [162, 173]. However, based on finite-element analysis, Fu Ruiyun et al. [152] showed that channel pinch-off does not occur in the SiC MOSFET even at high V_{DS} . Therefore, the channel length modulation with factor λ is insufficient to describe the unclear saturation region of SiC MOSFET.

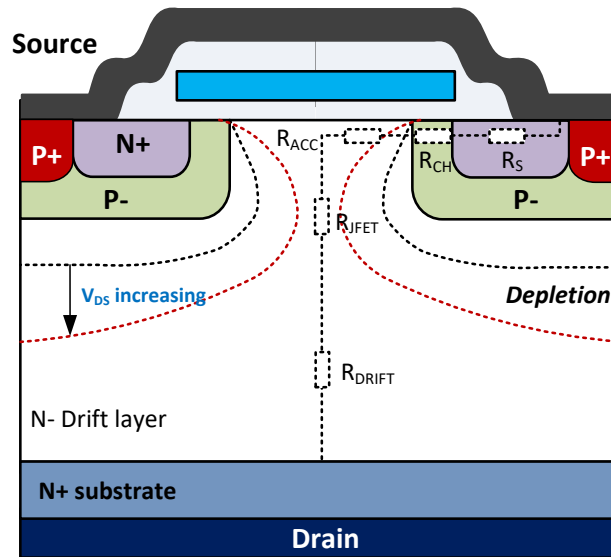


Figure 4.17. On-resistance of VDMOSFET at different drain voltage

Regarding physical phenomena, the channel conductance is well determined for a given V_{GS} above V_{TH} . Then, the current is controlled by JFET region. With V_{DS} increase, the depletions between the P-wells extend into the N-drift region, leading to a further strong constriction of the current path, as illustrated in Figure 4.17. Since most of the V_{DS} drop occurs in the depletion area, V_{CH} remains below the pinch-off voltage value. Thus, the current does not saturate. Therefore, the JFET has a significant contribution to current behavior of SiC MOSFET in terms of the non-uniform electron distribution in the N-drift.

In [152] the JFET region is modeled by voltage source for the lateral voltage drop (V_{SCL}) in the depletion layers and the resistor network (R_{JFET}) for a non-uniform current distribution. The growing of depletion regions makes the JFET resistance higher. Thus, the nonlinear resistance of JFET is used to describe the drain resistance variation with drain bias, gate voltage and temperature in [149, 162]. In other way, the SiC MOSFET saturation occurring at high V_{DS} can be explained by the control of a series of MOS channel and JFET channel. The author T. R. McNutt proposed the model as the superposition of 2 current components I_{mosh} and I_{mosl} which saturate at different drain voltages [150]. However, the model becomes complicated with large number of parameters to be extracted.

4.5.3. Channel voltage

From a physical viewpoint, Si MOSFET saturation current primarily occurs in the channel region. As aforementioned, saturation mechanisms (pinch-off or velocity saturation) are not fulfilled in the SiC MOSFET channel. Since a large part of the V_{DS} drops in the drain region, intrinsic SiC MOSFET channel

is still not saturated. Nevertheless, the current increases gradually to saturation level when the electrons near the JFET region reach their saturation velocity [110, 149, 152]. Especially, with high velocity saturation, the saturation current of SiC MOSFET occurring over the V_{DS} is expected significantly higher than usually experienced with Si MOSFETs.

Although the current does not get saturated in channel at high V_{DS} , the channel current-based model in equation (4-47) is still used to describe this behavior. For a given gate voltage, channel voltage V_{CH} is considered as an adjustable parameter in the model. The voltage drop in the channel (V_{CH}) in equation (4-11) is now determined by means of voltage drops in depletion region V_{SCL} , in JFET region ($I_D \times R_{JFET}$), and in drift region ($I_D \times R_{DRIFT}$):

$$V_{CH} = V_{DS} - (V_{SCL} + I_D \times R_{JFET} + I_D \times R_{DRIFT}) \quad (4-49)$$

V_{SCL} increases with the depletion extension. The incremental V_{DS} is balanced by the increase of V_{SCL} . Thus, V_{CH} reaches a maximum value at comparatively high V_{DS} , corresponding to saturation current. Therefore, a rational function is used to describe V_{CH} as the function of V_{DS} . The V_{CH} is used to represent the current path in the N-drift under the control of depletion layers, which depends on temperature, V_{DS} and V_{GS} . Here, the V_{CH} is treated as a temperature-dependent parameter with strong dependence on bias voltages:

$$V_{CH} = \frac{a_{(V_{GS}, T)} \times V_{DS}}{V_{DS} + b_{(V_{GS}, T)}} \quad (4-50)$$

$$I_D = k_{(V_{GS}, T)} \times \left[(V_{GS} - V_{TH}) - \frac{\alpha}{2} \times \frac{a_{(V_{GS}, T)} \times V_{DS}}{V_{DS} + b_{(V_{GS}, T)}} \right] \times \frac{a_{(V_{GS}, T)} \times V_{DS}}{V_{DS} + b_{(V_{GS}, T)}} \quad (4-51)$$

A simplified model is developed using equation (4-51) which incorporates interface traps with k , short-channel with factor α and temperature effects. For a given V_{GS} , the current I_D increases with V_{DS} , and slowly reaches the saturation level by the control of V_{CH} . Therefore, the current saturation mechanism for SiC MOSFET occurs in the JFET region is also well represented. This approach does commonly violate the physical phenomenon but often still gives acceptable results using normal equation.

4.6. Parameter extraction and model validation

4.6.1. Parameter extraction

The proposed model in equation (4-51) with 4 parameters, including k , α , a , and b is used to describe the DC characteristics of a SiC power MOSFET. The model parameters are directly extracted from the measured data. At small V_{DS} , the effect of longitudinal electric field on mobility can be neglected. Thus, the factor k and V_{TH} are archived from earlier sections. At particular temperature, the unknown parameters of V_{CH} (a and b) are adjusted to fit the output characteristics and they are listed below:

- for a given gate voltage, using the proposed model in equation (4-51) and experimental output curves I_D – V_{DS} , the “ a ” and “ b ” are determined with a best curve-fitting procedure.
- the coefficient α is kept constant at value 1.2 as gate bias-independent parameter.

- the same extraction is performed at 2-V increment of V_{GS} from 6 V to 20 V.

At the simulation temperature (i.e, $T = 30^\circ\text{C}$), based on the extracted data (a and b) with the V_{GS} step of 2 V, the gate bias-dependent model of V_{CH} is found, using the relation:

$$a^T_{(V_{GS})} = a_1^T \times V_{GS}^3 + a_2^T \times V_{GS}^2 + a_3^T \times V_{GS} + a_4^T \quad (4-52)$$

$$b^T_{(V_{GS})} = b_1^T \times V_{GS}^3 + b_2^T \times V_{GS}^2 + b_3^T \times V_{GS} + b_4^T \quad (4-53)$$

Figure 4.18 shows the experimental and simulated output characteristics after the extraction of the aforementioned sub-parameters ($a_1^{30}, a_2^{30}, a_3^{30}, a_4^{30}$) ($b_1^{30}, b_2^{30}, b_3^{30}, b_4^{30}$).

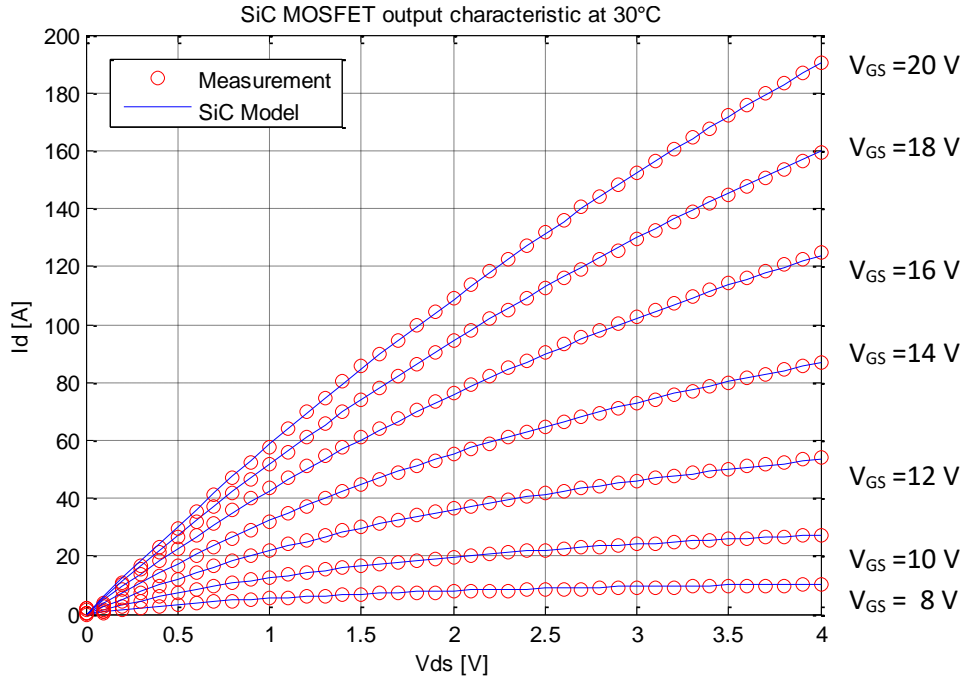


Figure 4.18. Measurement and simulation output characteristic at 30°C

The factor alpha ($\alpha = 1.2$) is fixed to the room temperature value. The values of sub-parameters a_1, a_2, a_3, a_4 and b_1, b_2, b_3, b_4 are obtained at several temperature points (each step of 30°C from 0°C to 150°C), then, the temperature scaling of V_{CH} can be using the temperature scaling form of:

$$a_1^T = a_{11} \left(\frac{T + 273}{300} \right)^2 + a_{12} \left(\frac{T + 273}{300} \right) + a_{13} \quad (4-54)$$

$$a_2^T = a_{21} \left(\frac{T + 273}{300} \right)^2 + a_{22} \left(\frac{T + 273}{300} \right) + a_{23} \quad (4-55)$$

$$a_3^T = a_{31} \left(\frac{T + 273}{300} \right)^2 + a_{32} \left(\frac{T + 273}{300} \right) + a_{33} \quad (4-56)$$

$$a_4^T = a_{41} \left(\frac{T + 273}{300} \right)^2 + a_{42} \left(\frac{T + 273}{300} \right) + a_{43} \quad (4-57)$$

With parameter b, the same extraction is performed. The complete model with all the temperature dependence can well represents a wide region of operations of device with time-efficient, as illustrated in Figure 4.19.

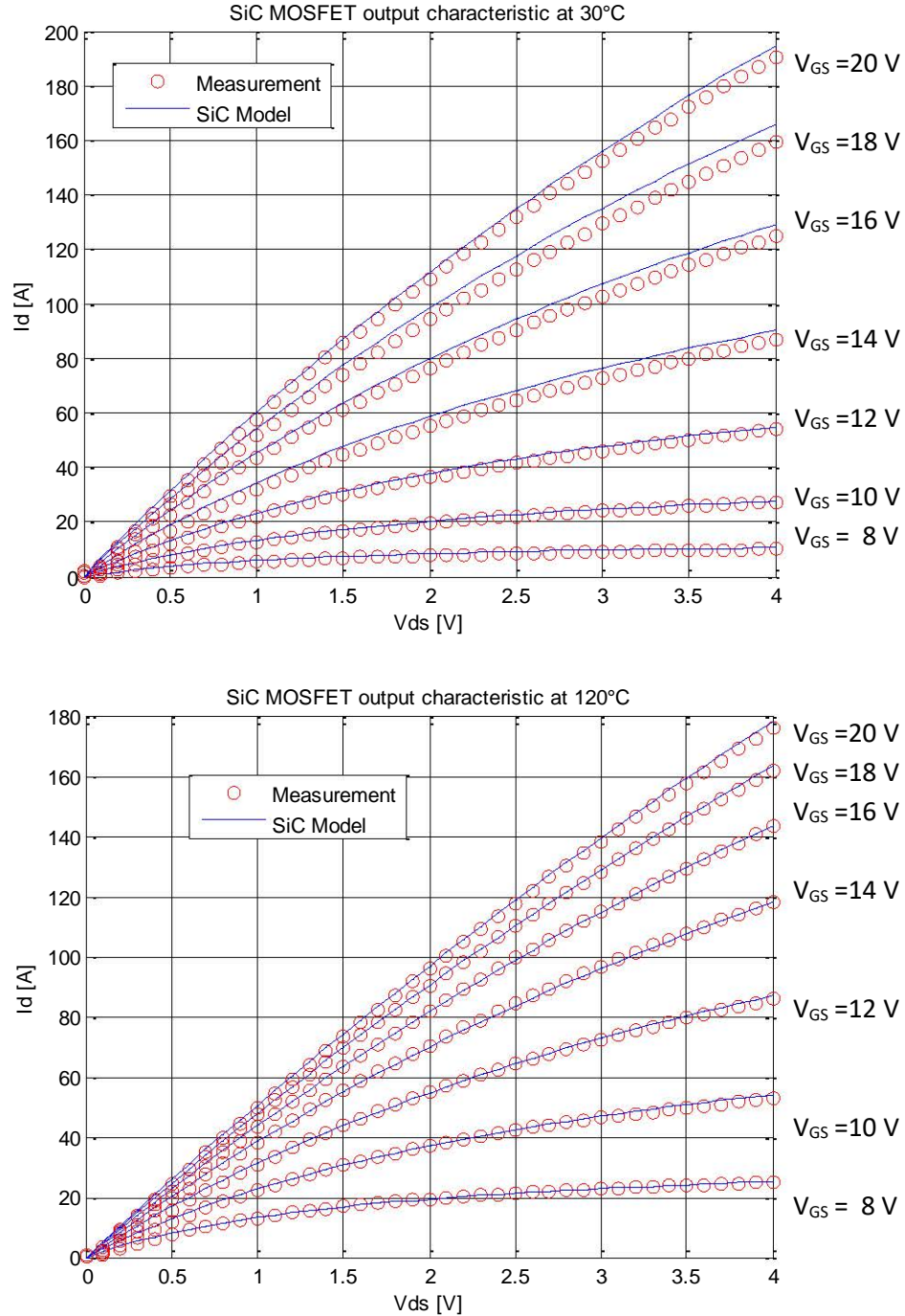


Figure 4.19. Output characteristic using full model at different temperatures

One should pay attention that the SiC MOSFET I_D increases with temperature at small gate bias but decreases at high gate voltage. This is contrary to what is normally observed in standard Si counterparts. It is explained by relating temperature dependent device performance to interface trap

charging in previous sections. This unique behavior is well described by the proposed model as predicted in Figure 4.19 with $T = 30\text{ }^{\circ}\text{C}$ and $120\text{ }^{\circ}\text{C}$.

4.6.2. Simulation in Saber

The SABER (Synopsys) is one of the most widely simulation platforms for power electronics used in industrial context as well as in academic institutions. SABER Sketch is the schematic interface of the simulator where circuit schemes are created by placing the parts onto the simulation window. The parts used in schematics are available in the parts gallery (known as a built-in library) where the models for commercially available semiconductor are provided [174].

With the possibility of creating new models, the power SiC MOSFET model has been developed and given specifically for the SABER platform. Using a single-piece model by equations (4-51), the SiC MOSFET model for the SABER simulator is created using MAST (a programming language unique to SABER®). The model with 3 electrical ports (G, D and S) and T_j for the temperature consideration is illustrated in Figure 4.20. The parameters of the model are extracted by the experiments, as discussed in sections 4.4 and 4.6.1.

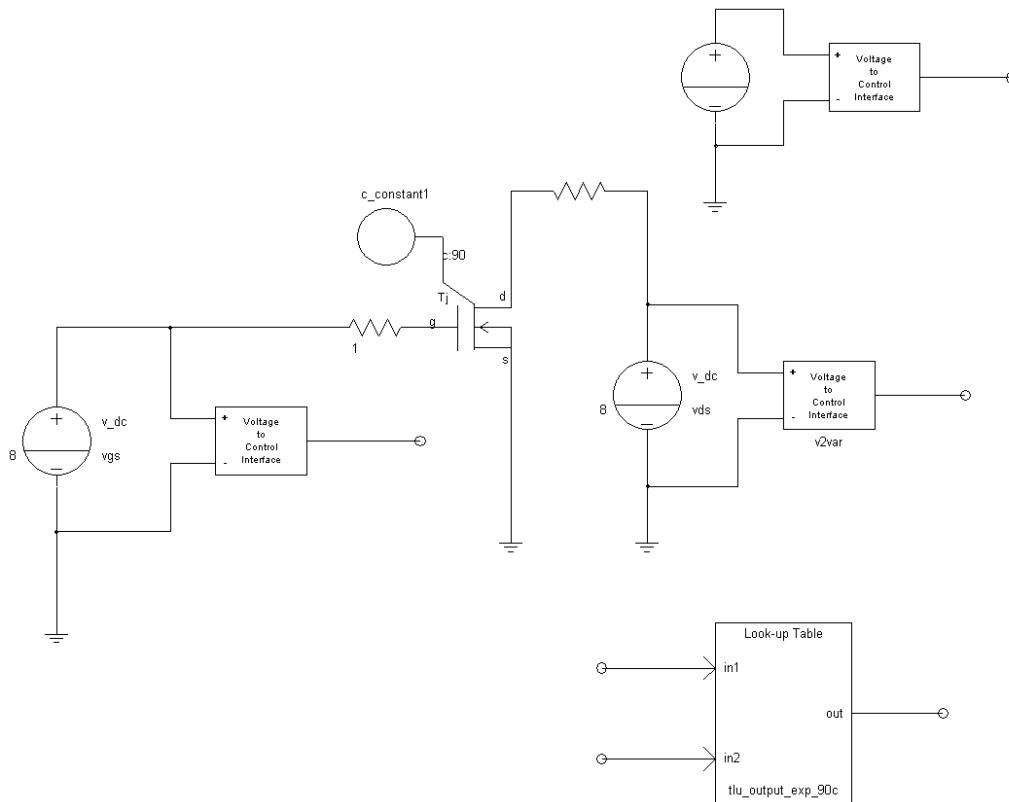


Figure 4.20. SiC MOSFET output characterization in Saber at temperature of 90°C

The simulation circuits have been implemented in Saber to verify the aforementioned characteristics (see Figure 4.20). The model developed in Saber is used to compare the output experimental curves (V_{DS} up to 4 V) over a wide temperature range of 0°C to 150°C . The good agreement between the experimental and simulation can be grasped in Figure 4.21.

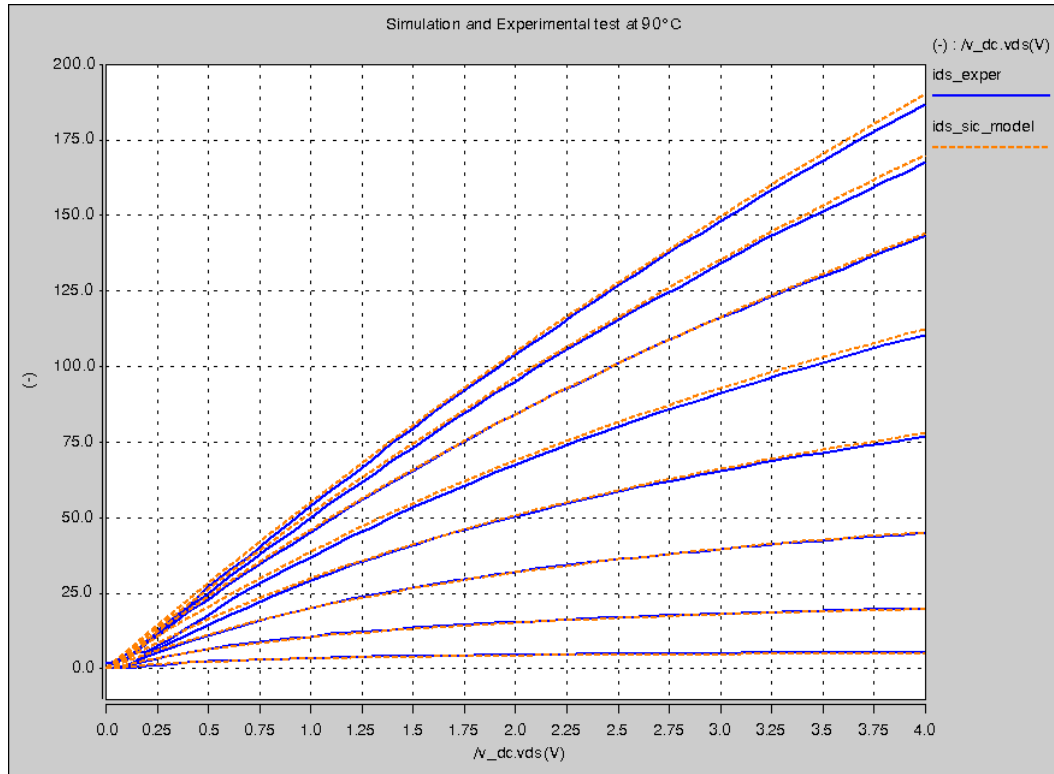


Figure 4.21. Output simulation curves and experiments at 90 °C

4.8. Conclusion

This chapter firstly discusses the effects of interface traps on modeling and simulation of 4H-SiC MOSFETs.

The model of threshold voltage has been developed which has been verified through experiments. The V_{TH} is independent from the operating voltages V_{GS} and V_{DS} . The effects of temperature on the SiC MOSFET V_{TH} are considered with the presence of interface traps by the exponential function.

The modeling for $R_{DS(ON)}$ has been developed where the model parameters are extracted from the measurements with the physical correlation. In the channel, the inversion mobility and free carrier concentration is determined by the interface trap charges at the SiC-SiO₂ interface which has been well described by factor k . The increase of drift resistance is modeled as the reduction of drift region mobility. The behavior of on-resistance of SiC power MOSFETs over temperature has been explained and modeled. The measurement result of $R_{DS(ON)}$ of the SiC MOSFET and its model have shown a good agreement in the whole range of working temperatures.

A new compact model for SiC power MOSFETs has been presented in the last part of this chapter. The proposed model is based on the level 1 model, with new current gain k . The channel voltage is considered as an adjustable parameter that is modeled as the function of V_{DS} , V_{GS} as well as temperature. The model can be implemented in Matlab or Saber. The parameters of the proposed model have been derived from the measurements of DC characteristics. The model simulations have been validated by the shape of the I-V characteristics of SiC MOSFET with unclear saturation of the drain current over a wide temperature range of 0° C to 150 °C.

Chapter 5 Thermal measurements and model validation

Under normal operating conditions, the power dissipation in either conduction or switching mode is transferred into heat due to the self-heating effect, resulting in the device temperature rise. Having a considerable influence on the device characteristics, therefore, the device's temperature must be monitored and guaranteed below the specified limits under all operating conditions [175, 176].

Since the SiC MOSFETs are designed to operate at high temperature and high-power applications, their thermal characteristics must be carefully considered in the design for reliable power electronics systems. Despite the high thermal conductivity of SiC material, the electro-thermal issues due to self-heating are still the challenge in using the SiC MOSFETs. This chapter deals with the thermal characterization of a packaged SiC MOSFET through experimental test and analyses.

5.1. Thermal issues in power semiconductor devices

5.1.1. Power semiconductor device package

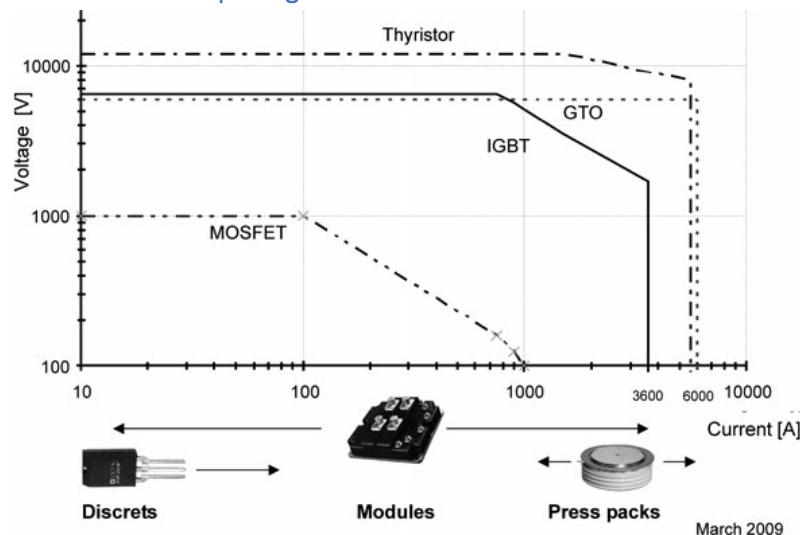


Figure 5.1. Power range vs package types of power semiconductor device [6]

In the commercial marketplace, the power semiconductor devices are available as either a discrete integrated circuit (IC) or power module, depending on the desired power level, voltage level and application as depicted in Figure 5.1. Besides, the modules in press-pack technology are designed with currents up to 1100 A, particularly for power transmission and industrial voltage drives applications [177, 178]. Typically, the package is used to prevent damage to the chip from the external environment, connect a die to the external circuit and provide a way to remove the heat from the device. Therefore, the package affects the device characteristics [6].

In the range of small power, the discrete SiC MOSFET prevails with the package of the transistor outline (TO), as shown in Figure 5.2. The active part (also referred as die) is soldered directly to a solid copper tab (called as lead frame) which mounts the component to a heat sink. Pins (leads) are

connected to contact areas on the chip by wire bonds. The whole set is either partially or completely encapsulated in plastic.

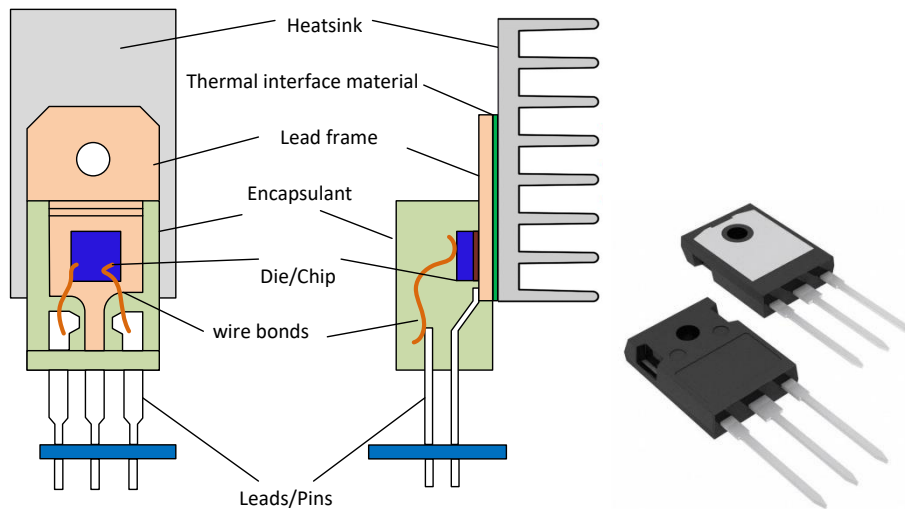


Figure 5.2. Power discrete device package

As for the power module, it is structured with multiple chips in parallel to handle a high power. The number of paralleled chips depends on the rated current of the device [179]. The schematic structure of the MOSFET module consists of several principle materials as presented in Figure 5.3. The chips are soldered in direct bonded copper (DBC) substrate (two layers of copper directly bonded onto a ceramic layer). The substrate is attached to the base plate by another solder layers.

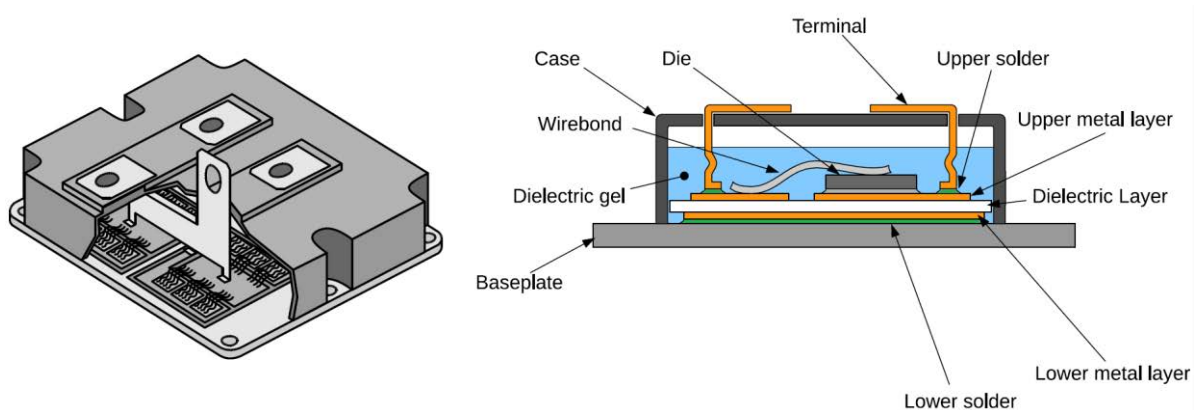


Figure 5.3. Internal layout of and cross-sectional structure of the module [179-181]

The existing package issues include wire-bonding, parasitic parameters (resistance, capacitance, and inductance), reliability, and thermal management. Particularly, increasing the current rating within the module also enlarges the unbalanced current sharing among the paralleled chips and the surge voltage during switching. Our study is based on the CREE module CAS100H12AM1 (1200 V-100 A) which consists of 5 SiC MOSFET chips and 5 Schottky diodes in paralleled.

5.1.2. Thermal management

The self-heating, which elevates the device junction temperature (T_j), is a byproduct of the current that flows in the device during normal operation. Heat is generated within the device, and is then transferred to layers inside the package, is moved into the local ambient by heat sink. The heat

transfer is governed by the laws of thermodynamics and the principles of heat transfer [182]. The heat flow can take place by one or more of three fundamental mechanisms, as shown in Figure 5.4.

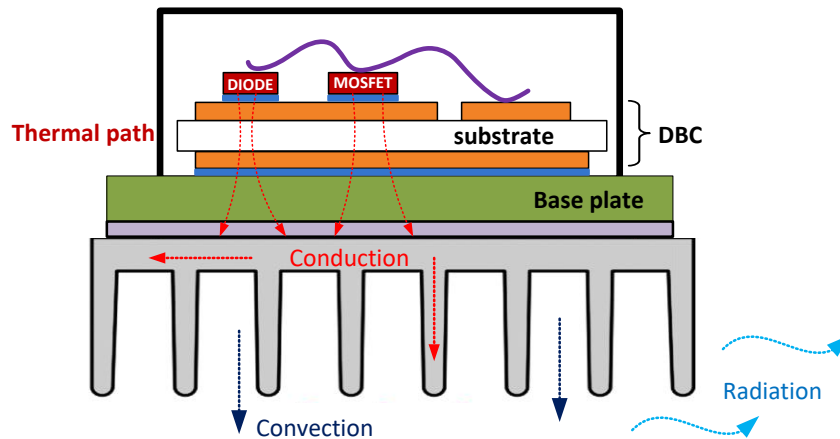


Figure 5.4. Heat transfer mechanisms in power device

In many respects, the junction temperature T_j strongly affects the device performance. The higher junction temperature, the more variation in electrical characteristic can affect the efficiency and the reliability of the device. Moreover, the higher temperature, the quicker lifetime can be reached by inducing mechanical stress or permanent damage, such as cracks in the solder joints, the wire-bonding separation, the gate oxide degradation, etc. Accordingly, the T_j must remain below the maximum temperature specified, which is generally around 150 °C.

At the component level, to preserve the junction temperature below the maximum allowed, the effective heat flow from the die through the package to the ambient is essential. Thus, the device heat transfer capability is an important aspect that is primarily fixed by the parameters of the layers inside the package [6, 180, 183, 184]. For thermal characteristics, it defines the important terms such as the impedance or thermal resistance that describes the heat transfer properties of package. By knowing the thermal characteristics of a package, one can calculate the T_j for a given power dissipation and its reference temperature. Hence, it provides the valuable thermal description inside the assembled package for development of thermal free-fault systems.

With advantages of SiC material, SiC MOSFETs are small size with the increasing power densities, producing higher junction temperatures. Thus, the SiC MOSFET thermal characterization becomes more and more crucial for the improvement of device performance and reliability, especially in high power applications.

5.2. Device electro-thermal characterization

5.2.1. Electrical analogy for thermal modeling

The propagation of heat from die to the heat sink is dominant by heat conduction mechanism which is similar to the conduction of electricity in conductor in many aspects [185-187]. Table 5.1 displays the thermal properties useful for thermal component model issues. The analogy between thermal diffusion and with electric diffusion is also exhibited.

THERMAL			ELECTRICAL		
Properties	Symbol	Unit	Properties	Symbol	Unit
Temperature	T	°C	Voltage	V	V
Heat flow	P	W	Current	I	A
Heat flux	J	W/m ²	Current density	J	A/m ²
Thermal resistance	R _{th}	°C/W	Resistance	R	V/A (Ω)
Thermal capacitance	C _{th}	J/°C	Capacitance	C	C/V
Amount of heat	Q _{th}	J=W.s	Charge	Q	C=A.s
Thermal conductivity	λ	W/ °C.m	Conductivity	σ	A/C.m
Temperature gradient	∂T/∂x	°C/m	Voltage gradient	∂v/∂x	V/m
Rate of temperature rise	∂T/∂t	°C/s	Rate of voltage rise	∂v/∂t	V/s

Table 5.1. Analogy between thermal and electrical phenomena

The heat flow through a plate with thickness d is proportional to a temperature difference from a hot surface T_1 to a cold one T_2 :

$$P = \lambda \times A \times \frac{T_1 - T_2}{d} \quad (5-1)$$

where A is the area of the surface to the heat flow. It is conceptually similar to the electrical resistance, in which heat flow and temperature difference are analogous to electric current and voltage difference, respectively. Therefore, the thermal resistance R_{th} refers to the ability of a material to resist to the heat transfer between two defined surfaces due to a temperature difference as:

$$R_{th} \equiv \frac{T_1 - T_2}{P} = \frac{d}{\lambda.A} \quad (5-2)$$

The temperature of an object will rise as heat flows into. The rate of the temperature increase dT/dt is proportional to the amount of heat transferred $P(t)$:

$$P(t) = C_{th} \cdot \frac{dT}{dt} \quad (5-3)$$

Following the analogies, the amount of heat stored can be equivalent to the electrical charge. The thermal capacitance C_{th} is a measure of the heat quantity stored by a material due to the temperature change, which is directly proportional to the mass m and the specific heat c_p of the material:

$$C_{th} = \frac{dQ}{dT} = c_p \cdot \rho \cdot A \cdot d = c_p \cdot m \quad (5-4)$$

where ρ is the density (kg/cm³) of the material. Figure 5.5 hereafter summarizes the electrical analogy commonly used for thermal modeling.

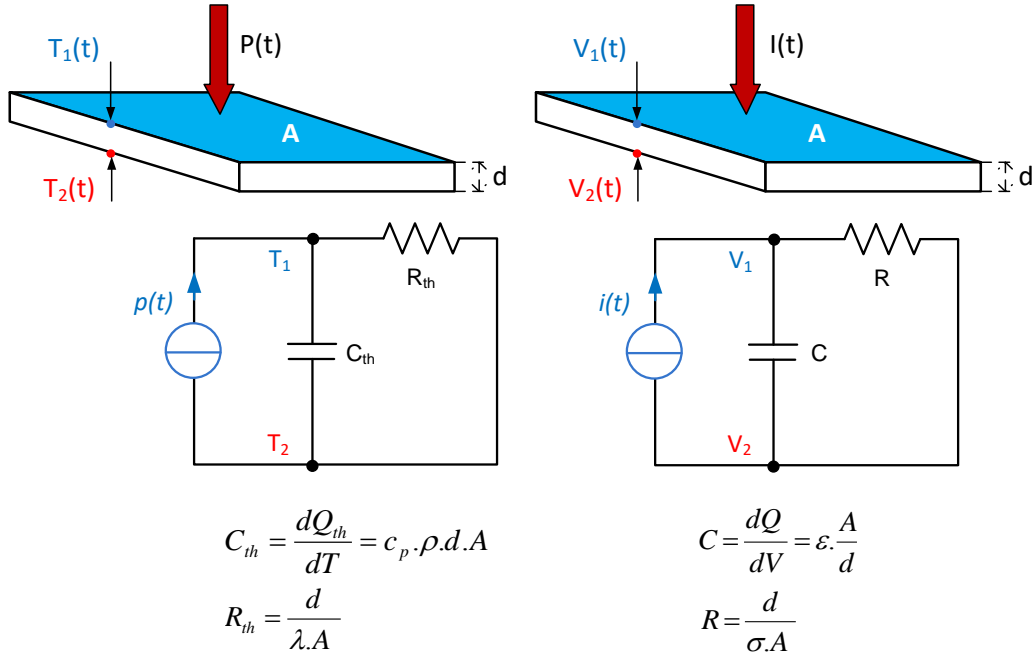


Figure 5.5. The equivalence between thermal and electrical quantities

5.2.2. Thermal equivalent circuit

The heat conduction path in a component is primarily considered as three-dimensional with spatial distribution of R_{th} and C_{th} . However, the thermal behavior of semiconductor device can be described using the thermal equivalent circuits where each physical layer within the device is described by R_{th} and C_{th} , either in the Cauer or the Foster networks [182, 185, 188].

The Cauer model, also known as T-model, ladder network or continued fraction circuit is an one-port electrical analogous network which results directly from the one-dimensional heat transfer equation [188, 189]. The thermal model is made up from the separate RC elements corresponding to a few selected points on the device, shown in Figure 5.6.

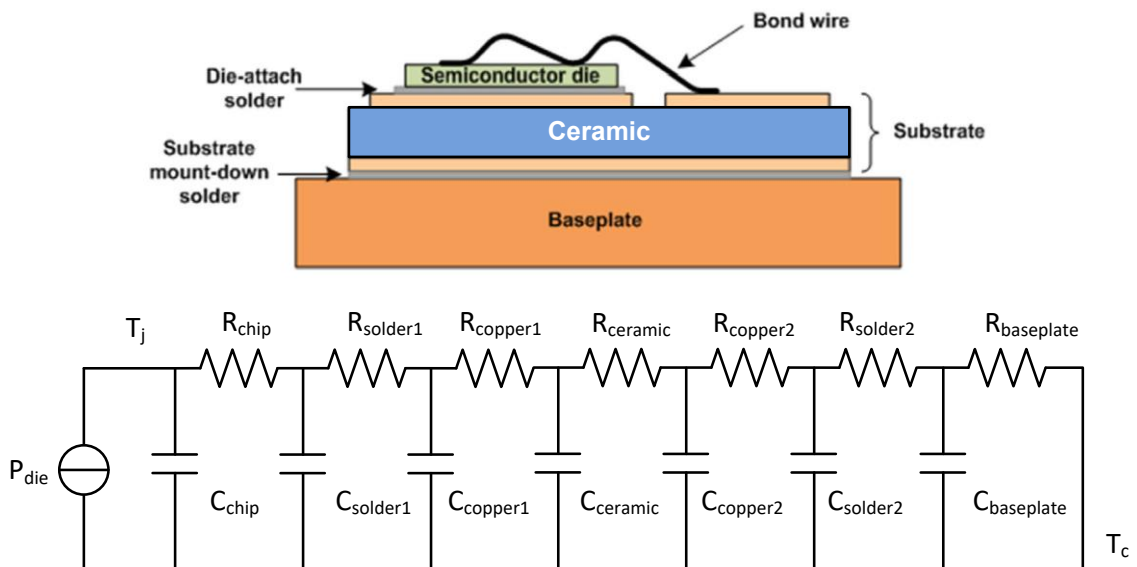


Figure 5.6. Cross-section layers and Cauer thermal model of semiconductor device

In the Cauer network, the voltage at each node has physical significance. It represents the temperature at a physical location (such as chip, DBC, base plate, etc.) of the device. The values of the RC in thermal equivalent circuit depend on the dimensions and the materials involved. Therefore, they are derived directly from the device structure, or with the use of special methods or algorithms.

Much simpler, a measurement-based equivalent circuit, called the Foster model, also known as Pi model, can be used. No design structure consideration is required, each layer in the MOSFET is merely represented by a RC cell. The cascade network is illustrated in Figure 5.7. Here, the current source P represents the power dissipation occurring in the device. The ground potential is equivalent to the ambient temperature. The subscripts j , c and a refer to junction, case and ambient respectively.

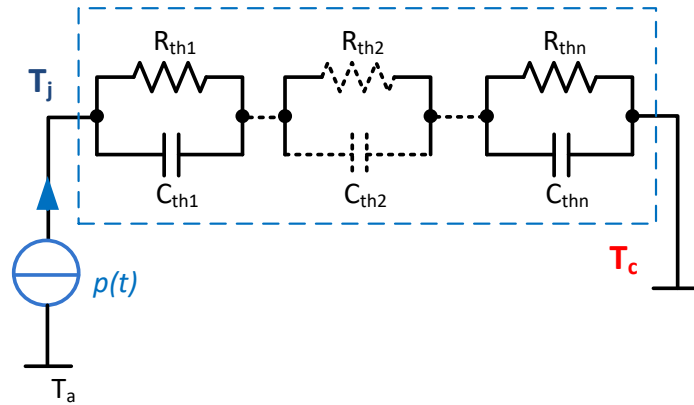


Figure 5.7. Foster thermal model of semiconductor device

The Foster model no longer describes the internal temperature distribution within device structure [188, 190]. However, the Foster has a simple mathematical form where the step response thermal impedance Z_{th} is given by:

$$Z_{th} = \sum_{i=1}^n R_{thi} \left(1 - e^{-\frac{t}{R_{thi}C_{thi}}} \right) \quad (5-5)$$

Since the junction temperature is interest rather than the exact internal temperature distribution, a Foster thermal equivalent circuit is used in datasheet. As a way of producing a simple model, its parameters are fitted from the measured response of a real component.

5.2.3. Thermal impedance

Due to the existence of capacitance, a step input of power results in thermal RC responses. The thermal impedance is a useful parameter to predict the junction temperature rise when pulse power is applied. Manufacturers usually provide empirical transient thermal curves. At each point, the maximum junction temperature is calculated as a function of time and the duty cycle of the rectangular power pulse in the component. As illustrated in Figure 5.8, the junction temperature rise is proportional to the power dissipated pulse due to self-heating. The thermal impedance depends on the duration t_p of pulse and the duty cycle D , as:

$$Z_{th} = \frac{1 - e^{-t_p/R_{th} \cdot C_{th}}}{1 - e^{-t_p/D \cdot R_{th} \cdot C_{th}}} R_{th} \quad (5-6)$$

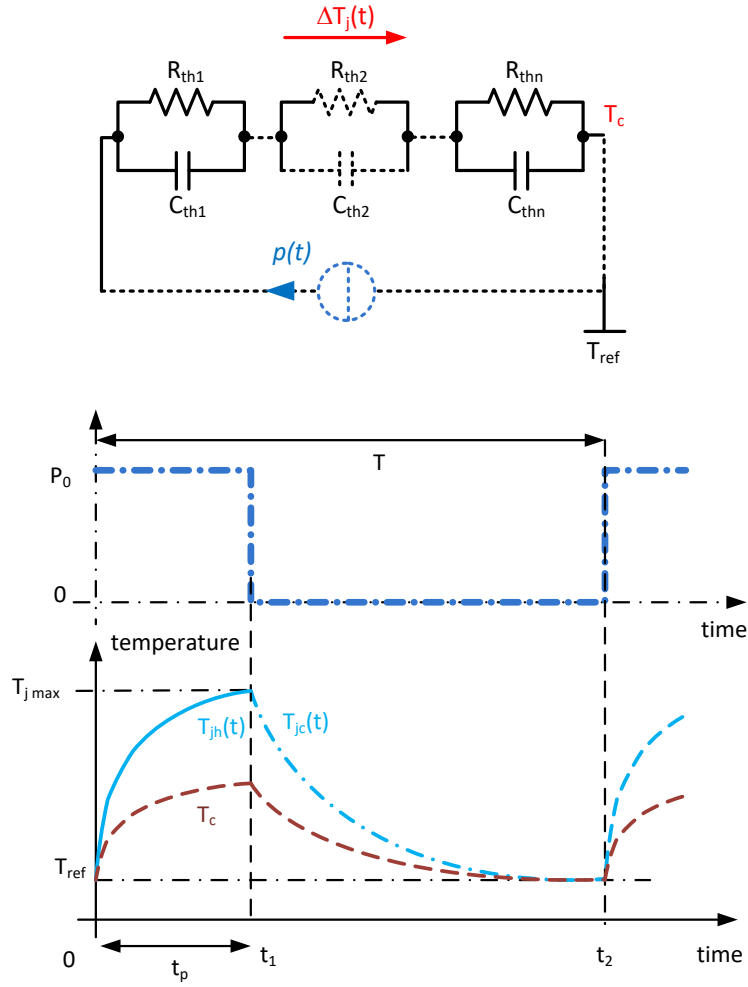


Figure 5.8. T_j vs. time for periodic pulse excitation of thermal impedance

Since the thermal capacitance is being charged to a different set of temperatures, it has a decisive influence on the Z_{th} for a short pulse width. Thus, the thermal impedance is called as the dynamic thermal resistance, which is affected by time of measurement. The temperature difference between junction temperature T_j (hotter site) and a predefined reference T_{ref} (colder place) is quantified as the Z_{th} in dynamic conditions. It is frequently cited as junction-to-reference $Z_{th(j-x)}$, where the reference point x can be the ambient air temperature, the component case or other well-defined reference site. In datasheets, transient response curves are often referenced to case of device.

5.2.4. Thermal resistance

When the heat capacitances existing between the two isothermal surfaces are no longer charging for a long period of pulse, their thermal stored energy is constant. The component temperature undergoes a heating transition toward the steady state equilibrium condition. Thermal impedance at thermal equilibrium is synonymous with thermal resistance. Similarly, the difference of the temperatures is equal to the product of the power losses and the thermal resistance R_{th} .

The thermal resistances within the device package are often defined by the selection of reference temperature sites:

- $R_{th(j-c)}$ stands for the resistance of heat flow paths from junction to case, which depends on the materials and the specific design of package.
- $R_{th(c-a)}$ includes thermal resistances for all heat paths from outside the package case to ambient.
- $R_{th(j-a)}$ is the thermal resistance from junction to ambient, which depends on the package, airflow, radiation, and heat sink system characteristics. It is often considered as the sum of the two previous ones:

$$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-a)} \quad (5-7)$$

Thus, $R_{th(j-c)}$ is always smaller than $R_{th(j-a)}$. Understanding of thermal resistances makes the knowledge of the working junction temperature of a device that is an important in design of the thermal management system.

For the packaged semiconductor device, $R_{th(j-c)}$ is crucial parameter in determining the reliability and performance of the device which is usually provided in datasheet for practical considerations. $R_{th(j-c)}$ the ability of heat dissipation from the surface of the die to a heat-sunk package surface, usually contact with a heatsink. $R_{th(j-c)}$ provides a simple and convenient means to determine the junction temperature with the environmental conditions and the component power dissipation. Thus, understanding of $R_{th(j-c)}$ is critical in designing a lighting system for maximum thermal performance.

5.3. Thermal resistance measurement

5.3.1. Principle of measurement

It is often measured by attaching the package surface directly to an infinite heat sink, i.e usually a liquid-cooled plate. $R_{th(j-c)}$ is measured by the traditional thermocouple measurement which needs the measurement of the junction temperature T_j , the case temperature T_c , and the power dissipation P . This method often produces wrong results since the measured temperature depends on the position of the thermocouple. Therefore, the method of transient measurements of the junction temperature that does not require the determination of the T_c has been used. The basic principle of measurement is described in [191].

The single pulse transient measurement consists of two phases including heating phase and cooling phase. During the heating phase, by applying a power step to the device, the T_j exponentially rises in response to the power step caused by the RC elements as shown in Figure 5.9. Then, Z_{th} corresponds to the thermal path between the junction and case, that is:

$$Z_{th(j-c)} = \frac{T_{jh}(t) - T_c}{P_0} = \frac{T_{jmax} - T_{jc}(t)}{P_0} \quad (5-8)$$

where T_{jh} and T_{jc} are temperatures of junction in heating and cooling down respectively, T_{jmax} is the steady-state junction temperature, T_c is the case temperature, and P_0 is the steady-state power dissipation.

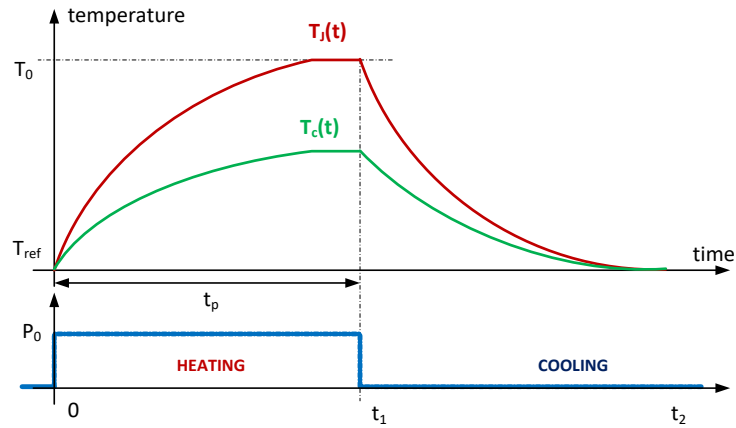


Figure 5.9. The transient thermal response for a single pulse

Since the power is conducted through the device until the thermal steady state is reached; both the junction temperature T_j and the case temperature T_c are increased. The ambient temperature T_a is considered as the reference temperature. Typically, the $R_{th(j-a)}$ can be measured either at the end of the heating phase, or at the early beginning of the cooling phase that follows. However, the cooling curve technique is, in fact, generally more suitable to determine $R_{th(j-a)}$ [185, 191, 192]. The thermal resistance is defined at thermal equilibrium:

$$R_{th(j-a)} = \frac{T_j - T_a}{P_0} \quad (5-9)$$

Here, the key of thermal resistance measurement is the determination of T_j , which cannot be measured directly.

5.3.2. Estimation of junction temperature

There are several ways to estimate the T_j including optical, physical contact and electrical methods, some of which are more applicable than others. The comparison between those methods has been addressed in the literature [193-197]. Among these methods, the electrical method for junction temperature measurement, also known as thermo-sensitive electrical parameter (TSEP), is by far the most widely used today. It can indirectly estimate temperature without any physical modification of the power device structure. The general principle is to measure an electrical parameter that changes over temperature to estimate the inner temperature T_j . TSEP displays a sufficiently high sensitivity and accuracy. The estimated T_j using TSEP is termed "average" temperature over the device but is very close to the temperature measured via infrared camera which enables an accurate mapping of the temperature. Moreover, the measured temperature can vary when using different indicator as a TSEP [132, 194, 195, 197-199].

5.3.3. Identifying the TSEP

The TSEP is based on a temperature dependency of a device parameter that can be measured via a current or voltage. The characteristics of an ideal TSEP consist of:

- Highly sensitive: high sensitivity can be described in terms of high ratio of voltage change to temperature which results in reduction of noisy data and thus accuracy improvement.

- Noninvasive: being a temperature indicator, the semiconductor temperature is not affected by the measurement technique.
- Uniform: the TSEP relationship to temperature is uniformly used for lot of identical devices without performing the calibration for every individual DUT.
- Linear: the TSEP is ideally a linear or nearly linear function of temperature.

5.3.4. Principle of TSEP

To determine the junction temperature, the TSEP of the component is used as a temperature sensor due to its quasi-linear temperature dependence. Prior to using the TSEP, calibration and power cycling are mandatory.

a. The calibration

Once a TSEP has been chosen, the device calibration process is performed to obtain the relationship between the TSEP and temperature. It involves forcing the semiconductor to known temperatures and then measuring the TSEP at these temperatures. Typically, a thermal chamber or a heat sink can be used in this procedure. The calibration power P_c applied in the device should be kept as low as possible to avoid any significant self-heating.

For example, when a small calibration current I_c (sometimes also referred as sense current) is applied across the body diode, a nearly linear relationship between forward-biased voltage drop (V_F) and temperature is obtained, as illustrated in Figure 5.10. In this case, V_F is the TSEP.

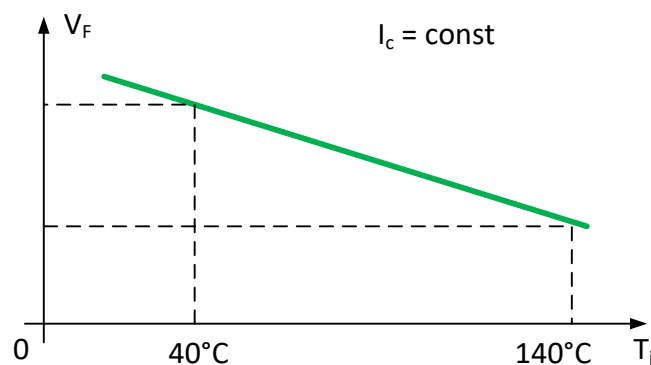


Figure 5.10. Approximation of V_F and temperature range

This calibration step can be time-consuming, depending on the number of calibration points, the time required for heating the power module to the desired temperatures, and the variability of the TSEP between each device. Since the stability of TSEP with power module age is considered, the recalibration may therefore be required.

b. The power dissipation cycling

There are 2 phases, namely the heating up and cooling down. In the heating phase, the junction temperature of the device rises due to the power self-heating P_h . After thermal stabilization, P_h is turned-off, the V_F is recorded (or any TSEP) as soon as the cooling down starts. The junction temperature is then deduced from the calibration curve.

Cooling is frequently preferred for temperature measurement, firstly because TSEP are often of better reliability under low calibration currents, secondly because turning-off the self-heating power corresponds to an actual power step, so that the cooling phase enables to obtain not only the thermal resistance, but also more generally the thermal step impedance.

5.4. Calibration for SiC MOSFET electro-thermal characterization

5.4.1. Selection of TSEP for SiC MOSFET

With traditional silicon MOSFETs, the most frequent TSEP are namely the body diode forward voltage V_F , on-resistance $R_{DS(ON)}$ and threshold voltage V_{TH} [131, 193, 198]. However, the SiC MOSFET exhibits some peculiarities. A trustworthy TSEP for SiC MOSFETs has been discussed in [199-202].

The V_F of body diode decreases at a constant rate with rising temperature at low constant current, which can be used to estimate junction temperature. To avoid any error in the temperature estimation, the channel must be completely opened (no conduction), so that a constant current through the body diode is guaranteed. However, it is well known that trapped charge carriers affect the channel of SiC MOSFETs, which leads to a variation of the threshold voltage V_{TH} . Therefore, a reliable gate voltage is required to ensure that the channel is in off-state. For example, the channel is totally opened with $V_{GS} = -6$ V at 25 °C, with -4 V at 125 °C [37, 131, 198, 203]. Particularly, the DUT is structured as a module with a Schottky diode in paralleled with body diode. Thus, using V_F as TSEP is not reliable option to estimate the junction temperature for this SiC MOSFET module.

Threshold voltage is often proposed as a TSEP to estimate T_j during device switching because of its high negative temperature coefficient [199, 204]. However, V_{TH} of SiC MOSFET is low. Due to the interface traps, SiC MOSFET exhibits extra difficulties, indeed the V_{TH} fluctuates for the applied gate bias. The change of V_{TH} over temperature is a rather nonlinear function when compared to silicon MOSFETs [201].

From a physical viewpoint, the heat rise should be measured as close as possible to the junction. In on-state, the current flows from drain to source, via N-drift layer and channel, represented by $R_{DS(ON)}$. V_{TH} is sensitive to the channel temperature while the body diode forward voltage is rather sensitive to the N-drift area temperature, and $R_{DS(ON)}$ (through both R_{CH} and R_{DRIFT}) is the most sensitive parameter to the junction temperature [132]. In addition, $R_{DS(ON)}$ can be easily inferred from measured current and voltage. Therefore, $R_{DS(ON)}$ is chosen for this work. However, $R_{DS(ON)}$ of SiC MOSFET has quadratic relationship with temperature. Thus, obtaining the temperature from this relationship can be a challenging task. Moreover, $R_{DS(ON)}$ of SiC MOSFET is less sensitive than for Si devices. Consequently, using $R_{DS(ON)}$ as indicator of junction temperature requires more accurate sensing technology and an appropriate small gate bias.

5.4.2. Calibration

Using $R_{DS(ON)}$ as a TSEP requires a calibration current I_c , then a relation between V_{DS} and temperature is obtained. This section describes the different steps to perform the calibration sequence.

a. Selection of the calibration current level

The calibration current I_c is required to be small to avoid any significant self-heating. In such a way, the junction temperature remains equal to the reference temperature (i.e. case temperature). However, I_c should be high enough for good V_{DS} resolution (measurable with the voltmeter and

recordable on the oscilloscope), and for greater sensitivity (dV_{DS}/dT is proportional to I_c). From the output characteristics of SiC MOSFET, the $R_{DS(ON)}$ temperature coefficient depends on both junction temperature and gate voltage. Positive coefficients are obtained for high gate bias (higher than 16 V) and negative coefficients for lower values. A much better sensitivity is obtained for low gate voltages (cf. Figure 5.12). Therefore, V_{GS} is chosen sufficiently low so that $R_{DS(ON)}$ constitutes a sensitive TSEP all over the temperature range (from 0 °C up to 150 °C).

b. Establishment of thermal equilibrium

For TSEP calibration, the component is immersed in a stable temperature environment. Since the power dissipation caused by calibration power is insignificant, the junction temperature is determined by thermal environment of the thermal chamber. Due to the heat capacitances existing within the module, the thermal transient response should be complete prior monitoring $R_{DS(ON)}$. The temperature distribution of the component is assumed to be homogeneous. In thermal equilibrium with its surrounding environment, the junction temperature is considered to be equal to that of the package case ($T_j = T_c$).

c. Measurement

Once the thermal steady state is reached, V_{DS} corresponding to the TSEP is measured for a given gate voltage. The calibration curve, i.e. $V_{DS} = f(T_j)$ at constant I_c and V_{GS} , is obtained by repeating the procedure for various environment temperatures. Figure 5.11 presents the calibration curves obtained for a MOSFET device of a SiC module CAS100H12AM1. The calibration current I_c is set to 1 A. MOSFET gates are biased at +7 V, +8 V, +9 V and +10 V. Drain voltages are measured by voltmeter at each step of 10 °C between 0 °C and 150 °C. It can be seen that the relationship between drain voltage and temperature is more sensitive at low gate voltage (more than 5 mV/K below 30 °C, and still 1 mV/K within the interval [60 °C, 90 °C]), but quite non-linear in the whole temperature range. The linearity of the curve is significantly better at higher gate bias but clearly less sensitive.

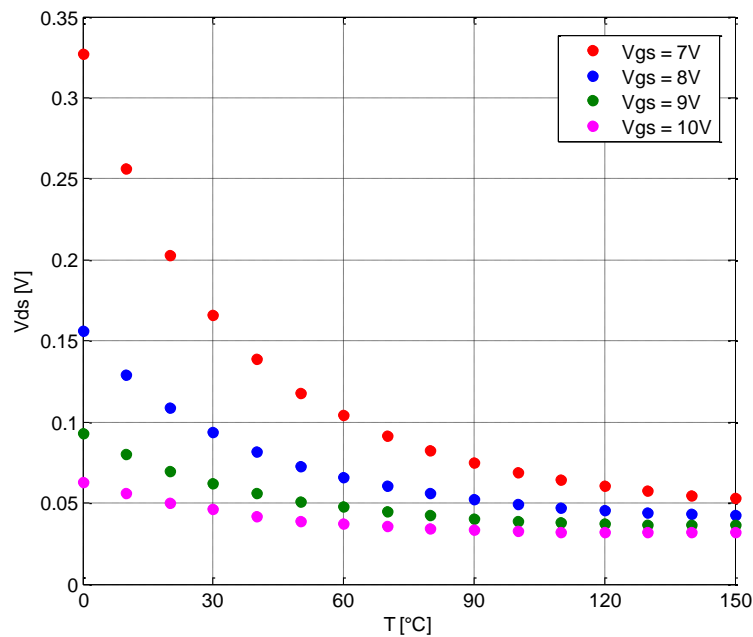


Figure 5.11. The calibration curves of 1200 V-100 A SiC MOSFET (CAS100H12AM1) at $I_c = 1$ A.

We will make use of the calibration curve obtained at $V_{GS} = 7\text{ V}$, because of its quite significant sensitivity. However, for certain reasons that will be detailed further on, a different calibration curve will be also required, under in-situ thermal conditions. Here, the temperature of the MOSFET module is fixed by means of a fluid-cooled plate (instead of a climatic chamber) on which the module is screwed. A fluid-flow regulator CORIO CD-300F is used to flow water through the heat sink, and to control water temperature. To avoid thermal exchange with the ambient, the component is placed in an adiabatic box. Two thermocouples associated with a dual thermometer RS 1314 measure the water temperature at both inlet and outlet of the heat sink, which enables to check if the system (component and heat sink within the adiabatic box) has reached its thermal steady state, and also if there is actually no heat exchange between the system and the ambient. Then, the component temperature is supposed to be equal to the water temperature. Figure 5.12 presents the calibration curve obtained for a MOSFET device of a SiC module CAS100H12AM1, at 100 mA for I_c and 7 V for V_{GS} . As foreseen, the TSEP sensitivity is lower than previously, from about 0.3 mV/K under 30 °C to less than 0.1 mV/K within [60 °C, 80 °C].

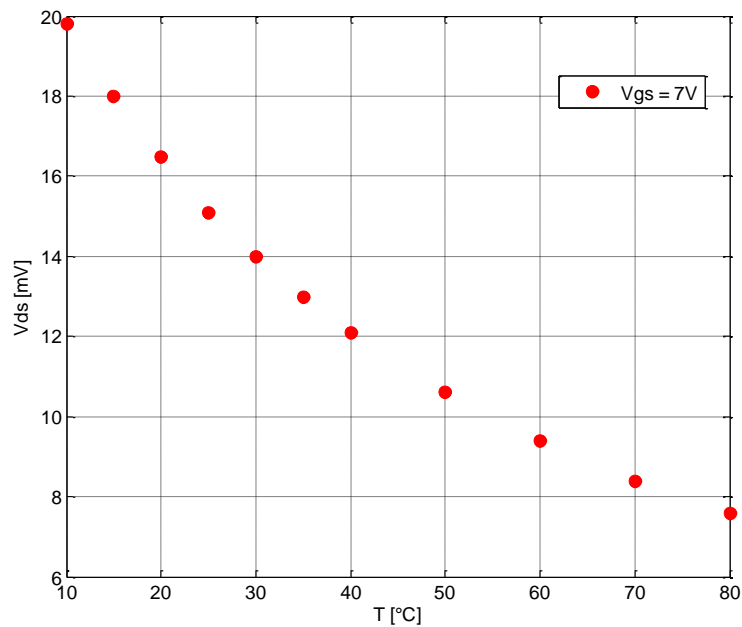


Figure 5.12. The calibration curves of 1200 V-100 A SiC MOSFET (CAS100H12AM1) at $I_c = 100\text{ mA}$

5.4.3. Discussion

Since the calibration data is not sufficiently linear, the junction temperature can be determined by means of a linear piecewise interpolation, based on calibration points. Nevertheless, a problem arises, linked to the nature of the TSEP. As far as the calibration is carried out at low gate voltage (to obtain sufficient sensitivity), the measured drain voltage is mainly due to the voltage drop in channel. Consequently, its reproducibility is not guaranteed, because of phenomena linked to trapped charges. In particular, repeating the calibration procedure on the same component at different periods of time may lead to different calibration curves; parallel one to another due to an offset.

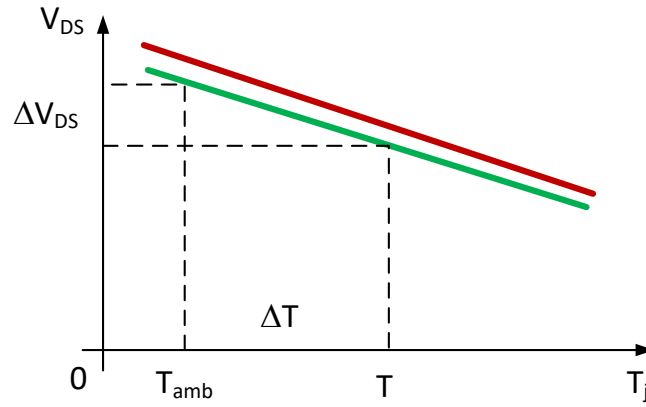


Figure 5.13. Multiple junction calibration curves

Therefore, to extract junction temperature from V_{DS} measurement, a specific calibration point is required, in addition with the shape of the calibration curve. Since the ambient temperature is known, the associated TSEP value is measured, which enables to evaluate the offset to be taken into account. Then, temperature difference ΔT can be estimated by measuring the drain voltage difference ΔV_{DS} , using the calibration curve shape as illustrated in Figure 5.13.

5.5. Measurement of the self-heating thermal resistance

5.5.1. Principle and experimental setup

The principle of the self-heating thermal resistance (or impedance) estimation basically consists in monitoring the component junction temperature during the cooling phase until thermal equilibrium, after a self-heating phase during which the DUT has conducted a high current until thermal steady state. The schematic of the experimental setup is shown in Figure 5.14. It is composed of:

- a DC power supply which provides the high level current I_h during the self-heating phase. Here, a linear power supply has been used (namely a bidirectional Höcherl & Hackl NL1V8C80 source-sink, voltage range: - 1 V to 8 V, current range: ± 80 A), to avoid noises generated by classical switch-mode power supplies,
- a pilot switch S_h , to turn-on or turn-off the heating phase. It is realized by means of two paralleled 300 A IGBT,
- a linear DC power supply (programmable power supply HM7044) which provides the calibration current I_c during the cooling phase, through a diode D to avoid any reverse current across the power supply,
- a fluid-cooled heat sink on which the DUT is screwed, associated with a thermostatic water bath CORIO CD-300F,
- a dSPACE real time card, carried out in combination with ControlDesk® software and Matlab-Simulink® mathematical environment, for the synchronized generation of both S_h and DUT gate signals. A standard driver is used for S_h , with however an unusual gate resistance at turn-off (1 k Ω), to enable slow commutation and then avoid inductive overvoltage. A specific electronic card is employed for the interface between the dSPACE card and the DUT gate, in

order to drive the component with two gate bias levels, V_{GSH} during heating phase and V_{GSL} during cooling phase (typically 20 V and 7 V, respectively).

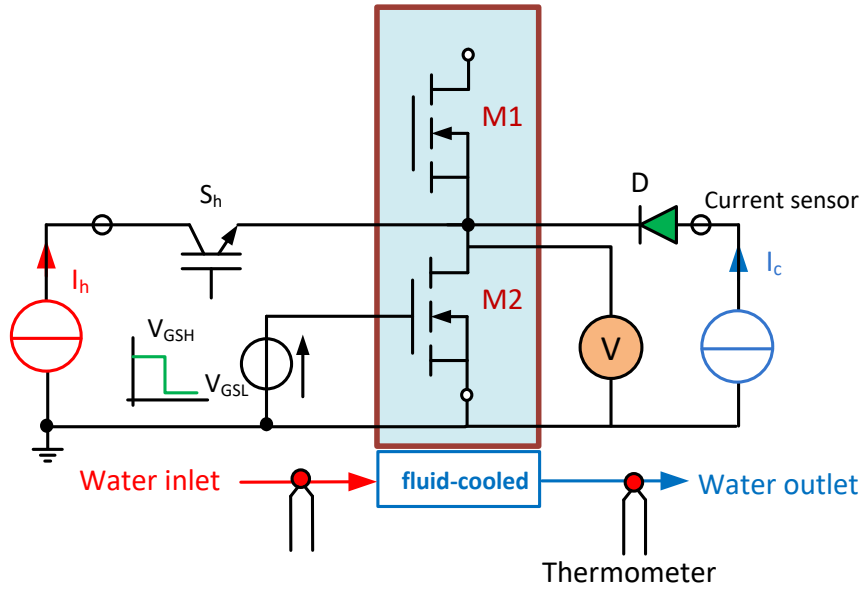


Figure 5.14. Circuit diagram of the measurement setup

As can be seen in Figure 5.15, the DUT and its heat sink are placed in an adiabatic box. Water temperature is measured at both inlet and outlet of the heat sink, by means of a dual thermometer RS 1314. For waveform measurements, an oscilloscope TDS5034B is used, coupled with a current probe TCP303 associated with an amplifier TPCA300 for the heating current, with an ADA400A differential probe for DUT drain voltage, and an ISOL 710 differential probe for DUT gate voltage.

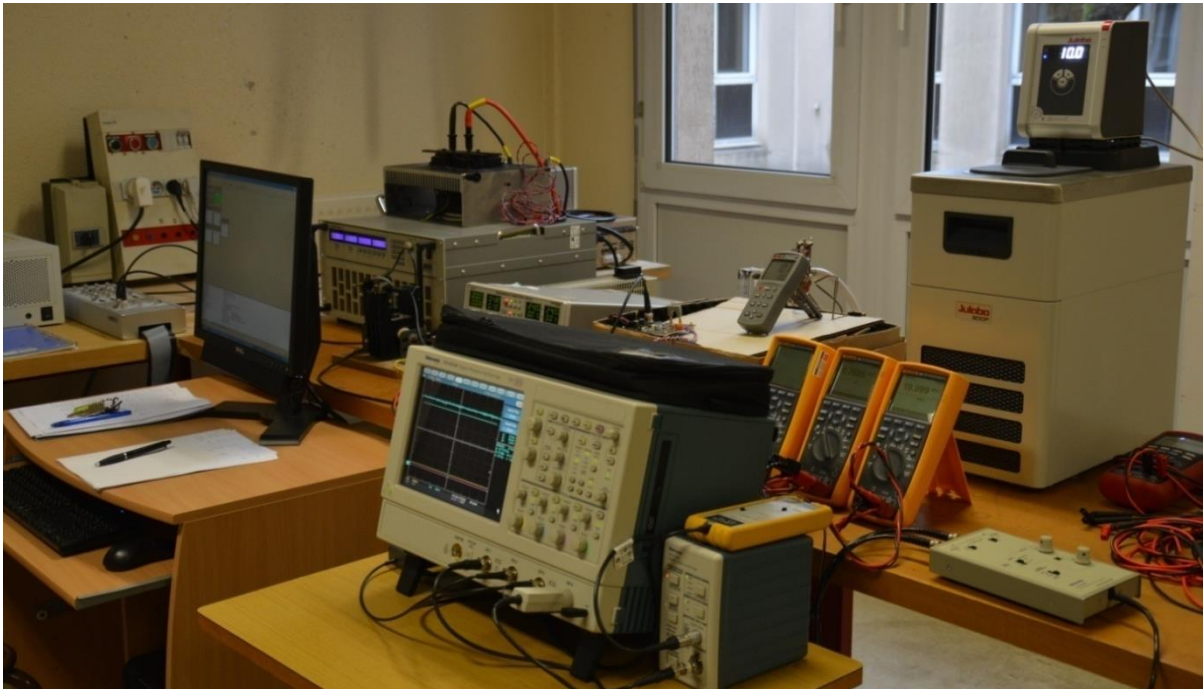


Figure 5.15. Experimental test bench

In fully on-state ($V_{GS} = 20$ V), the SiC MOSFETs operates in the ohmic region with $R_{DS(ON)}$ close to the value specified by the manufacturer, i.e. 16 m Ω . Therefore, the heating current I_h should be large enough to achieve a substantial self-heating. In this work, a current I_h up to 80 A (the DUT rated current is 100 A) can be applied. Thus, the power dissipated in the DUT can be set to a level close to the expected conduction losses at full load.

The gate bias is set to the high level $V_{GSH} = 20$ V to allow significant channel conduction. The low level of gate bias $V_{GSL} = 7$ V is only applied during the cooling phase. As already mentioned, the commutation between these two levels is synchronized with the pilot switch state: V_{GSH} when S_h is turned on, V_{GSL} when S_h is turned off. The experiment is conducted at a given ambient temperature which is determined by setting the temperature of the fluid-cooled plate.

5.5.2. Experimental procedure

T_{amb} is set at 10 °C, $I_c = 1$ A flows through the DUT. At the thermal steady-state, the temperature sensors at the inlet and the outlet of the heat-sink indicate the same value. V_{DS} is measured by means of a multimeter, and is also recorded via the oscilloscope, both value are referred as $V_{DS(0)}$. The heating period ($[0, t_1]$ in Figure 5.16) involves turning the DUT in fully on-state with a high gate voltage V_{GSH} , and simultaneously turning on S_h so that a high current I_h flows through the DUT, in addition with the calibration current: $I_D = I_h + I_c$. Junction temperature increases due to self-heating. It changes the $R_{DS(ON)}$ value and thus leads to a slow V_{DS} evolution, up to (or down to, depending on V_{DS} temperature coefficient, which is generally positive at $V_{GS} = 20$ V) a constant level, which indicates that thermal equilibrium is reached.

The greater the thermal capacitance, the longer the transition time required for the onset of thermal equilibrium. In this work, the width pulse for heating up is chosen to $t_1 = 25$ minutes, which is long enough to obtain steady state in heating phase. Before ending this phase by turning off S_h , the DUT drain voltage is measured (level $V_{DS(25-)}$ in Figure 5.16) with a multimeter, in order to estimate the power dissipation within the device as:

$$P = I_D \times V_{DS(25-)} \quad (5-10)$$

At S_h switch-off, the DUT gate voltage is changed to V_{GSL} . This starts the measurement phase during cooling down, under $I_D = I_c$. The drain voltage is recorded with the oscilloscope; it rises while the junction cools down, from $V_{DS(25)}$ to $V_{DS(0)}$ (cf. Figure 5.16). The voltage difference due to the change of temperature during the heating phase is expressed as:

$$\Delta V = V_{DS(0)} - V_{DS(25)} \quad (5-11)$$

Since the DUT is biased in the same conditions than for calibration step, the junction temperature increase ΔT can be deduced from this voltage difference using the calibration curve. As the temperature rise in the device is entirely due to its own dissipation, the self-heating thermal resistance can be deduced as:

$$R_{th} = \frac{\Delta T}{P} \quad (5-12)$$

At last, after switching off the heat source for 30 minutes, the thermal equilibrium is reached at time $t = t_2$. Then, V_{DS} is captured as $V_{DS(55)}$, in order to verify if this level is equal to $V_{DS(0)}$. Afterwards, the second method of junction temperature estimation is proceeded, by increasing the water temperature of heatsink until the same voltage difference ΔV is obtained. The procedures have been conducted for three I_h values (60 A, 70 A, and 80 A), and for two I_c values (1 A and 100 mA).

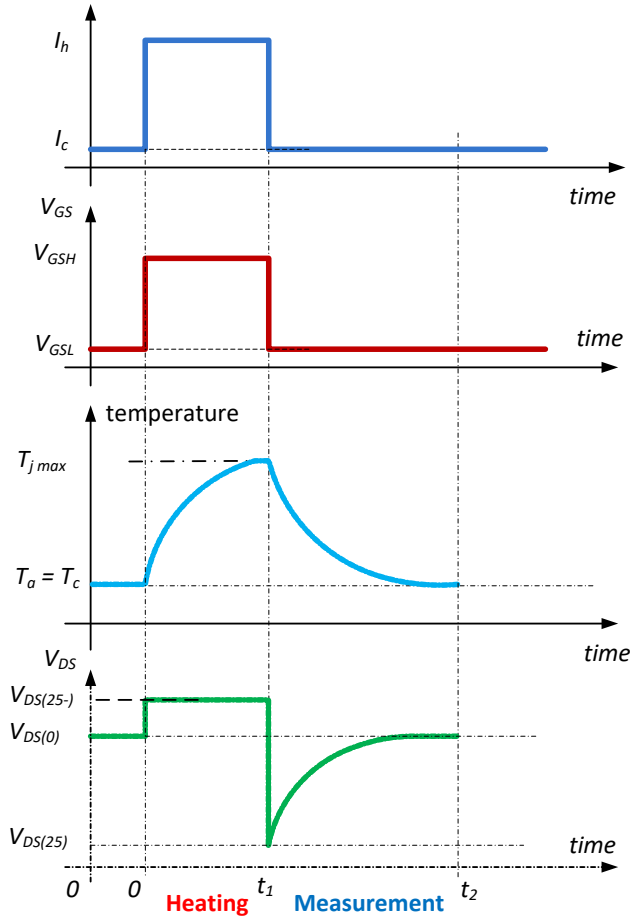


Figure 5.16. Time diagram of self-heating measurement method

5.5.3. Results and discussion

As mentioned above, the temperature measurement should be started as soon as the DUT drain current is switched from I_h to I_c . However, in practice, the calibration current is disturbed by the transition. Figure 5.17 presents waveforms obtained after the commutation between heating and cooling phases: I_c in yellow (CH1), V_{GS} in purple (CH3), and V_{DS} in blue (CH2). It can be first observed that V_{GS} and I_h commutations are correctly synchronized. Nevertheless, the interconnected parasitic impedance between the power supply and the device causes transient response of the current source used for I_c generation. As a result, the disturbance observed on calibration current introduces a delay time of some milliseconds (at $I_c = 1$ A) on TSEP measurement, and therefore a little error on junction temperature estimation.

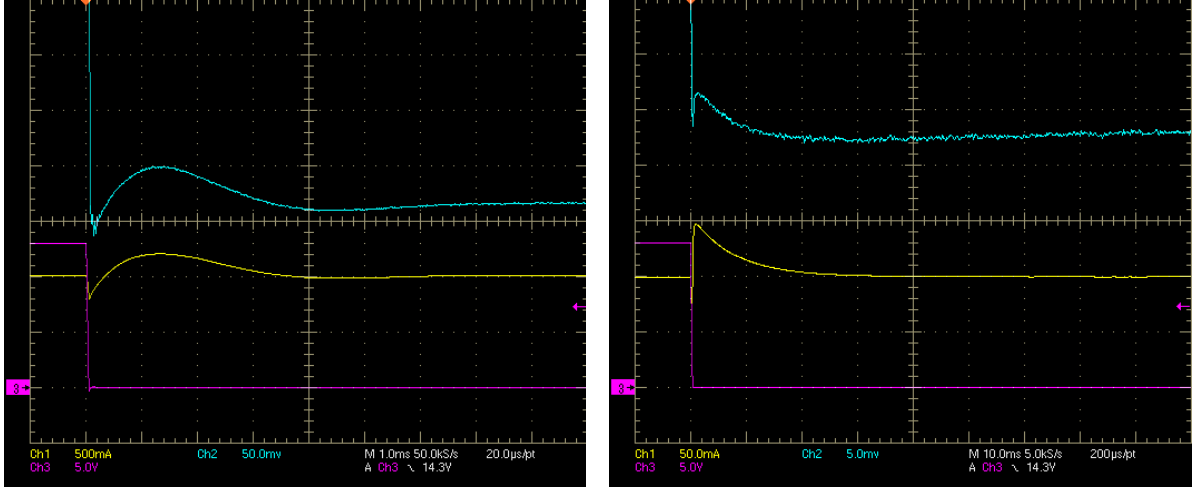


Figure 5.17. Measured waveforms obtained after the heating switching off. On left: $I_c = 1$ A and $I_h = 70$ A. On right: $I_c = 100$ mA and $I_h = 80$ A. CH1: calibration current, CH2: drain voltage, CH3: gate voltage ($V_{GS} = 7$ V).

Table 5.2 and Table 5.3 hereafter summarize experimental results for various heating currents, at $I_c = 1$ A and $I_c = 100$ mA, respectively. The junction temperature T_{cal} is obtained by means of the calibration curve, whereas T_{mes} is evaluated according to the second method (increase of the water bath temperature). Thermal resistances $R_{th(cal)}$ and $R_{th(mes)}$ are calculated according to equation (5.12), using T_{cal} and T_{mes} respectively.

I_h (A)	$V_{DS(0)}$ (mV)	$V_{DS(25-)}$ (V)	$V_{DS(25)}$ (mV)	$V_{DS(55)}$ (mV)	T_{cal} (°C)	$R_{th(cal)}$ (°C/W)	T_{mes} (°C)	$R_{th(mes)}$ (°C/W)
60	273	0.9583	188	256.3	30.5	0.351	31.2	0.363
70	278	1.1466	160	281	44.3	0.421	44.3	0.421
80	270	1.3589	130	276	57.3	0.430	62.0	0.472

Table 5.2. Data for $I_c = 1$ A, $T_a = 10$ °C

I_h (A)	$V_{DS(0)}$ (mV)	$V_{DS(25-)}$ (V)	$V_{DS(25)}$ (mV)	$V_{DS(55)}$ (mV)	T_{cal} (°C)	R_{th} (°C/W)	T_{mes} (°C)	$R_{th(mes)}$ (°C/W)
60	29.3	0.9422	24.8	29.0	24.4	0.254	24.0	0.247
70	29.5	1.1289	23.5	30.0	31.0	0.265	30.9	0.264
80	30.0	1.3384	22.3	30.8	40.0	0.280	39.5	0.275

Table 5.3. Data for $I_c = 100$ mA, $T_a = 10$ °C

It can be pointed out that for a given calibration current, results obtained for thermal resistances are quite similar, what is to be credited to the measurement method. However, a singular point appears in Table 5.2, at $I_h = 60$ A, for which it can also be observed a great difference between $V_{DS(0)}$ and $V_{DS(55)}$. As a reminder, these two drain voltage levels theoretically represent the same temperature (the ambient temperature, in this case). In the absolute, the measurement method is quite not satisfying. At low calibration current, results are not reliable, because of a too poor sensitivity of the TSEP. At higher calibration current, here $I_c = 1$ A, an unexplained phenomenon interferes with the measurement. Figure 5.18 presents waveforms obtained when commutating the DUT gate voltage from 20 V to 7 V, the DUT being flowed by the only calibration current. Ideally for the measurement method, a simple voltage step should be observed on V_{DS} , from $V_{DS}(V_{GS} = 20$ V, $T_j = T_a)$ to $V_{DS}(V_{GS} = 7$ V, $T_j = T_a)$. It is clearly not the case. Indeed, the drain voltage obtained immediately after the

transition is significantly higher than the one corresponding to ambient temperature, i.e. $V_{DS}(V_{GS} = 7 \text{ V}, T_j = T_a)$. In the present case, the overvoltage is 48 mV, which represents a measurement error of 6 °C. Furthermore, this steady state level is reached, but only after a long electrical transient (about 100 s).

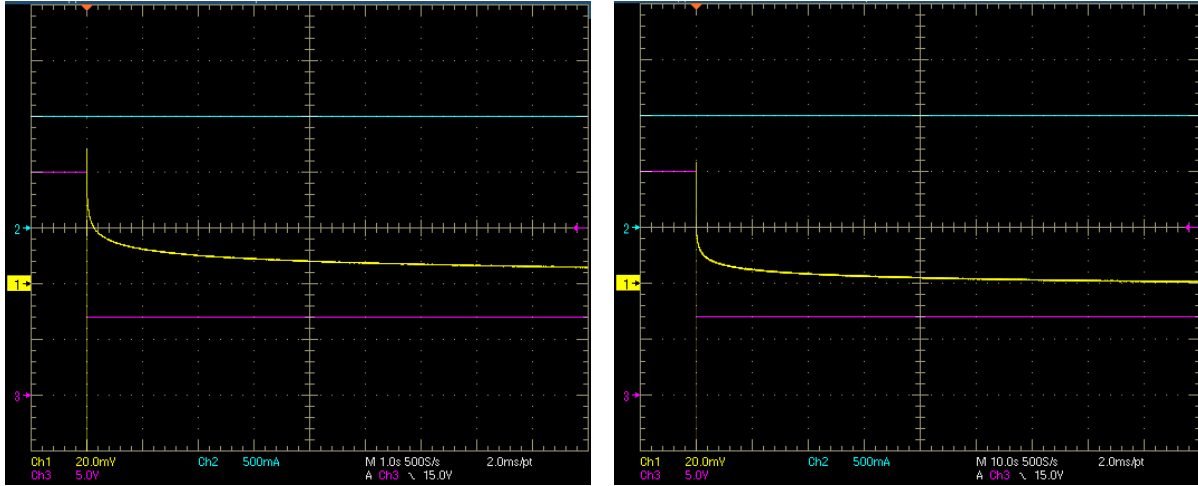


Figure 5.18. Measured waveforms obtained for $I_c = 1 \text{ A}$ at ambient temperature ($T_a = 10 \text{ °C}$), after V_{GS} transition from 20 V to 7 V. CH1: drain voltage variation (i.e. $V_{DS} - V_{DS}(I_c = 1 \text{ A}, T_a = 10 \text{ °C})$), CH2: calibration current, CH3: gate voltage. On left: 1 s/div, on right: 10 s/div.

As a conclusion, the measurement method is a little problematic, when directly applied to the estimation of self-heating thermal resistance. This is why we propose in the following to apply it in a different and indirect way.

5.6. Measurement of the mutual thermal resistance

5.6.1. Thermal phenomena in a multichip structure

In high power MOSFET modules, chips are situated closely to each other. Each chip generates heat that flows through multiple layers inside the package. As a result, chips within a module are thermally coupled, whether by the upper side of the DBC (for chips soldered on the same copper layer), or by the insulation layer of the DBC and/or the case, or even by the heat sink. These thermal interactions, referred in the following as mutual thermal couplings, give rise to supplemental warm-ups, in addition to those due to self-heating, which can be represented by mutual thermal resistances in steady state (or mutual thermal impedances, in transient).

For example, a power module has two MOSFETs, the temperature of each MOSFET can be written in steady state as the combination of a self-heating term, due to the dissipation within the chip, and a thermal coupling term, due to the dissipation within the other chip [184]:

$$\begin{aligned}\Delta T_1 &= R_{th1} \times P_1 + R_{th12} \times P_2 \\ \Delta T_2 &= R_{th21} \times P_1 + R_{th2} \times P_2\end{aligned}\tag{5-13}$$

where P_k is the power dissipated in chip k , ΔT_k is the temperature increase of chip k , R_{thk} is the self-heating thermal resistance of chip k , and $R_{th12} = R_{th21}$ (according to the superposition theorem) is the mutual thermal resistance between chips 1 and 2.

5.6.2. Experimental setup and measurement procedure

The schematic of the measurement setup is shown in Figure 5.19. To estimate the coupling thermal resistance between the DUT (M2 in Figure 5.19) and the second MOSFET (M1 in Figure 5.19) of the CAS100H12AM1 module, we proceed as previously by heating the DUT with a high level current I_h , its gate being biased at 20 V. The thermal effect on the second component is measured continuously, by means of its TSEP carried out with a calibration current $I_c = 1$ A and a gate voltage set at 7 V. It is quite the same as previously, except for the calibration circuit, which is connected to M1, and for the DUT gate voltage which can be maintained at a constant level.

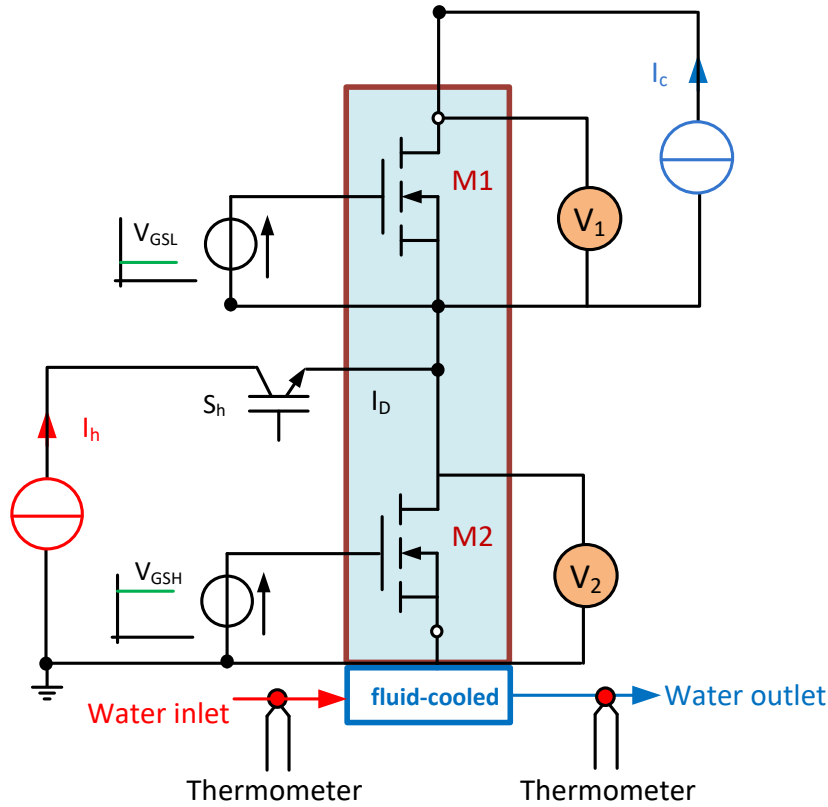


Figure 5.19. Circuit diagram of thermal coupling measurement

The ambient temperature is set at 10 °C. Since the temperatures of the inlet and the outlet of the heat-sink are equal, the system has reached the thermal equilibrium. V_{DS1} is measured with a multimeter, the value is referred as $V_{DS1(0)}$. Then, the heating period is started by turning on the pilot switch S_h . Junction temperatures of M1 and M2 increase, leading to a slow increase of V_{DS2} and a slow decrease of V_{DS1} (under gate biases mentioned before, the temperature coefficient of $R_{DS(ON)}$ is positive for M2, and negative for M1). Thermal equilibrium is reached when both V_{DS1} and V_{DS2} become constant, referred as $V_{DS1(25)}$ and $V_{DS2(25)}$, respectively (the index 25 is used, because as previously, the heating phase is maintained during 25 minutes). The power dissipation of the DUT is calculated as:

$$P_2 = I_h \times V_{DS2(25)} \quad (5-14)$$

The voltage difference due to the change of M1 temperature during the heating phase is expressed as:

$$\Delta V_1 = V_{DS1(0)} - V_{DS1(25)} \quad (5-15)$$

The junction temperature increase ΔT_1 is then deduced from this voltage difference, using the calibration curve established for M1. Finally, the mutual thermal resistance is evaluated according to:

$$R_{th12} = \frac{\Delta T_1}{P_2} \quad (5-16)$$

Afterwards, S_h is switched off, and after 30 minutes, V_{DS1} is measured as $V_{DS1(55)}$, in order to verify if this level is equal to $V_{DS1(0)}$. Then, a second junction temperature estimation is as previously proceeded, by increasing the water bath temperature until $V_{DS1(25)}$ is obtained. This procedure has been conducted for four I_h values (50 A, 60 A, 70 A, and 80 A).

5.6.3. Results and discussion

The thermal coupling measurement method presents some advantages, compared to the self-heating measurement one. Firstly, as the calibration current does not flow through the DUT, no commutation is required for junction temperature measurement, which can therefore be carried out without electrical perturbation induced by I_h turn-off on calibration current. Secondly, as M1 stays in the same operating regime, one may expect that its gate structure (notably its quantity of trapped charges) is not modified during heating phase. As a result, we have observed a quite fine reproducibility, with $V_{DS1(55)}$ nearly equal to $V_{DS1(0)}$ for all I_h values. Table 5.4 summarizes experimental results. The index "cal" means that M1 junction temperature measurement is carried out by means of the calibration curve, whereas the index "mes" refers to the second measurement method (increase of the water bath temperature). It can be seen that results obtained on mutual thermal resistance are quite similar.

I_h (A)	$V_{DS1(0)}$ (mV)	$V_{DS1(25)}$ (mV)	$V_{DS2(25)}$ (V)	P_2 (W)	T_{1cal} (°C)	$R_{th12(cal)}$ (°C/W)	T_{1mes} (°C)	$R_{th12(mes)}$ (°C/W)
50	257.1	223.7	0.754	37.7	17.1	0.188	16.2	0.164
60	257.1	210.4	0.9213	55.3	20.2	0.184	19.0	0.163
70	257.4	195.5	1.1009	77.1	23.1	0.170	22.6	0.163
80	257.7	179.3	1.3026	104.2	27.7	0.170	27.0	0.163

Table 5.4. Data for $I_c = 1$ A, $T_a = 10$ °C

The main disadvantage of the method is of course that it results in a temperature measurement which is not directly the DUT one. We propose in the following section a way to estimate it, based on the measurement of the mutual thermal resistance detailed in the present section, coupled with a thermal model of the module.

5.7. Evaluation of self-heating thermal resistance through thermal modeling

The SiC MOSFET power module CAS100H12AM1 has a quite standard architecture, consisting of a seven-layer stack (as depicted in Figure 5.3):

- a copper base plate (thickness: 4 mm, thermal conductivity: 400 W.m⁻¹.K⁻¹),

- a DBC substrate, composed of two copper heat diffusion layers (thickness: 300 μm , thermal conductivity: 400 $\text{W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$) directly bonded on either side of an insulation layer (here in aluminum nitride, thickness: 600 μm , thermal conductivity: 170 $\text{W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$),
- SiC chips (thickness: 400 μm , thermal conductivity: 490 $\text{W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$),
- two solder layers (tin-lead alloy, thickness: 50 μm , thermal conductivity: 20 $\text{W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$), which bond the DBC lower diffusion layer to the base plate, and the DBC upper diffusion layer to chips.

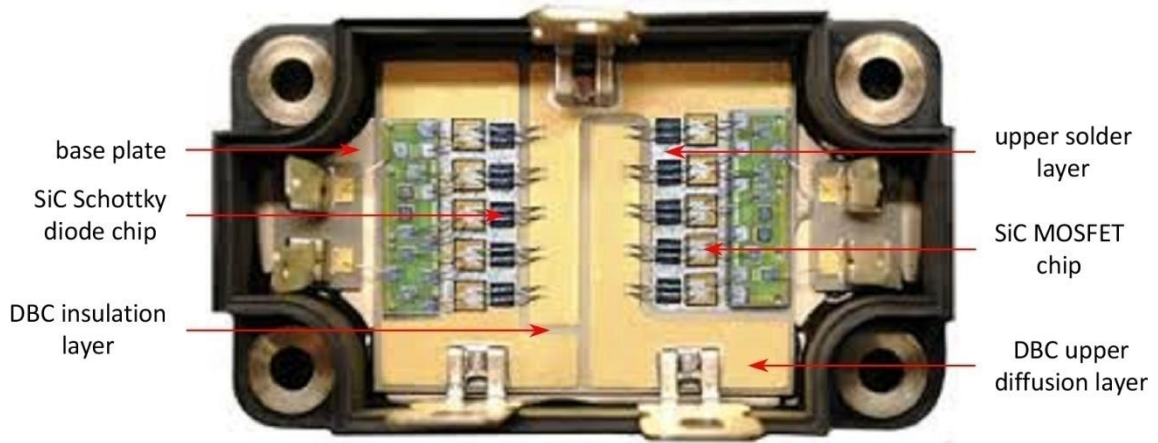


Figure 5.20. Internal top view of the CAS100H12AM1 power module

Typical values are considered for layer thicknesses (except for the base plate one, which has been measured) and material thermal conductivities. Other dimensions have been measured by means of a caliper. Figure 5.20 presents the internal top view of the CAS100H12AM1 module. As it can be seen, each MOSFET function of this power module is realized by means of five $4\times 4\text{ mm}^2$ chips in parallel. Module geometry and material thermal properties have been implemented in COMSOL Multiphysics software, using the heat conduction equations in steady state as model physics. For heat dissipation in MOSFET M2, it is supposed that current is equally shared between the five chips.

Moreover, heat dissipation is assumed to be uniform within the volume of each chip. As a result, the volume density of heat dissipation within M2 chips is calculated as:

$$q_2 = \frac{P_2}{5 \cdot V_{\text{chip}}} \quad (5-17)$$

where P_2 is the power dissipated in M2 expressed by equation (5-14), and V_{chip} is the chip volume ($V_{\text{chip}} = 6.4\text{ mm}^3$). Lastly, as a junction temperature definition is required to determine the thermal resistance matrix of the module, we have chosen to compute it as the mean temperature over the volume of the considered MOSFET:

$$T_{1,2} = \frac{1}{V_{M1,M2}} \cdot \iiint_{V_{M1,M2}} T(x,y,z) \cdot dx \cdot dy \cdot dz \quad (5-18)$$

The problem has been meshed in approximately 711,000 elements. A boundary condition of Fourier type is applied on the backside of the base plate, to account for the heatsink efficiency. The equivalent exchange coefficient h_{eq} is determined iteratively, in order to obtain the same mutual thermal resistance as experimentally. This results in $h_{eq} = 1190 \text{ W.m}^{-2}.\text{K}^{-1}$ for $R_{th12} = 0.170 \text{ K.W}^{-1}$, or in $h_{eq} = 1235 \text{ W.m}^{-2}.\text{K}^{-1}$ for $R_{th12} = 0.163 \text{ K.W}^{-1}$. In both cases, the symmetry of the module thermal resistance matrix is verified ($R_{th12} = R_{th21}$). Furthermore, the almost full symmetry of the module geometry is numerically found ($R_{th1} = R_{th2}$), to within 0.001 K.W^{-1} . The M2 self-heating thermal resistance is $R_{th2} = 0.405 \text{ K.W}^{-1}$ in the first case, $R_{th2} = 0.397 \text{ K.W}^{-1}$ in the second case. Figure 5.21 presents the module temperature field in the second case ($h_{eq} = 1235 \text{ W.m}^{-2}.\text{K}^{-1}$), for a dissipated power in M2 corresponding to the 80 A operating point of Table 5.4 ($P_2 = 104.2 \text{ W}$).

We can check the model accuracy by comparing the MOSFET junction-to-case thermal resistance to the typical value, i.e. 0.160 K.W^{-1} , specified in the CAS100H12AM1 power module datasheet. This thermal resistance corresponds to the MOSFET self-heating one, when applying a boundary condition of Dirichlet type on the backside of the base plate. The computation of the model under such a condition results in a self-heating thermal resistance of 0.154 K.W^{-1} for both MOSFETs, which is very close to the typical value given in the CAS100H12AM1 datasheet.

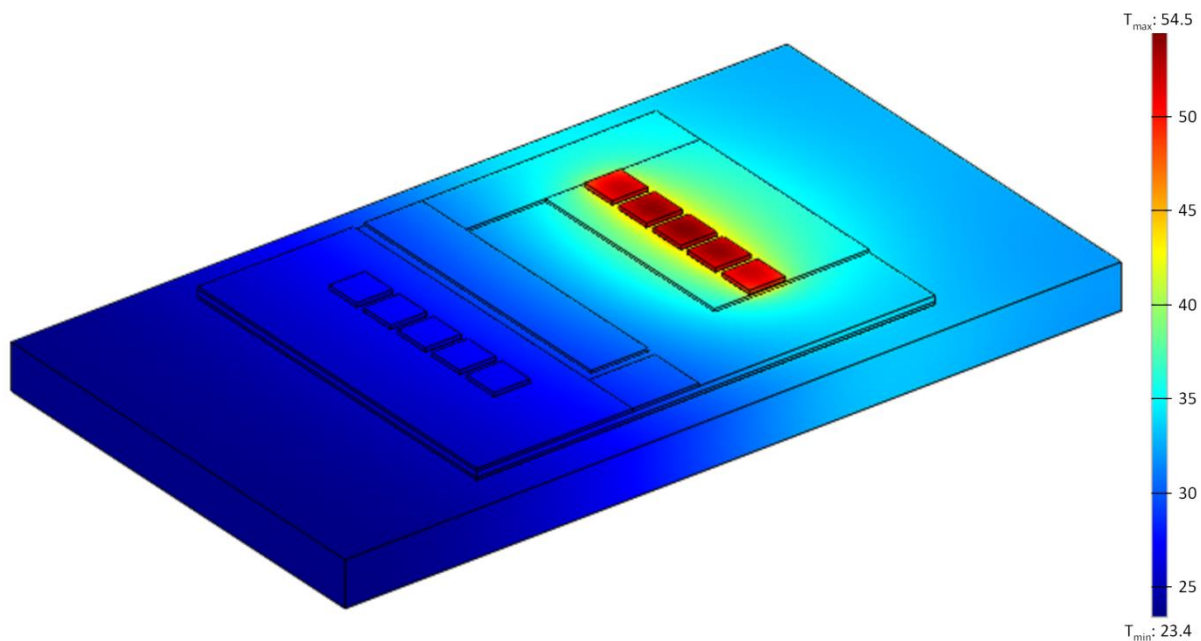


Figure 5.21. Temperature field of the CAS100H12AM1 module
(Simulation conditions: $h_{eq} = 1235 \text{ W.m}^{-2}.\text{K}^{-1}$, $P_2 = 104.2 \text{ W}$)

Table 5.5 hereafter summarizes experimental results (first four columns) from Table 5.4. The junction temperatures (T_{1simu} , T_{2simu}) are calculated using the finite element model (columns 5 and 6, $h_{eq} = 1235 \text{ W.m}^{-2}.\text{K}^{-1}$). $V_{DS2model}$ is the drain voltage of M2 computed by means of our steady state SiC MOSFET model (electrical model in chapter 4), using the junction temperature provided by the finite element model. As it can be seen, the modeling error is a bit significant at medium current. However, it represents only a few watts (or a few tens of millivolts) and decreases as current increases.

I_{DS2exp} (A)	V_{DS2exp} (V)	P_{2exp} (W)	T_{1exp} (°C)	T_{1simu} (°C)	T_{2simu} (°C)	$V_{DS2model}$ (V)	P_{2model} (W)	error (%)
50	0.754	37.7	16.2	16.1	25.0	0.822	41.1	9.0
60	0.9213	55.3	19.0	19.0	32.0	1.000	60.0	8.5
70	1.1009	77.1	22.6	22.6	40.6	1.181	82.7	7.3
80	1.3026	104.2	27.0	27.0	51.4	1.378	110.2	5.8

Table 5.5. Experimental and modeling results
(Experimental conditions: $I_c = 1$ A, $T_a = 10$ °C. Simulation conditions: $h_{eq} = 1235$ W.m⁻².K⁻¹)

5.8. Conclusion

The junction temperature of SiC MOSFET module is monitored using TSEP technique which has been taken into consideration in this chapter. To measure the junction-to-case thermal resistance $R_{th(j-c)}$, an approach of thermal impedance method has been investigated which could be used to estimate the junction temperature of packaged device. The difficulties in the SiC MOSFET electro-thermal characterization using TSEPs in the regards of module structure and interface trap influences have been discussed.

From analyzing, the $R_{DS(ON)}$ has been chosen as TSEP for SiC MOSFET module. The interface traps have made SiC MOSFET electro-thermal characterization ineffective implementation. The TSEP instability due to the commutating the DUT gate voltage has been clearly illustrated in the estimation of self-heating thermal resistance. The results are not reliable, thereby an error in estimated temperature.

In order to utilize this method, the stability of the proposed TSEPs should be taken. Thus, the gate-source bias is needed to be constant in the measurement to avoid the unstable threshold voltage and/or reduced free carrier concentration. The second experimental test has therefore been conducted with a dedicated test bench using the thermal coupling. The mutual thermal resistance measurement can provide good accuracy and reproducibility.

The thermal resistance measurement of packaged SiC MOSFET by using $R_{DS(ON)}$ as the TSEP is feasible. Based on averaging junction temperatures between parallel chips by TSEP technique, the value of R_{th2} provided by the finite element model is about 0.405 K.W⁻¹. Compared to the results calculated by the electrical model in steady state SiC MOSFET model, the modeling error is acceptable.

General Conclusions and Perspectives

The potential benefits of the SiC MOSFET are widely acknowledged to name a few improvements in system size, weight, efficiency and operating temperature compared to Si counterparts. However, the profile of high trap density at the SiO₂-SiC interface has been considered as the critical processing limitation for the development of power SiC MOS-based devices. The work on the characterization and modeling of SiC MOSFET has been carried out in this dissertation to this end. The commercial module package SiC MOSFET from CREE Inc. rated at 1200 V/100 A is used to study to better evaluate its potential utilization in systems.

Beyond a state-of-the-art in the field of SiC power components in chapter 1 and 2, this dissertation achieves several main results.

Chapter 3 relates to the static characterization. By single-pulse method, power dissipation of the SiC MOSFET in the characterization is controlled by the duration of the pulse to avoid self-heating effect, thus, keep T_j constant in the measurement. The I-V characteristics of a SiC MOSFET at different junction temperatures T_j from -30 °C to 150 °C are studied and thus presented. Another realized work in Chapter 3 is to measure the static on-resistance by the impedance spectroscopy technique. Compared to the conventional method, the proposed method takes the advantage of simple setup and the isolation of the measurement equipments from the high DC bias power source. The on-resistance of device is measured in the ohmic region at small V_{DS} . Through the measurement results, the influence of the interface traps charge on the characteristics is investigated as the function of gate bias and temperature.

Power SiC MOSFET modeling is presented in Chapter 4. The physical phenomena related to the interface traps have been investigated, which have considerable impact on the device behavior and modeling. Based on the characterization results, a compact model for SiC MOSFET by mathematical functions is developed and simulated in SABER. The model accounting for the interface traps and the short-channel effects within power SiC MOSFETs has been proposed. By using the simple expression of channel voltage, the SiC MOSFET saturation due to the velocity saturation effect in the drift region is also considered in this model. The electro-thermal issues have been carried out, including the effects of temperature on the threshold voltage, inversion layer mobility, drift region resistance and channel resistance. The unknown parameters of the compact SiC MOSFET model have been extracted where mathematical model matches the experiments with the physical reality. The parameter extraction procedure is also analyzed using the optimization tool in MATLAB. The temperature-dependent total current is introduced in the model which is well validated by comparing the simulation with the measurement.

The electro-thermal characterization and model validation are addressed in Chapter 5. As new device technologies and new packaging, some well-understood and well-known TSEPs for Si technology can not directly apply for SiC MOSFET. The performing a reliable TSEP for the SiC MOSFET electro-thermal characterization has been considered in this work. The on-resistance of the SiC MOSFET is used as the TSEP to estimate the junction temperature. The $V_{DS(ON)}$ -method is evaluated. The dedicated test

benches are built for the SiC MOSFET thermal measurement and several experimental tests have been performed. The results indicate that the self-heating measurement is affected by the interface traps, thereby an error in estimated temperature. Based on the thermal coupling, the mutual thermal resistance measurement method is developed which provides better accuracy and reproducibility. Using the junction temperature estimated by the 3D finite element model and the proposed electrical model in chapter 4, a good agreement between the simulations and experiments is demonstrated.

According to these contributions, the foundations of characterization and modeling of SiC MOSFET have been laid in this dissertation, especially on the static behavior. Areas of future work can be identified

Electro-thermal coupling needs to be developed for the consideration of the heat distribution and current sharing between paralleled chips in the module. The SiC Schottky diode in the module can be considered for mutual thermal resistance measurement.

Regarding the characterization, the switching behavior up to temperatures of 150 °C can be considered in the future work. Therefore, the characterization method can be further developed, which is adopted to power SiC MOSFET module with the profile of high trap density.

Based on the model presented in the dissertation, the compact SiC MOSFET model can be further ameliorated for switching behavior. The parameters used in the model can be obtained directly from the characterization results by the fitting method. Therefore, power device models can be automatically generated after characterization step. In such a way, they can be widely used in simulation software to represent the power SiC MOSFET behavior in the converters.

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“Characterization, analysis and modeling of silicon carbide power MOSFET”

Abstract

The characterization and modeling, in particular on-state of the SiC MOSFET, have been investigated in this dissertation to develop insight of the unique characteristics along with the effects on the design of power converters.

In such a way, the characterization test benches for high voltage power MOSFETs have been developed. The device is characterized using appropriate methods, which allows the junction temperature to remain constant during the measurement. The characteristics are then analyzed and compared to those of Si counterpart to provide further understanding of SiC MOSFETs. Subsequently, a novel compact model has been developed for circuit simulation, considering physical phenomena including interface traps, short-channel, intrinsic JFET and temperature effects. As a modified version of the Shichman Hodges, the model employs a few adjustment parameters, which are mostly derived from curve fitting of experimental data, using optimization tool software. In the end, the thermal characterization of SiC MOSFETs is examined. In the presence of the interface traps, the dedicated test benches have been developed for SiC MOSFET temperature measurement based on TSEP. 3D Finite element (FEM) simulation is performed to investigate thermal distribution inside the module. By comparing with the experiments, the electro-thermal model is validated with acceptable accuracy.

Keywords: SiC, MOSFET, I-V characteristics, modeling, thermal measurement, TSEP

« Caractérisation, analyse et modélisation du MOSFET de puissance en carbure de silicium »

Résumé

La caractérisation et la modélisation, en particulier l'état de fonctionnement du MOSFET SiC, ont été examinées dans le cadre de cette thèse afin de mettre en lumière les spécificités et les conséquences qui en découlent sur la conception des convertisseurs de puissance.

C'est ainsi qu'une méthodologie de caractérisation statique pour les MOSFET à haute tension a été développée. Les caractéristiques ont été mesurées par méthodes appropriées permettant à la température de la jonction de rester constante pendant la mesure. Les résultats expérimentaux ont été analysés et comparés à ceux relatifs aux dispositifs conventionnels en Si. Ensuite, un nouveau modèle compact du module MOSFET SiC a été mis au point sur le logiciel Saber pour des simulations orientées circuit. Ce modèle prend en compte les phénomènes physiques observés, notamment les effets des pièges d'interface, le comportement JFET intrinsèque, le canal court et la température. En tant que version modifiée de Shichman Hodges, le modèle utilise un nombre raisonnable de paramètres d'ajustement, lesquels sont principalement extraits par identification des courbes de données expérimentales à l'aide d'un logiciel d'optimisation. Finalement, nous avons abordé la caractérisation électro-thermique des MOSFET de SiC. Pour remédier à la présence de pièges d'interface, des bancs de test dédiés ont été développés pour la mesure de la température MOSFET au SiC sur la base du TSEP. Une simulation par éléments finis 3D (FEM) est réalisée pour étudier la distribution thermique à l'intérieur du module. En comparant avec les expériences, le modèle électro-thermique a été validé avec une précision acceptable.

Mots-clés: SiC, MOSFET, caractéristiques I-V, modélisation, mesure thermique, TSEP