



HAL
open science

Converter architecture integrating detection of electric arc faults applied to continuous photovoltaic energy sources

Benjamin Vidales

► **To cite this version:**

Benjamin Vidales. Converter architecture integrating detection of electric arc faults applied to continuous photovoltaic energy sources. Signal and Image processing. Université de Lorraine; Instituto tecnológico de Morelia (Mexique), 2021. English. NNT : 2021LORR0040 . tel-03335792

HAL Id: tel-03335792

<https://hal.univ-lorraine.fr/tel-03335792v1>

Submitted on 21 Jun 2022

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



AVERTISSEMENT

Ce document est le fruit d'un long travail approuvé par le jury de soutenance et mis à disposition de l'ensemble de la communauté universitaire élargie.

Il est soumis à la propriété intellectuelle de l'auteur. Ceci implique une obligation de citation et de référencement lors de l'utilisation de ce document.

D'autre part, toute contrefaçon, plagiat, reproduction illicite encourt une poursuite pénale.

Contact : ddoc-theses-contact@univ-lorraine.fr

LIENS

Code de la Propriété Intellectuelle. articles L 122. 4

Code de la Propriété Intellectuelle. articles L 335.2- L 335.10

http://www.cfcopies.com/V2/leg/leg_droi.php

<http://www.culture.gouv.fr/culture/infos-pratiques/droits/protection.htm>



Architecture de convertisseur intégrant une détection de défauts d'arcs électriques appliquée aux sources d'énergie continues d'origine photovoltaïques.

THÈSE

Présentée et soutenue publiquement le 15 Décembre 2020

Pour l'obtention du

Doctorat de l'Université de Lorraine
(Spécialité systèmes électroniques)

Par

Benjamin Vidales Luna

Composition du jury

Président :

M. Bertrand Raison, Professeur, Université de Grenoble Alpes, Grenoble

Rapporteurs :

M. Erwann Carvou, Enseignant chercheur HDR, Université de Rennes 1, Rennes

M. El-Hassane Aglizim – Professeur, Université de Bourgogne, Nevers

Examineurs :

M. Serge Weber, Professeur, Université de Lorraine, Directeur de thèse (DT)

M. Patrick Schweitzer, MCU – HDR, Université de Lorraine, Co-directeur de thèse (CDT)

M. Manuel Madrigal Martínez Profesor SNI- II, Tecnológico Nacional de México – (DT Mexique)

M. Domingo Torres Lucio, Profesor, Tecnológico Nacional de México - (CDT Mexique)

Mme. Nadia Maria Salgado Herrera, Profesora Asociada, Instituto de Energías Renovables (IER - Mexique).

M. José Luis Monroy-Morales, Profesor SNI- C, Tecnológico Nacional de México.

Remerciements

I want to express from the bottom of my heart my most sincere gratitude to my beloved family for all their love and support along this path in the search of knowledge, especially to my father who with his example instilled in me the will to achieve my goals with respect and honesty.

I thank my advisor and friend Dr. Manuel Madrigal Martínez for allowing me to work shoulder to shoulder on this great project, as well as sharing his valuable advice and experiences with me, which shape me as a human being and as a professional for the future.

I thank my advisor and friend Dr. Domingo Torres Lucio for having shared his french studies experience with me, which undoubtedly motivated me to have this type of experience and which allowed me to polish new skills in a great environment of work.

I thank my advisers Patrick Schweitzer and Serge Weber for all their support, advice and guidance in discovering new branches of knowledge that overcome barriers of distance, languages and cultures.

I thank all the departments of the PGIIE and IJL for all their hard work and effort which favor the high-level technological development of science without losing the human warmth and kindness that characterizes them so much.

I also thank my colleagues Dr. José Luis Monroy Morales and Dr. Juan Ramón Rodríguez Rodríguez, not only for their knowledge and experience shared but also for their kind friendship.

To the National Council of Science and Technology (CONACYT), for having allowed me to be part of the scholarship holders for postgraduate studies in both my master and doctoral degree.

I am grateful to the National Association of Universities and Institutions of Higher Education (ANUIES) for its support through the exchange project for researchers and students, México-France ECOS-NORD.

To the Technological Institute of Morelia and the University of Lorraine for given me the opportunity to train as a professional within these beautiful educational institutions.

Abstract

In this research work, the development of a multilevel inverter for PV applications is presented. The PV inverter, has two stages one DC/DC converter and one DC/AC inverter, and is capable of generating an AC multilevel output of nine levels, it's a transformerless inverter and uses a reduced number of components compared to other topologies. The conception of a novel DC/DC converter is capable of generating two isolated DC voltage levels needed to feed the DC/AC stage. This DC/DC stage is developed in two variants, buck and boost, the first to perform the reduction of voltage when the DC bus is too high, and second to increase the voltage when the DC bus is too low to perform interconnection with the grid through the DC/AC inverter.

This is achieved thanks to the parallel functioning of the developed topology, which make use of moderated duty cycles, that reduces the stress in the passive and switching components, reducing potential losses. The validation of the PV inverter is performed in simulation and experimental scenarios. In the other hand, the response of the inverter facing an arc fault in the DC bus is studied by performing a series of tests where the fault is generated in strategic points of the DC side, this is possible thanks to the design and construction of an arc fault generator based in the specifications of the UL1699B norm. During the tests is observed that with the apparition of an arc fault, there is a lost in the half-wave symmetry of the AC multilevel output voltage waveform, generating even harmonics which aren't present during normal operation, only when an arc fault is present in the DC system.

The monitoring of even harmonics set the direction for developing the detection technique. Since the magnitude of even harmonics in the inverter is very low, the total even harmonic distortion is employed as a base for the detection technique presented in this thesis. The effectiveness of this method is verified with a series of tests performed with different loads.

Résumé de Thèse

En 2019, l'EIA (Energy Information Administration) a publié l'annual Energy Outlook (AEO) où la projection énergétique pour les Etats-Unis est étudiée et modélisée afin de prédire d'une façon approximative la demande d'énergie nécessaire d'ici 2050. Cette étude est basée sur le système national de modélisation énergétique AEO (NEMS), un modèle intégré qui prend en compte les interactions des changements économiques, tels que l'offre et la demande mais également les prix de l'énergie. Selon cette étude, la production d'énergie au moyen de sources renouvelables, comme la production éolien et le solaire photovoltaïque seront les principales sources d'énergies du futur.

Le solaire photovoltaïque représentera 48% de la production totale et la production éolienne 25% d'ici l'an 2050, comme le montre la Fig. 1.

Electricity generation from natural gas and renewables increases, and the shares of nuclear and coal generation decrease—

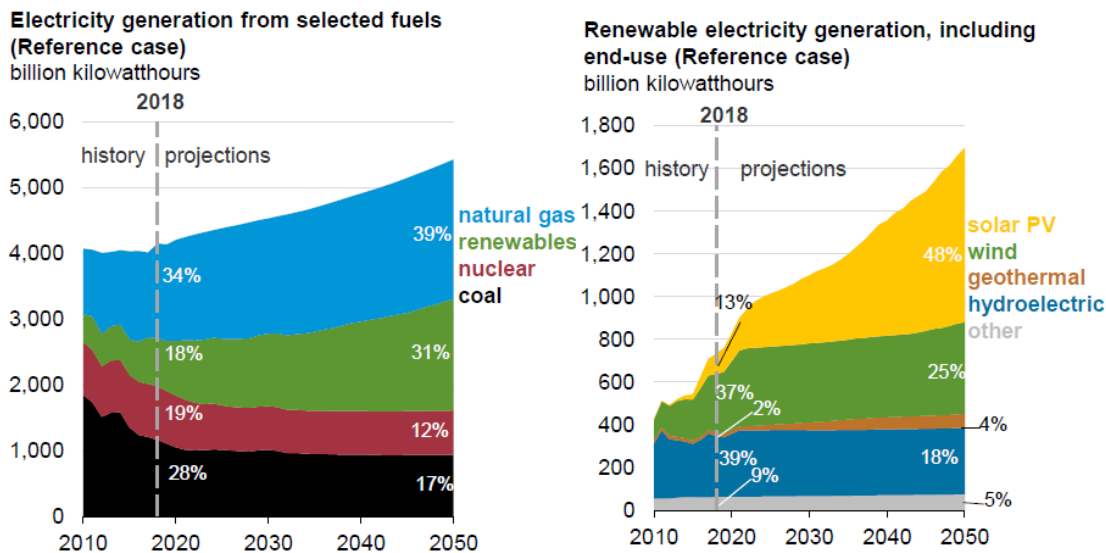


Figure 1. AEO report of renewable energy production projected to 2050.

La constante croissance des installations solaires photovoltaïques a conduit à la recherche et au développement de convertisseurs de haute puissance nécessaires pour effectuer l'interconnexion des panneaux photovoltaïques au réseau national. Cette technologie de convertisseurs tente d'obtenir une réduction du nombre de composants, tout en maintenant

une efficacité performante et en intégrant une protection contre les défauts, entre autres.

Dans le domaine des énergies renouvelables et la production d'énergie électrique, la détection des arcs électriques est d'une importance fondamentale et constitue une des préoccupations de cette thèse. Plus particulièrement nous nous concentrons sur la détection des défaut d'arc électrique série qui peuvent apparaître dans notre installation.

La structure principale d'un réseau smart grid est présentée sur la Fig. 2. L'ensemble se compose de convertisseurs DC/DC et DC/AC transformant l'énergie produite par les panneaux photovoltaïques en courant alternatif dans le cas particulier d'un système interconnecté au réseau électrique. Une autre configuration consiste à utiliser des batteries pour le stockage de l'énergie.

La première partie de ces travaux de thèse consiste à développer une topologie de convertisseur multiniveaux innovant. En effet une structure de convertisseur multiniveaux apporte de multiples avantages pour la génération d'énergie tels qu'un faible contenu harmonique, un nombre de composants réduit et un meilleur contrôle de la puissance transmise au réseau.

Le second thème abordé concerne l'intégration d'un système de détection de la présence d'un défaut d'arc électrique dans le convertisseur. En effet, l'apparition des défauts d'arc électrique peut conduire à l'apparition d'un incendie dans un système de génération photovoltaïque et doit absolument être détecté.

Ces arcs peuvent apparaître soit à l'intérieur de panneaux (câbles internes de connexion des cellules silicium, entre les cellules etc.) soit à l'extérieur des panneaux (boîte de connexion, câbles des distributions, etc.). Ces défauts d'arc électrique sont soit des arcs séries soit des arcs en parallèle. La Fig. 3 montre les principaux défaut d'arc en série ou parallèle pouvant se produire dans une installation des panneaux solaire photovoltaïque.

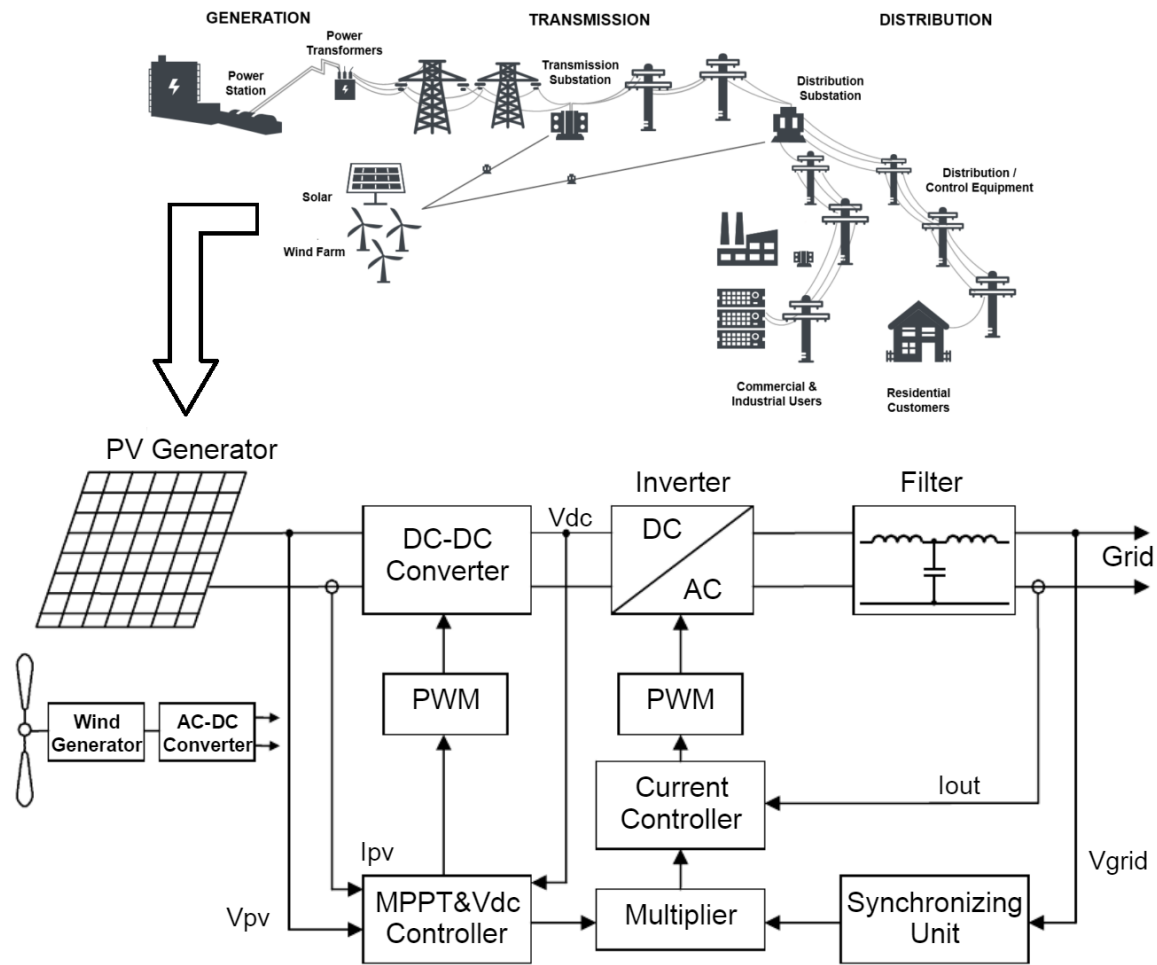
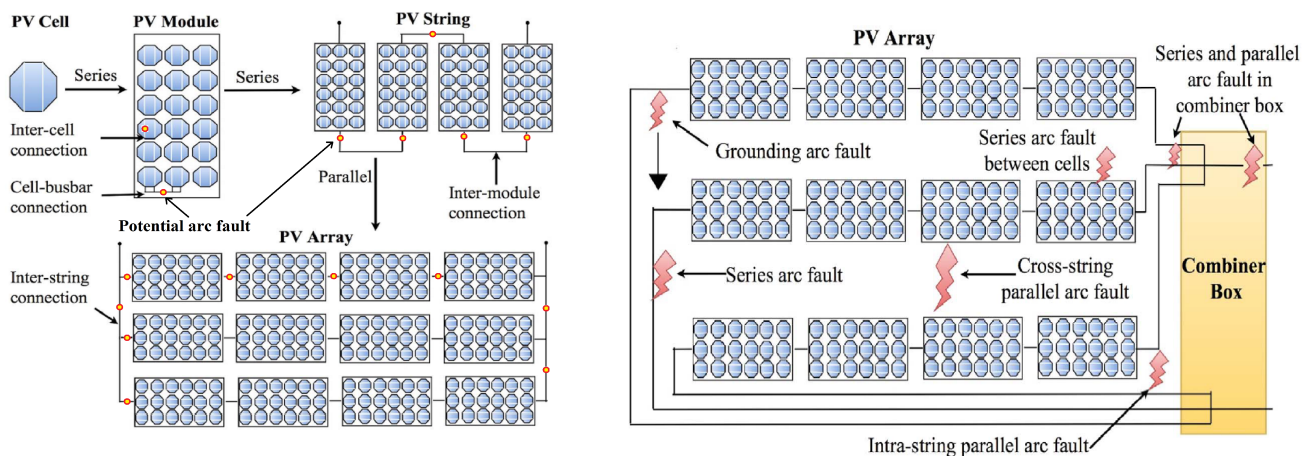


Figure 2. Distribution Grid arrangement.



(a) Potential points of internal fault in a PV panel.

(b) Potential points of fault in a PV array.

Figure 3. Potential Arc Fault in PV panels.

En raison des nombreux points de défauts possibles et de leurs différentes causes, le défi de développement d'un système capable de détecter efficacement les arcs dans ce type de système est une réelle préoccupation pour la sécurité des installations et des personnes.

Convertisseur Multiniveaux

Les systèmes de production PV utilisent des convertisseurs électroniques de puissance afin de transformer l'énergie provenant des panneaux en énergie exploitable par le réseau électrique. Parmi ces types de convertisseurs, les onduleurs à plusieurs niveaux présentent des avantages clés par rapport aux onduleurs conventionnels à deux niveaux.

Les onduleurs multiniveaux sont couramment utilisés pour des applications de forte puissance. La littérature présente de nombreuses topologies multiniveaux destinées aux applications dans le domaine des énergies renouvelables, à base des les topologies clamping diode, flying capacitor et cellules en cascade. Les principaux inconvénients de ces deux premières topologies sont l'utilisation de nombreux composants ainsi que le déséquilibre des niveaux de tension des condensateurs.

Cette topologie de cellules est constituée de plusieurs (minimum deux) modules connectés en série, sont basé sur des ponts en H complets. Le nombre de niveaux de tension peut facilement être augmenté en ajoutant de nouveaux modules, alors que les autres topologies voient le nombre des diodes ou de condensateurs augmenter de façon exponentielle.

Une topologie innovante de convertisseur neuf niveaux, présentée en Fig. 4, est proposée dans le chapitre 3 de la thèse.

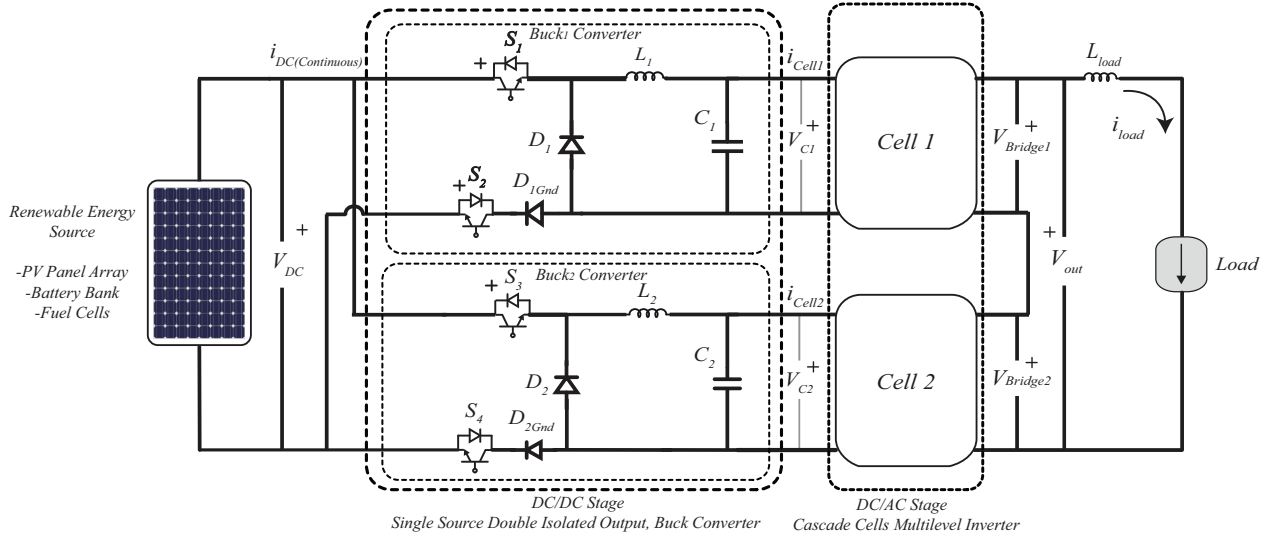
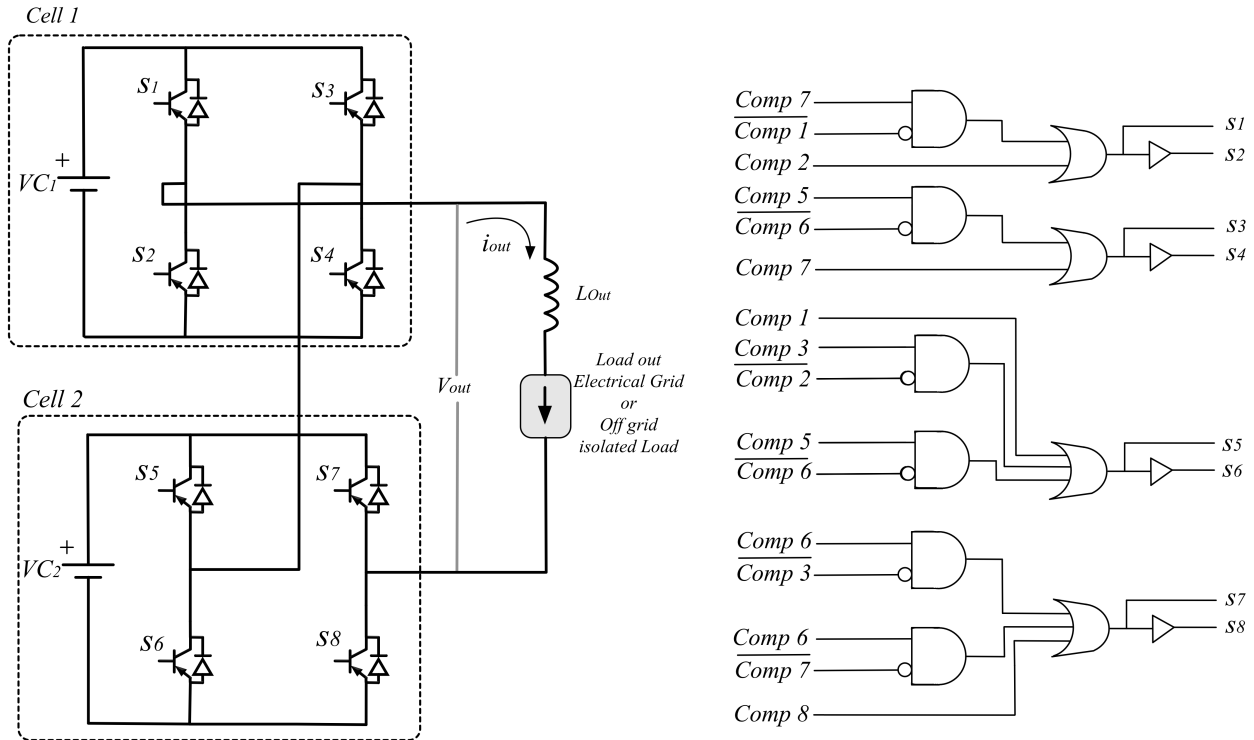


Figure 4. Inverter proposed system schematic diagram, buck variant.



(a) CCMI schematic circuit for a nine-level asymmetrical inverter. (b) Boolean logic combination for a nine-level asymmetrical inverter.

Figure 5. Cascade cells multilevel inverter topology and control.

Cette topologie utilise deux cellules en cascade et ainsi qu'une topologies DC/DC qui alimente ces deux cellules à partir d'une seule source. Dans le chapitre 3, deux structures différentes de convertisseurs DC/DC (variantes buck et boost) développés spécifiquement pour cette thèse sont proposés. La configuration des cellules en cascade ainsi que leur contrôle est présentée sur la Fig. 5 (a) et (b).

Avec cette configuration, les formes d'ondes simulée obtenues à la sortie de la cellule 1 (VBridge1) et de la cellule 2 (VBridge2), ainsi que les sorties tension et courant de convertisseur sont représentés dans la Fig.6.

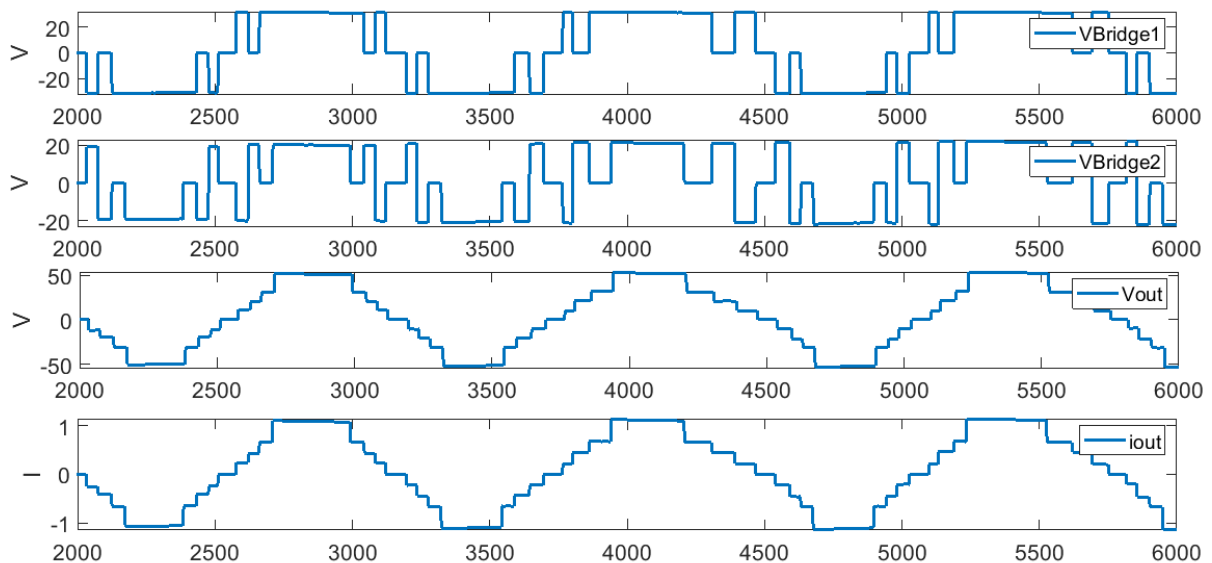


Figure 6. Simulation results of the DC/AC stage a) $V_{Bridge1}$, b) $V_{Bridge2}$, c) V_{out} , d) I_{out} .

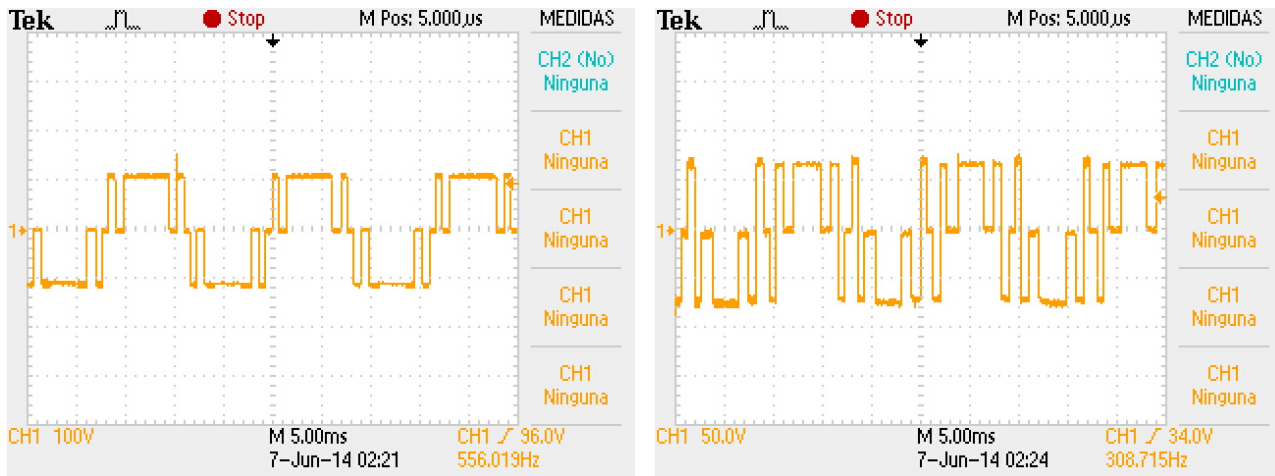
A partir des résultats de simulation, la topologie du convertisseur multiniveaux a été validée. Un banc de test a été développé pour tester expérimentalement ce convertisseur.

Banc d'essai

La Fig. 9 représente le banc d'essai et les équipements utilisés qui sont également listés dans la table 0.0.1.

Pour la mise en oeuvre de la partie électronique des convertisseurs, les PCB sont détaillés dans l'annexe 3. Avec ce banc d'essai, les Fig. 7 et Fig. 8 représentent les tensions mesurée a

$V_{Bridge1}$ et $V_{Bridge2}$ au niveaux de convertisseur.



(a) Voltage waveform of $V_{Bridge1}$.

(b) Voltage waveform of $V_{Bridge2}$.

Figure 7. $V_{Bridge1}$ and $V_{Bridge2}$ signals obtained using DC/DC Buck variant.

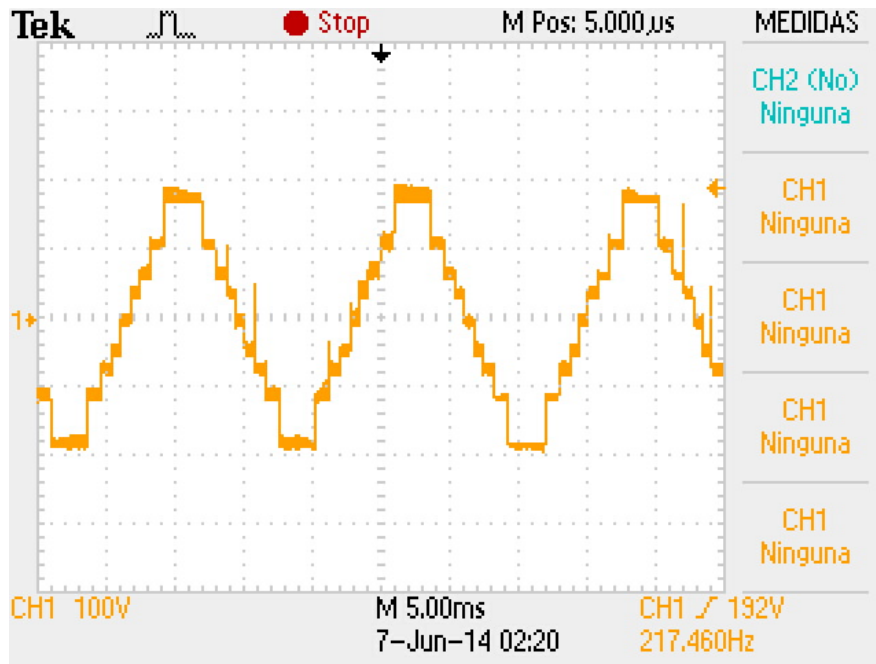
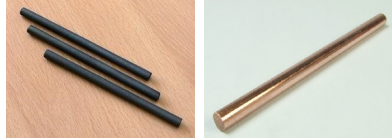
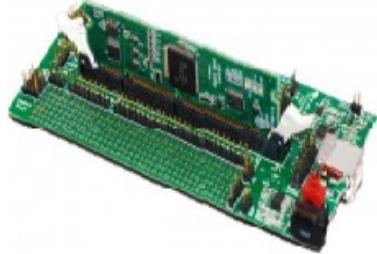






Figure 8. Voltage and current waveforms of the nine-levels AC output, using buck variant.

TABLE 0.0.1. Test Bench Equipment.

<i>Componet</i>	<i>Value – Image</i>
<i>Temperature</i>	20C°
<i>Electrodes Material</i>	 (a) Carbon (b) Copper
<i>Electrodes Distance Gap</i>	1 mm & 2 mm
<i>Protective Case Material</i>	10 mm acrylic box
<i>Texas Instruments DSP Matlab Simulink</i>	
<i>High Definition</i> <i>Oscilloscope LeCroy HD4096</i> 12 – bit resolution up to 8 GHz and 20 GS/s	
<i>Voltage Probe TESTEC TT – SI 9010</i> 7000 V 70MHZ	
<i>Arc Fault Generator UL1699B Based</i>	
<i>Current Probe CP030A</i> 30 A 50 MHZ	
<i>Load Type tested</i>	<i>R, RL, Complex Motor</i>
<i>Load Values Tested</i>	$R = 22\Omega, 47\Omega$ $L = 20mH, 141mH$ <i>Universal Motor = 1200 W Hammer Drill</i> <i>Universal Motor = 600 W Vacum Cleaner</i>

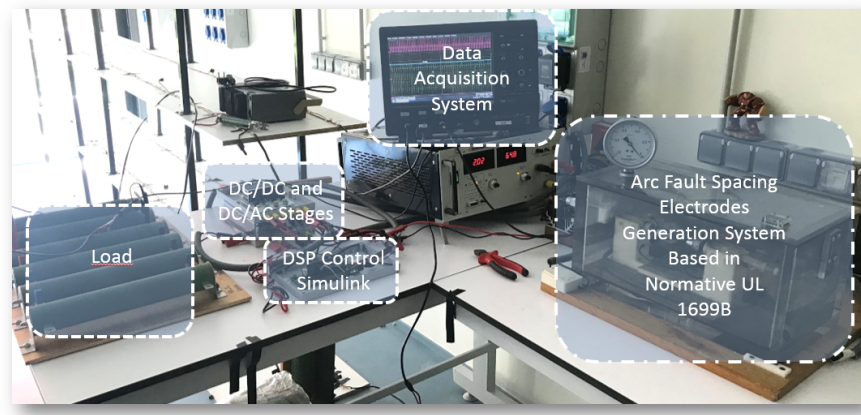


Figure 9. Experimental Test bench.

Pour étudier le comportement du convertisseur en présence des défauts d'arcs électriques, un générateur d'arc respectant la norme UL 1699B a été proposé. Les arcs électriques sont fait en suivant ainsi les spécifications de la norme UL 1699B. La technique d'écartement des électrodes est utilisée pour générer les défauts d'arcs (AF). La Fig. 10 illustre le dispositif.

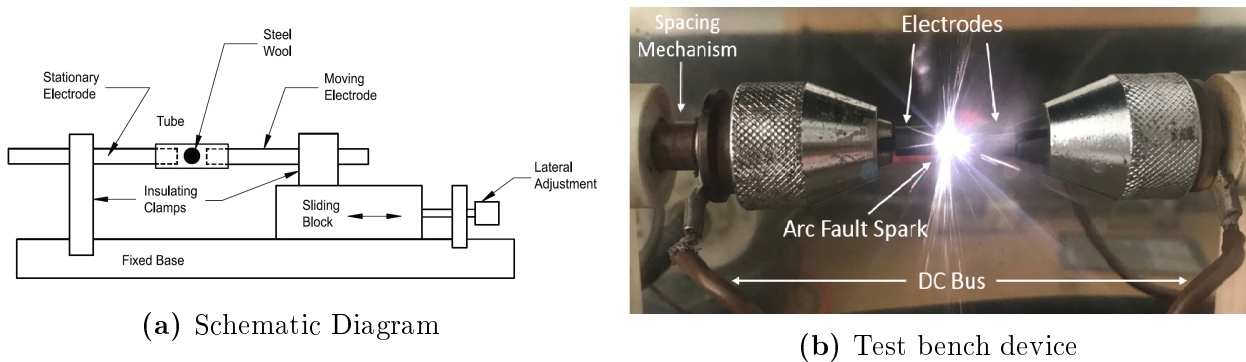


Figure 10. AF Generation device UL1699B.

Pour évaluer le comportement des convertisseurs, la partie DC/DC est testée expérimentalement en présence d'un AF. Ensuite la partie DC/AC est soumise au même défaut. Le schéma du banc d'essais représente sur la Fig. 11 montre l'emplacement du défaut inséré dans le circuit et des mesures de tension et courant réalisées.

Avec ces expériences, nous avons pu confirmer que l'étage DC/DC du convertisseur se limite a suivre les variation produite par l'AF. Par conséquent, chacune des fluctuations de l'AF

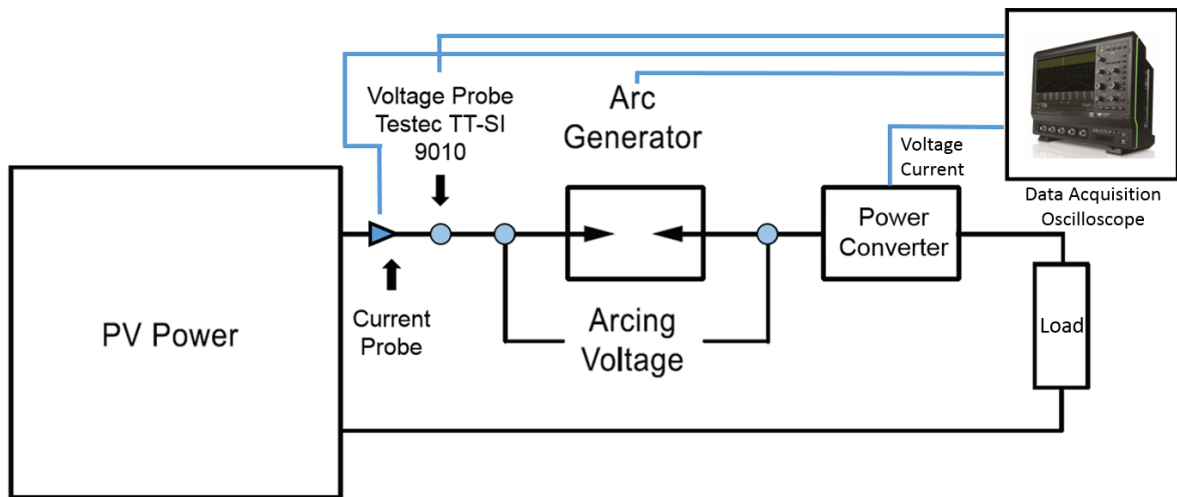


Figure 11. AF Load Study Schematic Diagram.

affecte la tension de sortie du convertisseur (même en utilisant un bloc de régulation MPPT). Néanmoins, nous montrons que l'AF crée des perturbation au niveau de l'étage de conversion DC/AC.

Détection des AF

Suite à la mise en évidence de l'influence de l'AF sur la topologie proposée du convertisseur multiniveaux. Avec l'apparition de l'arc dans le système, l'équilibre entre la cellule 1 et la cellule 2 de la configuration de cellules en cascade est altéré par les rapides fluctuations de l'arc. Ce changement produit la perte de certains des neuf niveaux dans la signal de sortie.

C'est sur ces phénomènes présentés dans la Fig. 12 que se base la stratégie de détection présentée dans ces travaux. La perte de niveaux associée à l'apparition est une d'arcs est une perturbation spécifique des défauts d'arc. Par contre, les modifications du rayonnement solaire sur le panneau n'affectent pas la symétrie des ondes comme le fait l'apparition d'arc.

Dans le mode de fonctionnement neuf niveaux du convertisseur (dans un mode de fonctionnement sans défaut dans le circuit), l'analyse spectrale de la tension montre que le

spectre est exclusivement composé d'harmoniques impaires.

Cela signifie qu'avec l'apparition d'un arc, la symétrie de l'onde est modifiée et la quantité d'harmoniques paires (inexistante en fonctionnement normal) se voit augmentée brusquement à l'apparition d'arcs (taux de distorsion d'harmoniques paires donc $THDe$).

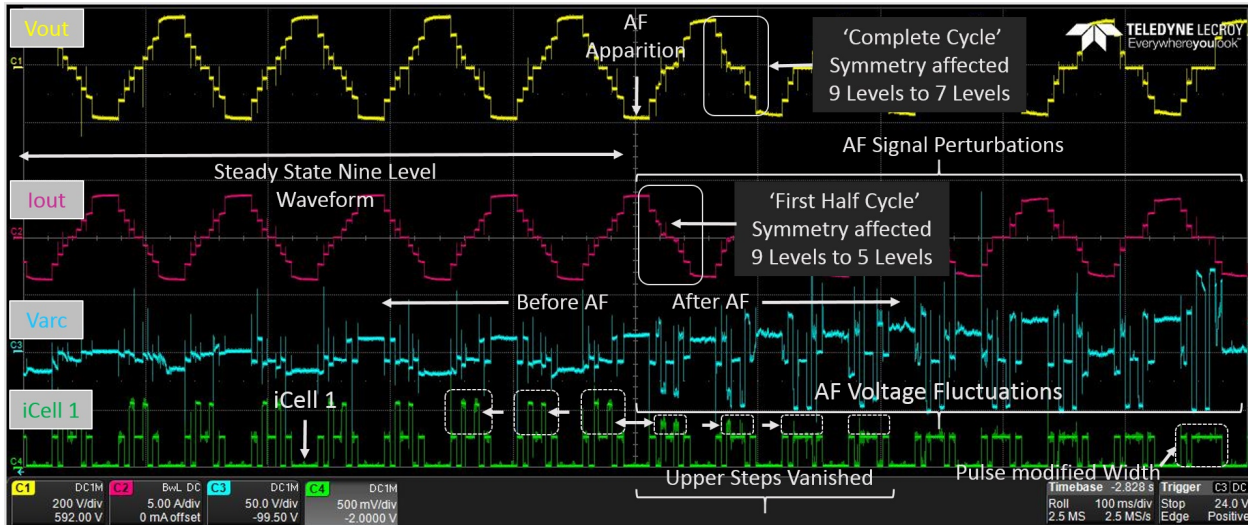


Figure 12. Multilevel waveforms obtained under AF.

L'échantillonnage des signaux expérimentaux se fait avec une cadence de 250 k/s afin de réaliser le traitement du signal avec Matlab. La Fig. 13 montre l'évolution du taux de distorsion harmonique en fonction de temps. Ces observations nous permettent de confirmer notre hypothèse concernant les changements sur le contenu harmonique paire au moment de l'apparition d'AF.

Génération des AF dans un Système isolé

Dans un premier temps, l'approche consistant à utiliser des signaux internes provenant du convertisseur pour déterminer la présence d'AF dans le système est testée dans la configuration de génération isolée. Pour la validation de cette approche, différentes charges sont alimentées avec la topologie présentée dans la Fig. 14. Les signaux pris en considération et mesure sont V_{H2} et I_{out} .

Les tests avec cette configuration nous permettent d'analyser comment le contenu harmonique

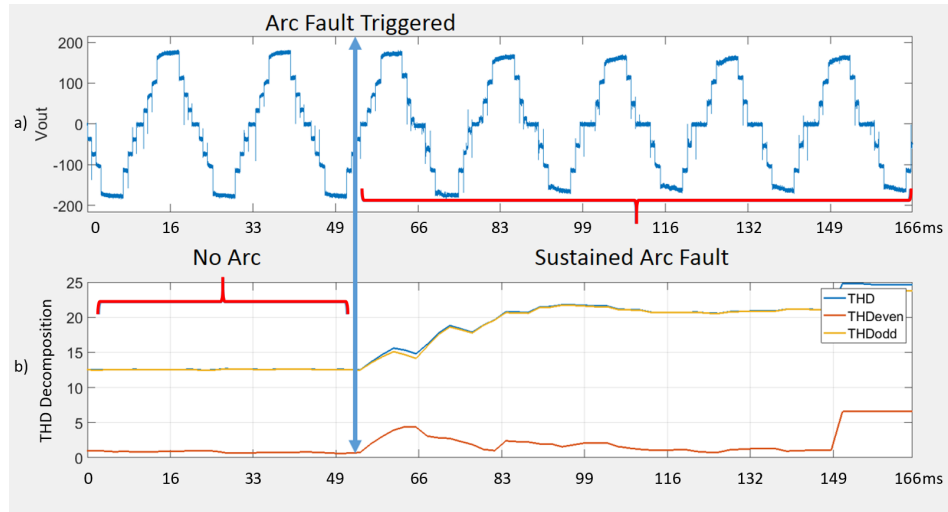


Figure 13. THD decomposition in THD_{even} and THD_{odd} before and after an AF.

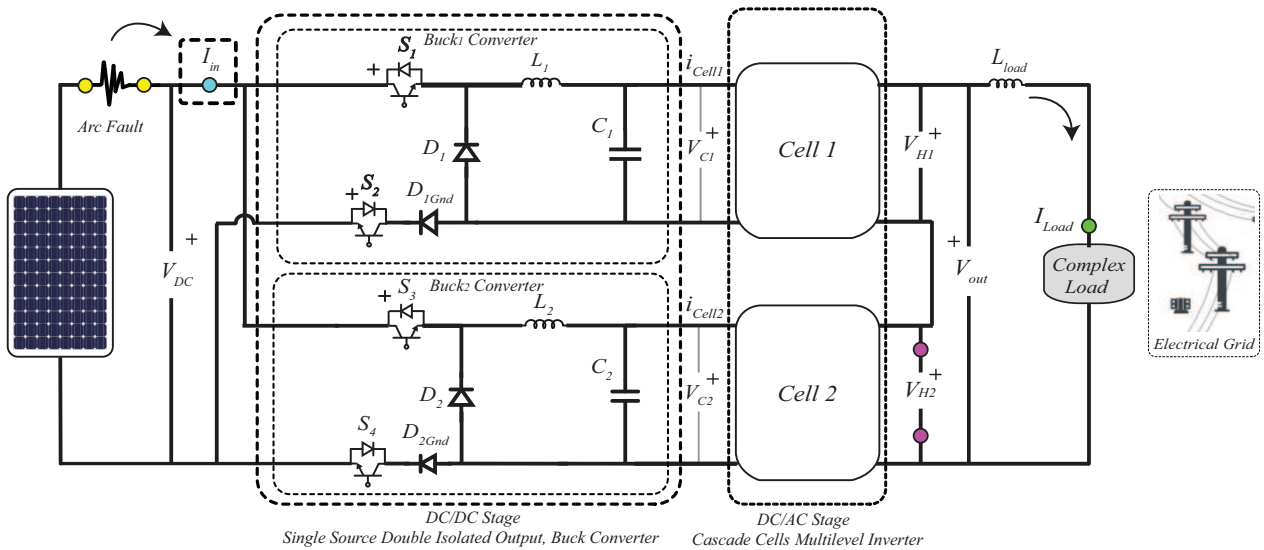


Figure 14. AF Testing protocol for different loads, with highlighted measuring points.

des signaux enregistrés varie avec l'apparition des arcs. A partir du contenu harmonique paire pour chacun de ces signaux, nous sommes en mesure de déterminer une valeur moyenne qui servira de seuil pour indiquer la présence d'arc.

Un exemple d'utilisation de cette approche est présenté en Fig. 15 et Fig. 16 pour une charge fortement inductive utilisée dans test. Les pics du contenu harmonique paire portant sur la signal $VH2$ liés à l'apparition de l'arc,

L'augmentation des harmonique paires liée a l'apparition du l'AF, est validée dans la section

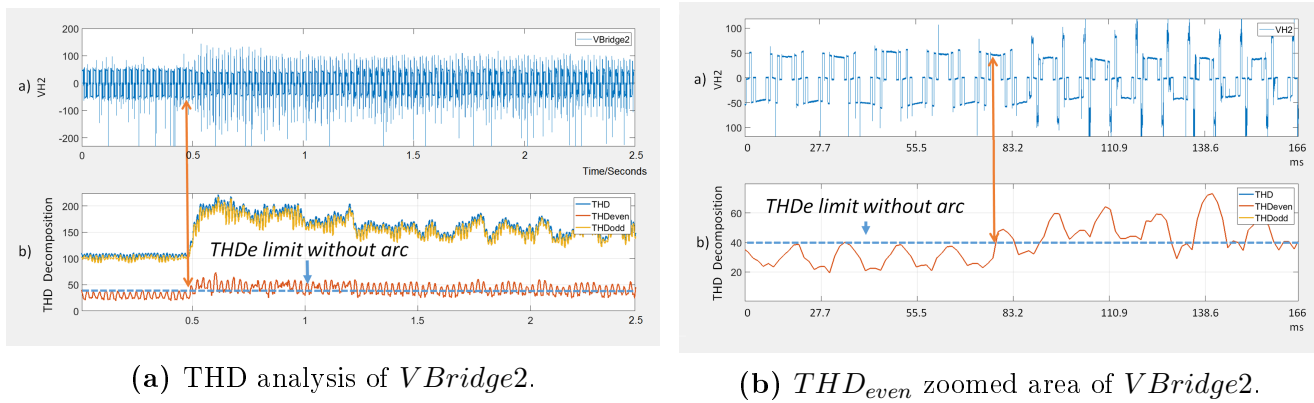


Figure 15. $V_{Bridge2}$ harmonics decomposition.

6.4 de la thèse pour l'ensemble des types de charges testées.

Par contre le comportement de I_{out} est très variable en fonction de la charge present dans le circuit, ce qui empêche sont utilisation dans un système de détection.

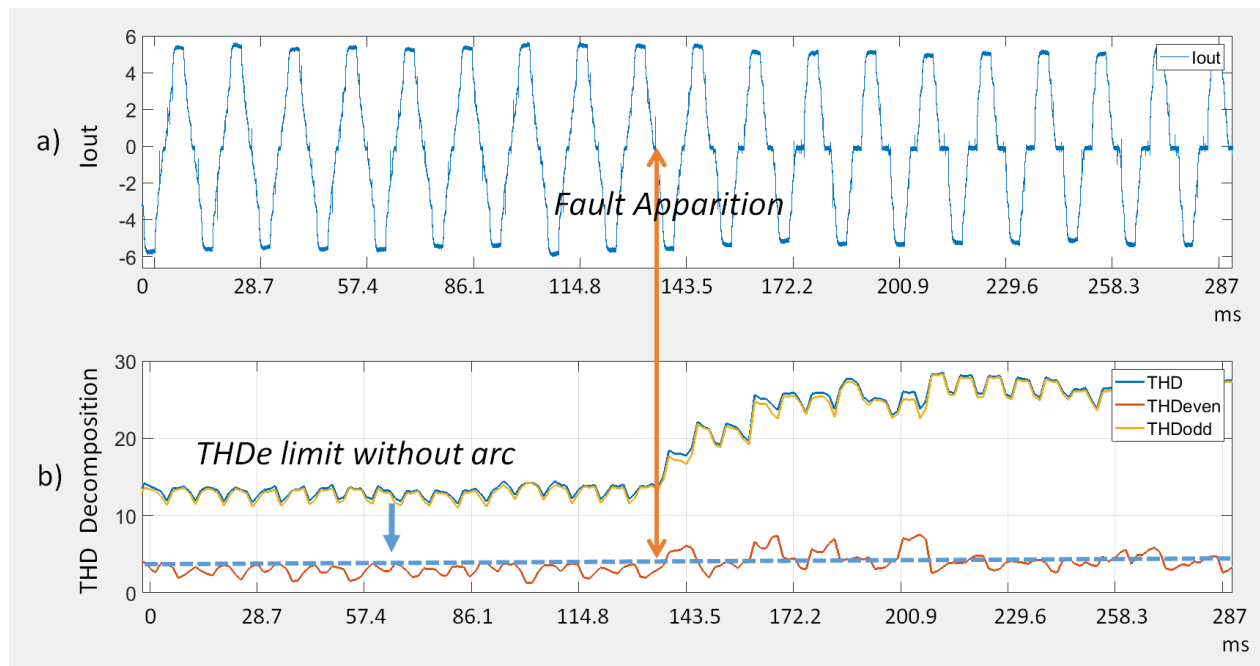


Figure 16. I_{out} THD Decomposition technique.

Le récapitulatif des changements dans le taux de distorsion avec l'apparition d'arc selon la charge connectée pour un système isolé est présenté dans la Fig. 17.

Signals	Without Arc	Without Arc	Without Arc	With Arc	With Arc	With Arc
THD Type	THD	THDo	THDe	THD	THDo	THDe
<i>I</i> _{out} 22 Ohms + 20mH	11-14%	11-14%	2-4%	25-29%	25-29%	5-8%
<i>V</i> _{Bridge2} 22 Ohms + 20mH	110-115%	95-110%	20-40%	150-220%	145-210%	38-65%
Criterion of 3% of increment						
<i>I</i> _{out} 22 Ohms + 141mH	8%	8%	0.5-1%	8-10% Only during ignition	8-10% Only during ignition	0.5-4% Only during ignition
<i>V</i> _{Bridge2} 22 Ohms + 141mH	110-115%	90-100%	22-40% 0.5sec during ignition	120-130%	110-115%	35-50%
Criterion of 13% of increment in THDe						
<i>I</i> _{out} Hammer-Drill	24%	24%	1-2%	26-29%	26-29%	8-13% Only during ignition
<i>V</i> _{Bridge2} Hammer-Drill	100%	100%	1-12%	165-195%	165-195%	8-35%
<i>I</i> _{out} Vacuum	22%	22%	3-4%	26-34%	26-34%	9% Only during ignition
<i>V</i> _{Bridge2} Vacuum	100%	100%	5-13%	145-200%	145-200%	10-29%

Figure 17. Summary of Results for AF Tests.

Les mêmes expérimentations sont menées en situation de système interconnecté au réseau.

Génération des AF dans un Système Interconnecté au Réseau

Pour étudier la réponse d'un système interconnecté au réseau en présence d'un AF, le schéma est identique à celui utilisé à la Fig. 14, avec la particularité d'avoir un filtre de couplage en sortie (calculé au paragraphe 6.5.2). Un algorithme de détection basé sur l'analyse des harmoniques paires est proposé pour tous les tests suivants. Le principe de détection consiste à effectuer une analyse période par période de la valeur maximale de l'amplitude du taux de distorsion $THDe$ de $VH2$, et en même temps la mesure de la quantité de pris dépassant un seuil déterminé de façon expérimentale. Pour tous les tests présentés, l'utilisation de l'algorithme de détection (basé sur l'étude des harmoniques paires) de la Fig. 18 est utilisé.

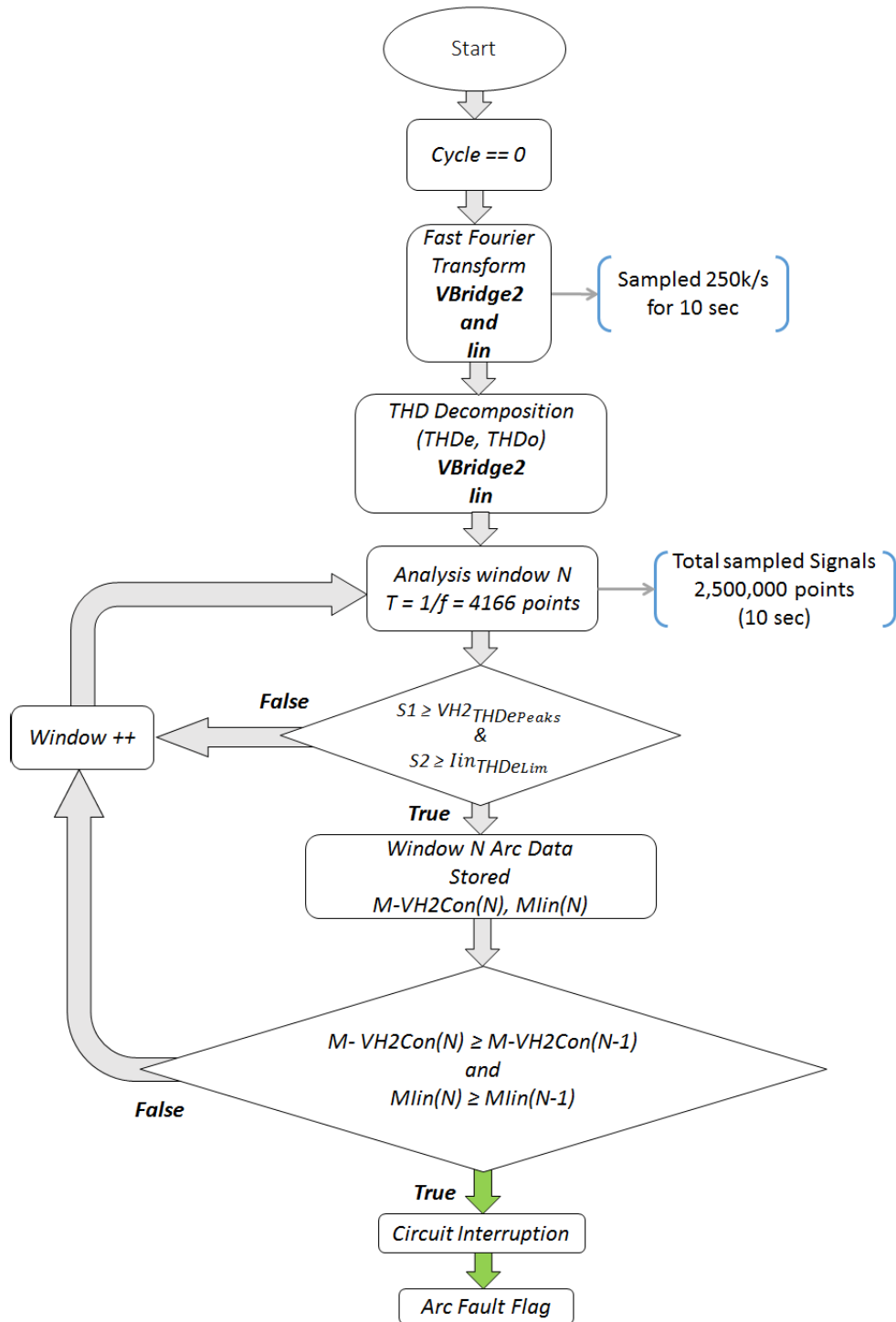


Figure 18. Proposed electric DC AF detection algorithm.

La Fig. 19 illustre comment cette opération est effectuée sur le signal $VH2$. Une fois ce processus terminé, l’algorithme de détection générera un signal logique avec une valeur de 1 qui restera à 1 jusqu’à ce que le défaut disparaisse. Sur la Fig. 20 est présenté le résultat obtenu dans le cas d’un AF pour une charge résistive.

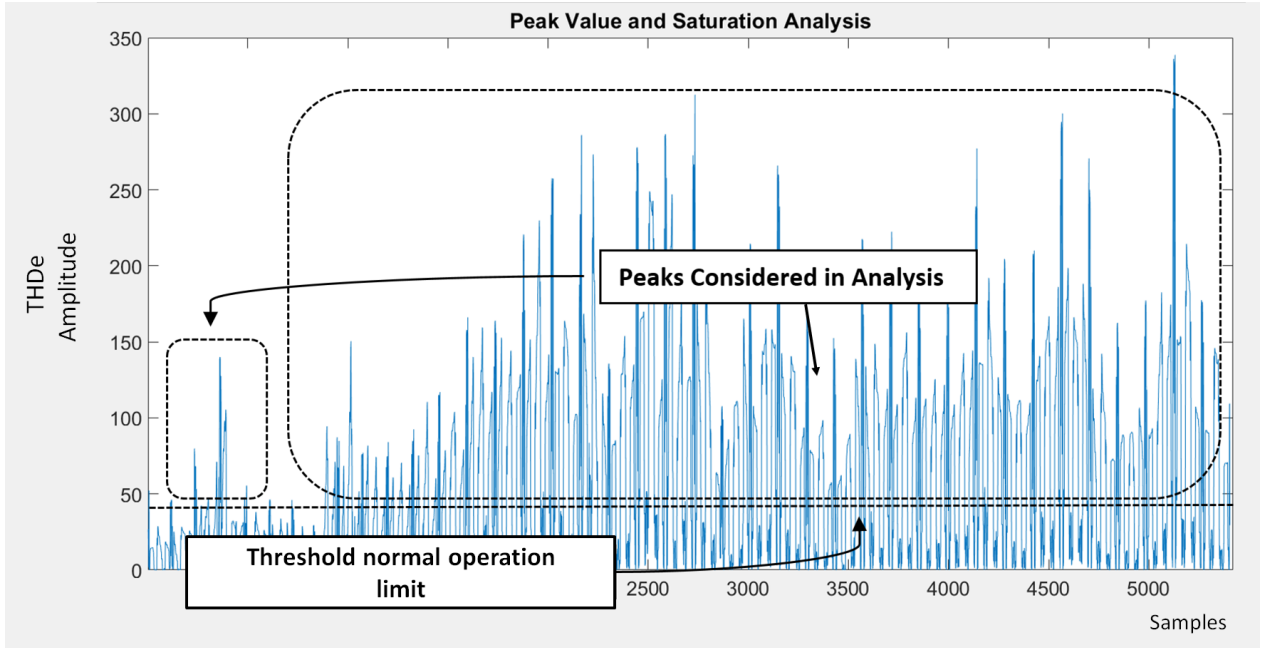


Figure 19. $THDe$ peak saturation analysis before and after an AF.

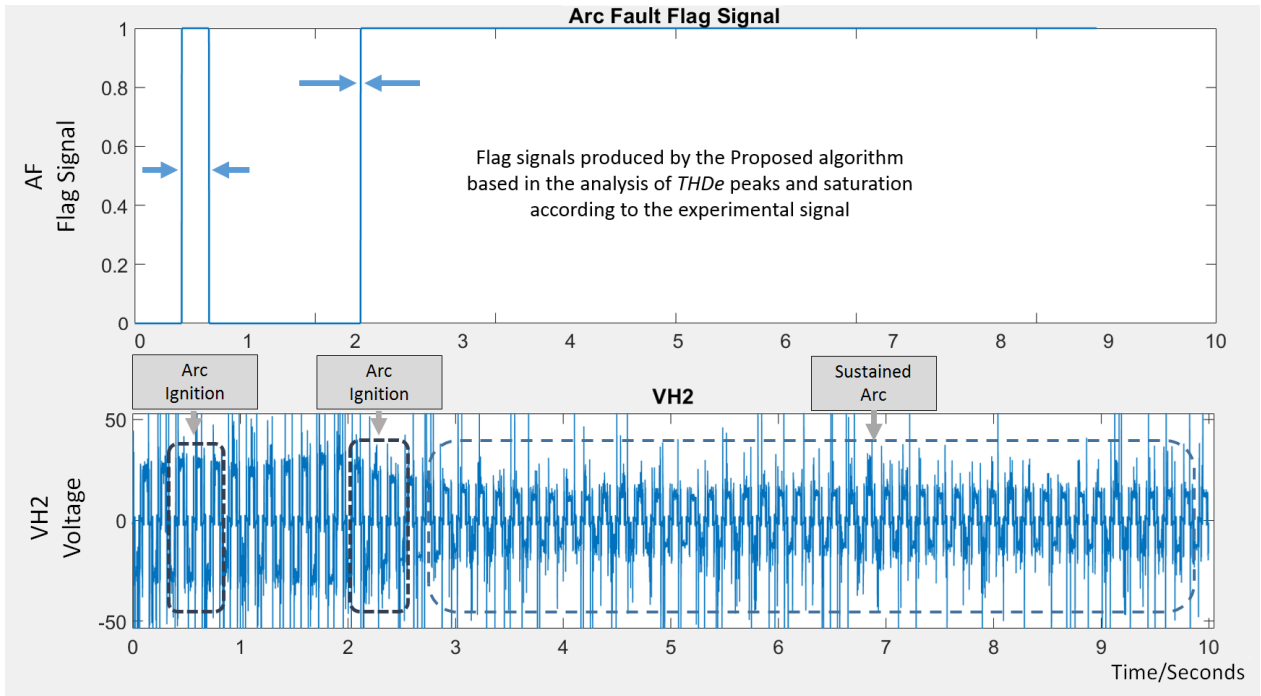


Figure 20. $VH2$ and AF Flag comparison.

Pour effectuer une validation approfondie, l'algorithme est soumis à une série de tests avec différents types de charges, et des variations d'illumination, de changement de charge instantané. Les valeurs spécifiques de toutes les expériences sont répertoriées dans le Tableau 0.0.3

TABLE 0.0.3. AF Algorithm testing with different loads.

<i>Loads & Number of AF tested</i>	<i>Value of Load</i>
<i>Resistance – 5</i>	47Ω
<i>Resistance – 5</i>	22Ω
<i>Resistive 47Ω Inductive – 5 each = 15</i>	$5mH, 30mH, 58mH$
<i>Resistive 22Ω Inductive – 5 each = 15</i>	$5mH, 30mH, 58mH$
<i>Resistive $22\Omega + 1200W$ Vacuum – 5</i>	<i>Fast speed</i>
<i>Resistive $22\Omega + 1200W$ Vacuum – 5</i>	<i>Slow speed</i>
<i>LCL Couplin Filter 5</i>	<i>LCL Filter Values</i>
<i>Total – 55</i>	

Dans l'ensemble des résultats d'expérimentation présentés dans la Fig. 21, des défauts d'arcs multiples sont générés dans un seul enregistrement afin d'augmenter la difficulté de détection et évaluer l'adaptabilité de l'algorithme. Nous remarquons également comment la distance d'écartement joue un rôle très important dans l'augmentation des perturbations. Plus grand sera l'écartement des électrodes plus grandes seront les variations générées par le défaut.

Les résultats expérimentaux présentés dans les différentes figures sont obtenus par concaténation de plusieurs enregistrements différents de défauts d'arc afin de tester la robustesse d l'algorithme de détection.

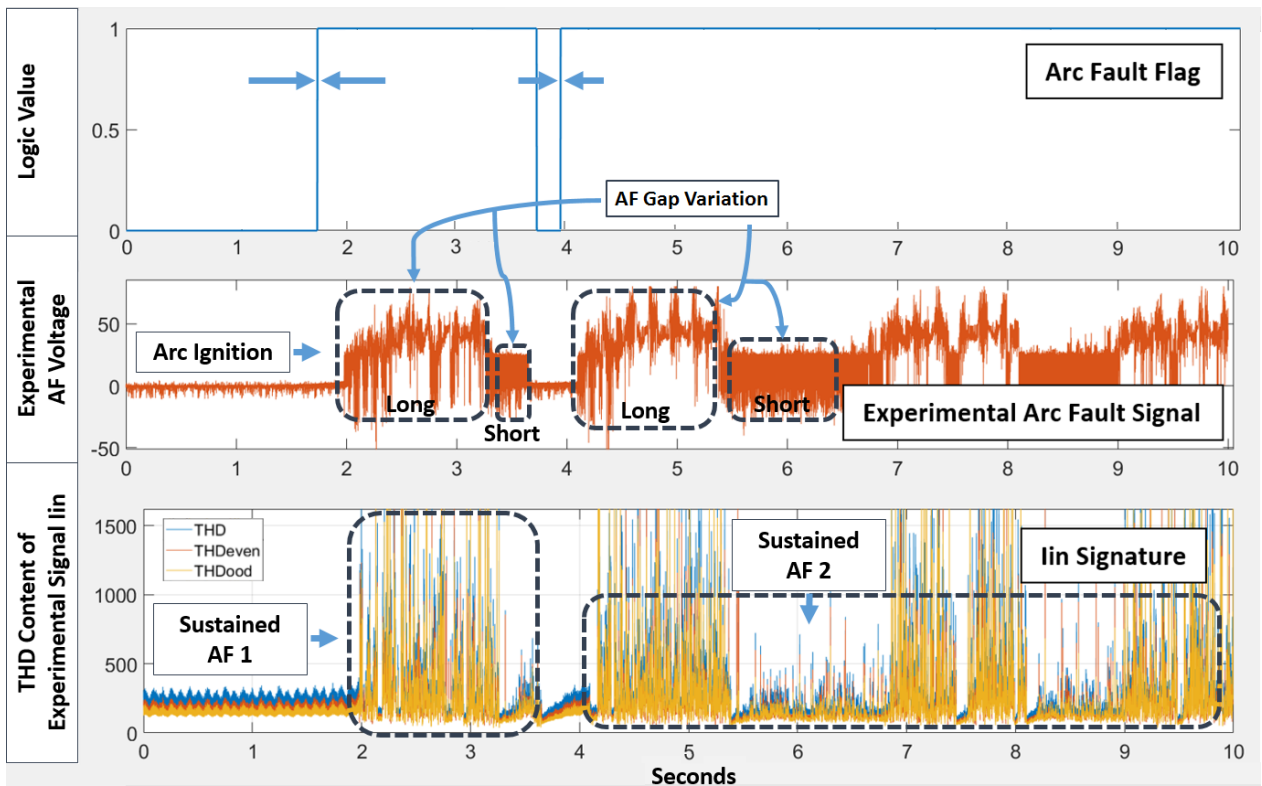


Figure 21. Multiple AF scenario with a 47Ω load.

Pour le cas du moteur comme charge, trois défauts sont générés dans le système. En Fig. 22 on observe que l'algorithme détecte sans difficultés tous les défauts. Néanmoins pour cette charge au moment de défaut le moteur s'arrête et redémarre très rapidement tout le long de défaut.

La Fig. 23 présente le comportement de la détection en cas de commutation de charges. Le résultat de détection n'est pas perturbé.

Pour le cas d'une connexion au réseau électrique les résultats de détection sont concluants malgré un retard compris entre 0.3 et 0.6 seconde.

Dans les deux cas on peut observer de légères variations dans le spectre harmonique mais sans conséquences sur l'exactitude de la détection. Ces résultats sont discutés plus en détail à la section 6.6.

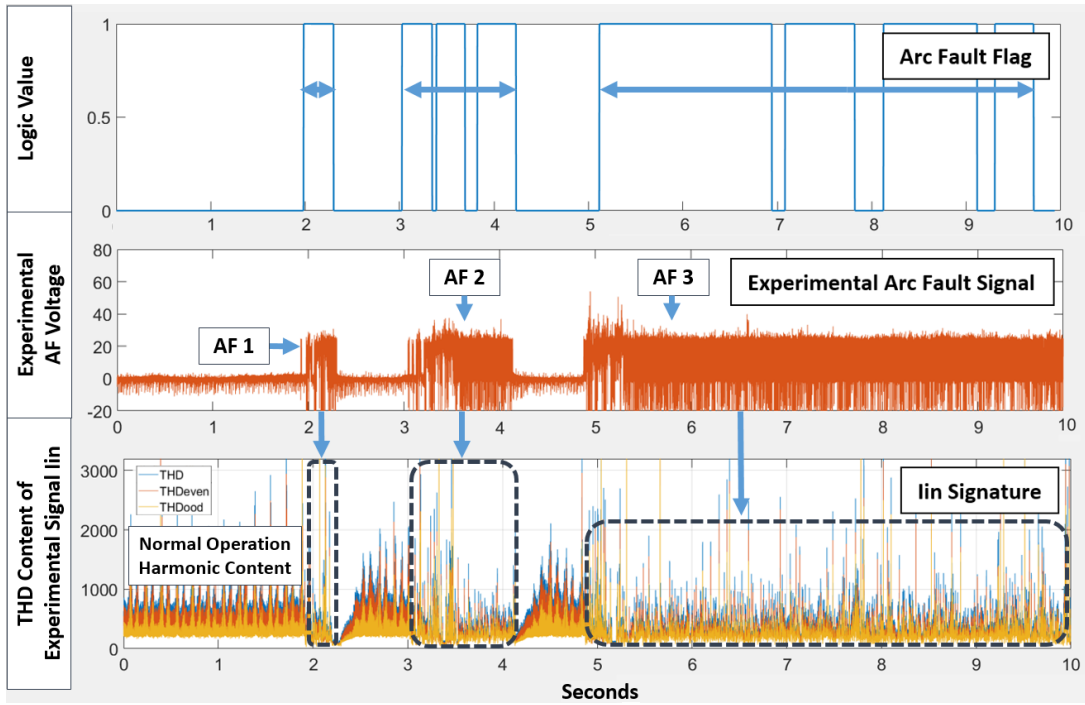


Figure 22. Test 2, algorithm results with 1200 W vacuum load.

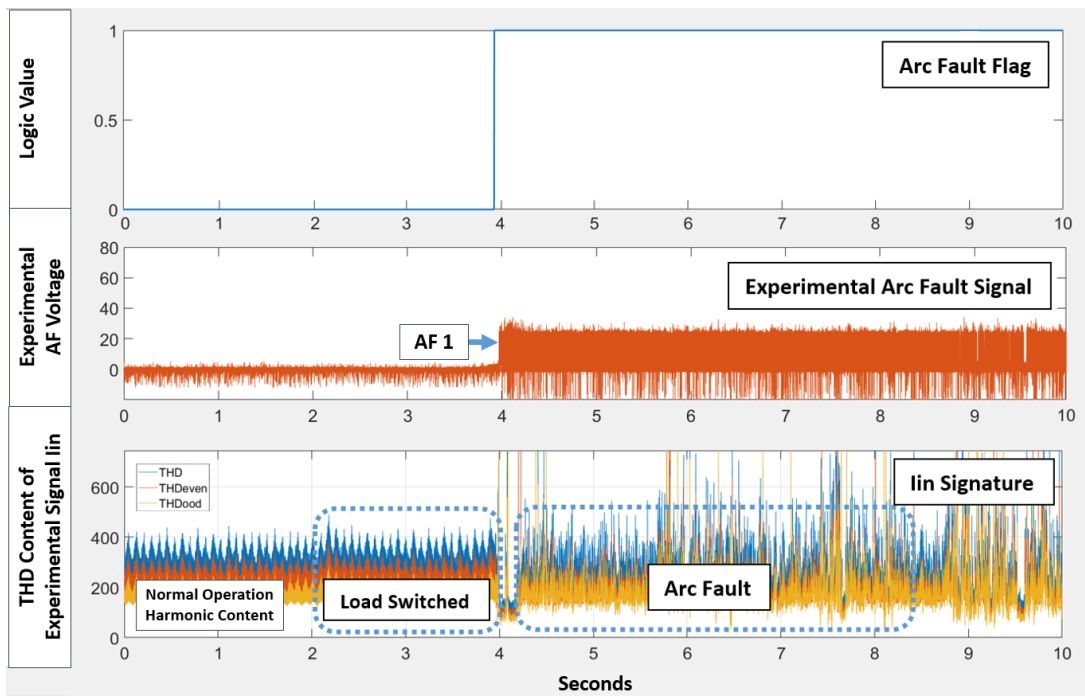


Figure 23. AF test side by side with a resistive switched load and its effect in the THD content.

Symbols and Abbreviation

<i>IGBT</i>	Insulated Gate Bipolar Transistor
<i>AF</i>	Electric Arc Fault
<i>PV</i>	Photovoltaic
<i>AFDD</i>	Arc Fault Detection Devices
<i>DC</i>	Direct Current
<i>AC</i>	Alternating Current
<i>DC/AC</i>	Direct Current to Alternating Current
<i>MPPT</i>	Maximum Power Point Tracking
<i>NCC</i>	Non Current Carrying
<i>CCC</i>	Current Carrying Conductor
<i>EGC</i>	Equipment Grounding Conductor
<i>NEC</i>	National Electric Code
<i>AFCI</i>	Arc Fault Circuit Interrupter
<i>kW</i>	kilowatt = 1000 Watts
<i>RC</i>	Resistive Capacitive
<i>RLC</i>	Resistive Inductive and Capacitive
<i>EIA</i>	Energy Information Administration
<i>AEO</i>	Annual Energy Outlook
<i>NEMS</i>	National Energy Modeling System
<i>MLC</i>	Multilevel Converter
<i>MLI</i>	Multilevel Inverter

<i>NPC</i>	Neutral Point Clamped
<i>FLC</i>	Flying Capacitor
<i>CCMI</i>	Cascade Cells Multilevel Inverter
<i>EMI</i>	Electro Magnetic Interference
<i>UPS</i>	Uninterpretable Power Supply
<i>DETL</i>	Distributed Energy Technologies Laboratory
<i>DFT</i>	Discrete Fourier Transform
<i>Tws</i>	Time Windows
<i>MPWM</i>	Multiple Pulse Width Modulation
<i>SPWM</i>	Sinusoidal Pulse Width Modulation
<i>THD</i>	Total Harmonic Distortion
<i>THD_{even}</i>	Total Even Harmonic Distortion
<i>THD_{odd}</i>	Total Odd Harmonic Distortion

List of Figures

1	AEO report of renewable energy production projected to 2050.	iv
2	Distribution Grid arrangement.	vi
3	Potential Arc Fault in PV panels.	vi
4	Inverter proposed system schematic diagram, buck variant.	viii
5	Cascade cells multilevel inverter topology and control.	viii
6	Simulation results of the DC/AC stage a) <i>VBridge1</i> , b) <i>VBridge2</i> , c) <i>V_{out}</i> , d) <i>I_{out}</i>	ix
7	<i>VBridge1</i> and <i>VBridge2</i> signals obtained using DC/DC Buck variant.	x
8	Voltage and current waveforms of the nine-levels AC output, using buck variant.	x
9	Experimental Test bench.	xii
10	AF Generation device UL1699B.	xii
11	AF Load Study Schematic Diagram.	xiii
12	Multilevel waveforms obtained under AF.	xiv
13	THD decomposition in THD_{even} and THD_{odd} before and after an AF.	xv
14	AF Testing protocol for different loads, with highlighted measuring points.	xv
15	<i>VBridge2</i> harmonics decomposition.	xvi
16	<i>I_{out}</i> THD Decomposition technique.	xvi
17	Summary of Results for AF Tests.	xvii
18	Proposed electric DC AF detection algorithm.	xviii
19	$THDe$ peak saturation analysis before and after an AF.	xix
20	<i>VH2</i> and AF Flag comparison.	xix
21	Multiple AF scenario with a 47Ω load.	xxi

22	Test 2, algorithm results with 1200 W vacuum load.	xxii
23	AF test side by side with a resistive switched load and its effect in the THD content.	xxii
1.1	Schematic diagram of proposed converter in [1].	38
1.2	Schematic diagram of proposed converter in [2].	39
2.1	AEO report of renewable energy production projected to 2050.	48
2.2	Main structure of a PV installation.	49
2.3	Schematic diagram of three-level NPC MLI.	52
2.4	Schematic diagram of four-level FLC MLI.	53
2.5	Schematic diagram of nine-level CCMI.	55
2.6	Output DC voltage and current of a PV array under normal and AF conditions.	56
2.7	The volt-ampere (V-I) characteristics of electric arcs fault.	57
2.8	AF generator schematic diagram.	58
2.9	Main blocks diagram of a PV installation.	59
2.10	PV system current signature tested with two different inverters and without inverter, after an AF scenario.	62
2.11	PV system current signatures tested with two different types of inverter and without it, under AF scenario.	63
2.12	PV system current signatures tested with two different types of inverter and without it, under AF scenario.	63
2.13	Single string current waveform for PV configurations of Table 2.5.1.	64
2.14	String current arc signatures, applying DFT for 0.10s subsections.	65
2.15	PV modules distribution for noise recording in tests of Sandia Labs.	66
2.16	Noise recordings with AF scenario and baseline system in DETL.	66
2.17	<i>Idif</i> waveform from different time window length (a) $T_{sw} = 1$ ms. (b) $T_{sw} = 5$ ms. (c) $T_{sw} = 25$ ms. (d) $T_{sw} = 125$ ms.	67
2.18	Baseline AF signature to perform calculations.	68

3.1	Inverter proposed system schematic diagram, Boost variant.	70
3.2	Inverter proposed system schematic diagram, Buck variant.	70
3.3	Control strategy for boost variant converter; a) $Carry_1$ and $Duty_1$, b) Pulse m_1 c) $Carry_2$ and $Duty_2$, d) Pulse m_2 , e) i_{L_1} and V_{C_1} , f) i_{L_2} and V_{C_2} g) i_{Load} .	73
3.4	Discharging circuit during state 0.	75
3.5	Proposed topology in switching state 3 where $S_1=1, S_2=0$ with highlighted currents paths.	76
3.6	Proposed topology in switching state 2 where $S_1=0, S_2=1$ with highlighted currents paths.	77
3.7	Proposed topology in switching state $S_1=1, S_2=1$ with highlighted currents paths.	78
3.8	Proposed topology buck variant in switching state $S_1=1, S_2=0$ with highlighted currents paths.	79
3.9	Proposed topology buck variant in switching state $S_1=0, S_2=1$ with highlighted currents paths.	80
3.10	Multilevel V_{out} for cascaded converter.	82
3.11	Nine-level SPWM technique.	83
3.12	Cascade cells multilevel inverter topology and control.	84
4.1	Schematic diagram of the smart inverter buck variant.	86
4.2	Simulink resulting schematic diagram of the Fig. 4.1.	87
4.3	Stimulation results of the DC/DC stage a) V_{C_1} b) i_{L_1} c) V_{C_2} d) i_{L_2}	87
4.4	Stimulation results of the DC/AC stage a) $V_{Bridge1}$, b) $V_{Bridge2}$, c) V_{out} , d) I_{out}	88
4.5	Schematic diagram of the inverter boost variant.	89
4.6	Simulink resulting schematic diagram of the Fig. 4.5.	90
4.7	Simulation results of the DC/DC stage a) V_{C_1} b) i_{L_1} c) V_{C_2} d) i_{L_2} e) i_{DC}	90
4.8	Simulation results of the DC/AC stage a) $V_{Bridge1}$, b) $V_{Bridge2}$, c) V_{out} , d) I_{out}	91
4.9	$V_{Bridge1}$ and $V_{Bridge2}$ signals obtained using DC/DC Buck variant.	92
4.10	Voltage and current waveforms of the nine-levels AC output, using buck variant	93

4.11	<i>VBridge1</i> and <i>VBridge2</i> signals obtained using DC/DC boost variant. . . .	93
4.12	Voltage and current waveforms of the nine-levels AC output, using boost variant. 94	
4.13	Experimental test bench.	94
5.1	UL1699B AF generator mechanism diagram	96
5.2	AF generation "Fixed Distance Ignition".	97
5.3	AF Load Study Schematic Diagram.	98
5.4	UL1699B AF generator mechanism diagram	98
5.5	DC/DC stage (Buck variant), with highlighted measuring point.	101
5.6	Current waveform i_{DC} delivered for the DC/DC stage.	101
5.7	Conventional DC/DC boost converter behavior, before and after an AF. . .	102
5.8	Cascade cells configuration for AF testing.	104
5.9	Multilevel waveforms obtained under AF.	104
5.10	Texas Instruments MPPT Prototyping Board.	106
5.11	Schematic diagram for AF testing with AF before MPPT module.	107
5.12	Experimental results of arcing before MPPT module.	108
5.13	Schematic diagram for AF testing with AF after MPPT module.	108
5.14	Experimental results of arcing after MPPT module.	109
6.1	THD study of multilevel waveform.	114
6.2	THD decomposition in THD_{even} and THD_{odd} before and after an AF. . . .	115
6.3	AF Testing protocol for different loads, with highlighted measuring points. .	117
6.4	<i>VBridge2</i> harmonics decomposition.	119
6.5	I_{out} THD Decomposition technique.	119
6.6	<i>VBridge2</i> harmonics decomposition.	120
6.7	I_{out} Harmonic Decomposition.	120
6.8	<i>VH2</i> harmonics decomposition.	122
6.9	I_{out} THD analysis for hammer-drill load.	122
6.10	<i>VH2</i> harmonics decomposition.	123
6.11	I_{out} THD analysis for vacuum load.	123

6.12	Summary of Results for AF Tests.	124
6.13	Distribution Grid arrangement.	126
6.14	Schematic diagram of impedance between the converter and the grid.	128
6.15	Phasor-diagram of the voltages and currents of the single-phase inverter.	128
6.16	LCL coupling filter schematic.	131
6.17	Nine level inverter voltage and LCL coupling filter smoothed voltage.	131
6.18	<i>THDe</i> Analysis of <i>VH2</i> before and after an AF.	133
6.19	<i>THDe</i> peak saturation analysis before and after an AF.	134
6.20	<i>VH2</i> and AF Flag output comparison.	134
6.21	<i>THD</i> Analysis of lin.	135
6.22	Proposed electric DC AF detection algorithm.	137
6.23	Single AF with a 22Ω load, constant electrodes spacing, detection algorithm result.	141
6.24	Single AF with a 22Ω load, variable electrodes spacing, detection algorithm result.	142
6.25	Multiple AF scenario with a 47Ω load.	143
6.26	Multiple AF scenario with a 47Ω load.	143
6.27	Test 1 with RL of 22Ω and $5mH$ load.	145
6.28	Test 2 with RL of 22Ω and $5mH$ load.	145
6.29	Test 3 with RL of 22Ω and $31mH$ load.	146
6.30	Test 4 with RL of 22Ω and $31mH$ load.	146
6.31	Test 5 with RL of 22Ω and $51mH$ load.	147
6.32	Test 6 with RL of 22Ω and $51mH$ load.	147
6.33	Test 1 algorithm results, 1200 W vacuum load.	148
6.34	Test 2 algorithm results, 1200 W vacuum load.	149
6.35	Test 3 for Vacuum cleaner of 1200W.	149
6.36	AF test side by side with a resistive switched load and its effect in the THD content.	150

6.37	AF test 1 with coupling LCL filter.	152
6.38	AF test 2 with coupling LCL filter.	152
6.39	AF test 3 with coupling LCL filter.	153
6.40	AF test 4 with coupling LCL filter.	153
6.41	Test 1 - fast radiation fluctuation in the DC input source.	155
6.42	Test 2 - fast radiation fluctuation in the DC input source.	155
6.43	Test 3 - slow radiation fluctuation in the DC input source.	156
6.44	Test 4 - slow radiation fluctuation in the DC input source.	156
A.1	Schematic diagram of an ungrounded PV system.	175
A.2	Schematic diagram of a grounded PV system.	175
A.3	RC model representation of PV panel.	176
A.4	Potential points of internal fault in a PV panel	178
A.5	Potential points of fault in a PV array	178
A.6	Arc Fault damage in a 10 kW installation, due to inappropriate AF handling.	179
A.7	V-I characteristics curves of AF for different materials of electrodes.	181
A.8	V-I AF ignition curve.	183
B.1	Design of isolated double buck converter.	186
B.2	Developed double DC/DC buck converter.	186
B.3	Design of isolated double boost converter.	187
B.5	Developed double DC/DC boost converter (left) and full H bridge (Right).	187
B.4	PCB Design of the full bridge for the DC/AC stage.	188
C.1	Fourier representation of a square waveform as the sum of a series of sinusoidal waves.	193

List of Tables

0.0.1 Test Bench Equipment.	xi
0.0.3 AF Algorithm testing with different loads.	xx
1.1.1 Single Sourced Converters Comparison	40
2.5.1 PV Configurations.	65
3.2.1 Boost Variant Switching States.	72
3.2.2 Buck Variant Switching States.	79
3.3.1 Stepping Logic for a Nine-Level Converter.	82
4.2.1 Simulation Components Values.	88
4.2.2 Component Values and Settings.	92
5.3.1 Test Bench Equipment and Values.	100
5.5.1 Experimental Values for MPPT Test.	106
6.7.1 AF Algorithm testing with different loads.	140
C.1.1 Waveform Symmetry Characteristics.	193

Contents

Symbols and Abbreviation	xxiii
List of Figures	xxv
List of Tables	xxxi
1 Introduction	36
1.1 PV Converters	37
1.2 Electric DC Arc Fault Detection	40
1.3 PV Converters and Electric DC Arc Detector	42
1.4 Objectives	43
1.5 Justification	43
1.6 Chapters Description	44
1.7 Results of this Research	44
2 Inverter for PV Applications and electric DC arc Fault Detection	47
2.1 Introduction	47
2.2 Context of this Study	47
2.3 Photovoltaic Installation Structure	48
2.3.1 Neutral Point Clamped Multilevel Inverter	51
2.3.2 Flying Capacitor Multilevel Inverter	52
2.3.3 Cascade Cells Multilevel Inverter	53

2.4	Arc Fault Modeling	55
2.5	Arc Fault Detection Techniques	59
2.5.1	Spectrum Analysis Detection Technique	60
3	Inverter Proposal for PV Applications	69
3.1	Main Structure of the Proposed Inverter Topology	69
3.2	Development of the DC/DC Stage	70
3.2.1	Isolated Double Boost Converter for DC/DC Stage	71
3.2.2	Isolated Double Buck Converter for DC/DC Stage	77
3.3	Multilevel DC/AC Stage	81
3.3.1	DC/AC Proposal Operational Principle	81
3.3.2	Nine-Level SPWM Modulation	83
4	Inverter Simulation and Experimental Results	85
4.1	Introduction	85
4.2	Simulation Results	85
4.2.1	Inverter Buck Variant	86
4.2.2	Inverter Boost Variant	88
4.3	Inverter Experimental Implementation Results	91
4.3.1	Inverter Buck Variant	91
4.3.2	Inverter Boost Variant	92
5	Analysis of Internal Signal Perturbations in DC/DC and DC/AC Converters Under AF	95
5.1	Introduction	95
5.2	DC Arc Fault Generation	96
5.2.1	Series Arcing Test Connection	96
5.3	Converter Configuration for Arcing Test	98
5.4	Converter Behavior under DC Arc Fault	99
5.4.1	DC/DC converter	99

5.4.2	DC/AC converter	103
5.5	Arc Fault Influence in a MPPT Tracking System	105
5.5.1	MPPT Arc Fault Test Considerations	105
5.5.2	Single Phase Arcing before MPPT Module	106
5.5.3	Single Phase Arcing After MPPT Module	108
6	Study of Harmonics Decomposition Technique in Both PV Isolated and Interconnected Systems Using Experimental Signals	111
6.1	Introduction	111
6.2	Harmonics in AC Systems Under Normal Operation	112
6.3	Signals Analysis Guidelines for Stand Alone System Tests	115
6.4	AF Influence Study in a Stand Alone Isolated PV System	118
6.4.1	THD Case (1) - Resistive and low inductive load (22ohms + 20mH) .	118
6.4.2	THD Case (2) - Resistive and strong inductive load RL Load (22ohms + 141mH)	119
6.4.3	THD Case (3) - 1200W Hammer-Drill Test	121
6.4.4	THD Case (4) - 1200W Vacuum Cleaner Test	121
6.4.5	Stand alone test conclusion	124
6.5	AF Influence Study in a Grid Synchronized PV System	125
6.5.1	Introduction	125
6.5.2	Grid Interconnection Concepts and Filtering Theory	126
6.5.3	Coupling LCL Filter Design Procedure	129
6.5.4	Simulation results of the Designed LCL Filter	131
6.6	Sliding Window Decomposition Analysis	132
6.7	Performance of the Proposed THD Decomposition Technique with Sliding Window	136
6.7.1	Introduction	136
6.7.2	Stand Alone Isolated PV System Study	138
6.7.3	AF Detection performance in a stand alone scenario	139

6.7.4	Detection Results for Stand Alone and Grid Connected Systems . . .	139
6.7.5	Resistive variation Load AF scenario	150
6.7.6	Grid Synchronized PV System Study	151
6.7.7	Irradiation changes in the input source	154
7	Conclusions	157
7.1	Achievements of this Work	158
7.2	Future Research Works	159
	References	161
A		174
A.1	Definition of Ground Faults	174
A.2	Line to Line Faults	176
A.3	PV Arc Faults	177
A.4	Historic Back Ground	179
B		185
B.1	Smart Inverter PCB Conception	185
B.1.1	Conception of the Isolated Double Buck Converter Board	185
B.1.2	Conception of the Isolated Double Boost Converter Board	186
B.1.3	Conception of Full H Bridge for DC/AC Stage Board	188
C		189
C.1	Fourier Series	189
C.1.1	Periodic Functions	189
C.1.2	Even and odd Functions	190
C.1.3	Trigonometrical Fourier Series	191

Chapter 1

Introduction

In recent years, the photovoltaic (PV) market has grown remarkably, especially in the last few years thanks to the various stimulating factors such as a drop of production costs and numerous governmental support and initiatives. That promotes the use of clean energy generation. These stimulating factors make the return of investment of a PV installation more and more interesting.

However, like all other industrial processes, a PV system can be subjected, during its lifespan, to various faults and anomalies that lead to a decrease in the system performance and even to total unavailability of the system. All these adverse consequences will reduce productivity, and thus the profit of the installation. Is for this reason that a next-generation power converter destined to the interface of PV generation should integrate the main features for regulation, power tracking, and protections, making every system more reliable.

1.1 PV Converters

In order to set a proper background for the development of this thesis proposal, the state of art for PV converters and arc faults protection are studied, in a manner that it can be determinate which are the best suited measures of design for this proposal.

PV inverters are the basic electronic component of PV energy generation, and because of this, many topologies have been studied and proposed achieving the interfacing PV module(s) with the grid, this by injecting a sinusoidal current into the grid. In the past the grid-connected stage was usually line commutation by means of thyristors, involving many current harmonics and poor power quality.

The undesirable large amount of harmonics was the reason of new multilevel inverter topologies and system layouts. That make the combination of multiple blocks in order overcome the power quality needs of the grid. These converters make use of solid state switching devices such as IGBT's in combination with capacitors or diodes to create multiple voltage levels across the topology which are controlled to output an AC semi sinusoidal waveform, which harmonic content is lower than conventional inverters. Nonetheless protection requirements by the standard NEC 690 demands that the PV modules shall be grounded and monitored for ground faults when reaching a maximum output voltage of the PV's.

Since this is just one example of common protection in PV system, that external devices need to be addressed. Nowadays, detection techniques to prevent a wider scope of potential catastrophic faults are based in frequency analysis.

A comparison between various recently proposed DC/AC multilevel converters, mainly based on a single DC source, is presented in Table 1.1.1. The characteristics that are considered for the selection of these topologies where the number of IGBT's, diodes, inductors and capacitors involved, but also the number of levels achieved by the topology, the elevation capacities of the proposals and the use of galvanic transformers.

The first example is the converter in [3] that is capable of achieving a nine-level output with twelve IGBT's and is a transformerless topology, the inconvenience of this proposal is that the input voltage has to be always higher than the desired output since is based in two modified buck converters.

In references [3], [4] and [5] the converters are able to generate a nine-level output, many of these converters produce a higher total harmonic distortion (THD) and use more elements.

The actual tendency in multilevel converter development is to use the minimum number of components and improve reliability and functionality of the system. As part of the most recent developments the work in [1] is able to achieve a seven-level AC output by employing ten IGBT's, the topology presented in Fig. 1.1 consist of cascading two three-level flying capacitor inverters with a half-bridge module in between, as a particular condition, this topology needs three pre-charged capacitors at $V_{dc}/2$, $V_{dc}/3$ and $V_{dc}/6$, respectively.

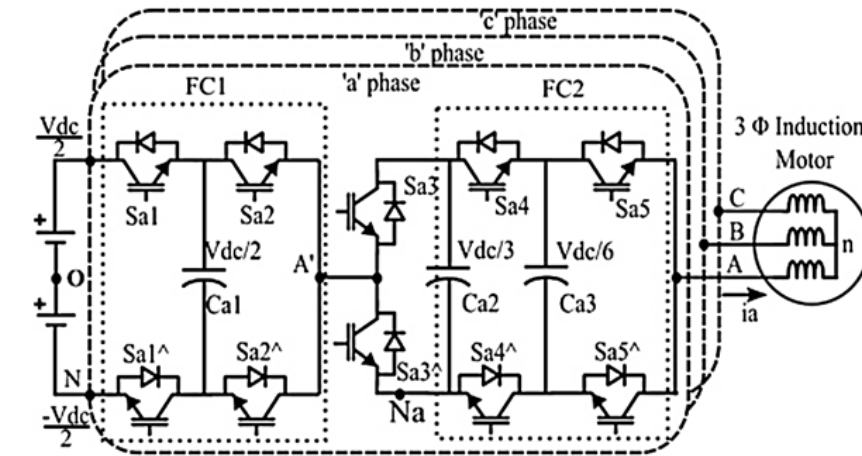


Figure 1.1. Schematic diagram of proposed converter in [1].

The topology presented in [6] may be attractive considering the number of components employed, and also because of the elevation capacity but a transformer is required as presented in Table 1.1.1. The elevation capability is only present in [6–8].

In [9] an asymmetrical cascade cells configuration is implemented replacing one of the voltage

sources by a capacitor accompanied by a voltage balancing control. Due to the symmetrical voltage level needed between the capacitor and the input source, the converter can only achieve five levels which along with [2, 10, 11] are the topologies that generate the minor number of levels increasing considerably the THD.

Of the few proposals in literature, with an elevation capability, [7] and [8] offers a well balanced range of features such as seven-level and no use of transformer, but they are surpassed by [3], [4].

In [11] and [12] is proposed a similar replacement of a DC source by a capacitor similar to [9], nonetheless, stable operation in this type of converters can be challenging especially if a high power is demanded as explained in [12].

In [2] a five-level converter with even less IGBT's is presented in Fig. 1.2, but as the proposals in [2, 9, 11, 12] one of the DC sources is replaced with a capacitor to make the converter operates.

The techniques presented in [2] and [6], uses a galvanic transformer, therefore they are not a suitable option to be implemented compared to transformerless techniques, such as those presented in [1-4, 7-13]

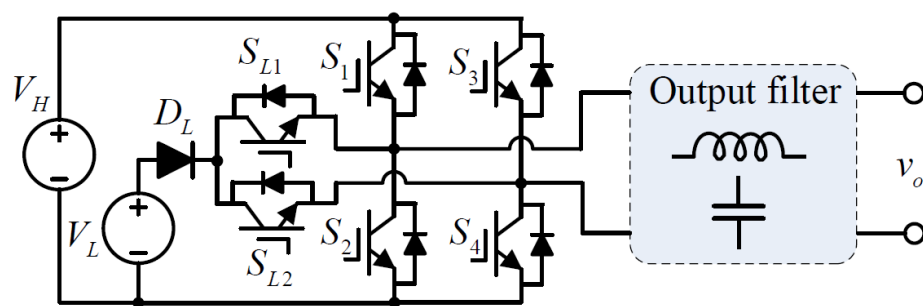


Figure 1.2. Schematic diagram of proposed converter in [2]

In Table 1.1.1 are presented developments from year 2009 to 2019, the criterion to include these topologies are, the number of levels generated, operation from a single source, that is transformerless, and that employs the fewer amount of components possible to achieve the task.

According to this analysis of literature, it's clear that the recent developments in PV inverters have the tendency of developing multilevel inverters with a reduced number of IGBT's and achieving the major number of levels possible, always avoiding the use of transformers. Considering this, in this research work is proposed a nine-level multilevel inverter with a novel DC/DC stage that allows to perform the energy conversion with fewer components and achieving more levels than the analyzed topologies.

TABLE 1.1.1. Single Sourced Converters Comparison

Publications	Year	No.	No.	No.	No.	No.	No.	Elevation	Continous
		Levels	Transformer	IGBTs	Capacitors	Indutors	Diodes	Factor	Current
[2]	2017	5	0	8	1	0	4	None	None
[1]	2016	7	0	10	3	0	0	None	cap&cell
[3]	2015	9	0	12	2	2	4	None	None
[4]	2014	9	0	11	3	1	4	None	None
[13]	2014	7	0	10	4	1	0	None	None
[6]	2014	7	1	8	3	2	5	2:1	None
[9]	2013	5	0	8	1	0	0	None	None(absorb)
[10]	2012	5	0	8	2	0	0	None	cap&cell
[7]	2011	7	0	7	4	10	10	2:1	None
[8]	2011	7	0	15	3	11	11	3:1	None
[11]	2009	5	0	8	1	0	0	None	cap&cell
[12]	2009	7	0	8	1	0	0	None	cap&cell
[5]	2009	9	4	9	0	0	0	None	Yes

1.2 Electric DC Arc Fault Detection

In this section will be presented the fundamental definitions of an electric arc fault (AF), the different types of possible AF in PV panels, the literature approaches to model this phenomenon based on implementation results, also will be analyzed the actual normative

that helps in the development of efficient AF detectors along with recent proposals to achieve successful detection.

An AF is a high power discharge of electricity between two or more conductors. This discharge translates into heat, which can tear down the wire's insulation and possibly trigger an electrical fire. These AF can range in power from a few amps up to thousands of amps high and are extremely variable in terms of strength and duration. Common causes of arc faults include faulty connection due to corrosion and faulty initial installation.

Arc faults can be classified mainly in three categories. Series, parallel and grounding arcs. Generally, parallel arcs can be considered as short circuit effects and they are characterised by high levels of current. On the contrary, in the case of a series arc, the current level is limited by the presence of the load in series with the arc itself. While the electrical circuit has a ground connection, the line-to-ground arc occurs when the arc flows through a grown path and in most cases it can coexist with either series and parallel arcs [14].

During last years, the main normative for arc protections, in order to have safer PV implementation, has been the normative by UL1699B. This first standard for AF detection appears more than a decade ago as the normative UL1699, and soon after as a second and more detailed revision UL1699B where recent research and development of novel Arc Fault Detection Devices (AFDD) are based [15].

Arc faults can appear in both systems, direct current (DC) and alternating current (AC) systems. The aims of this bibliographic study are to analyze the detection and prevention methods oriented for AF in DC systems using PV panels.

The principal methods that have gained popularity to achieve DC AF detection are, harmonic content based detection, low pass filter, drop voltage window, current drop and frequency comparison, current limiting, among other. These type of detection algorithms will be presented in the next chapter.

The most common DC arc faults are classified as: ground fault, line to line fault, hot spot formation, polarity mismatch, PV arc fault, open fault, bypass diode and dust/soil formation in a PV array. Where the ground fault, line to line fault and PV arc fault are the mayor responsible for what is called a catastrophic failure [16].

1.3 PV Converters and Electric DC Arc Detector

With the advantage of converters for PV applications can be possible to use the capabilities of the converter to identify electric DC arc faults. By keeping this scope in mind, the PV inverter project is conceived and developed in this thesis.

In order to fully understand the many components present in an PV installation, the role of each stage and the possible types of faults related to them, an conscious literature analysis of both, power electronics converters and AF are required.

Some international companies such as Hager, Texas Instruments, Schneider Electric, among others have developed protection systems against AF, which under simple operating conditions presume to be able to detect this type of faults, however, these devices commonly make use the current signature of the DC bus as a detection reference. This implies that detection will be affected by the connected load, the type of converter used and the maximum power point traking (MPPT) algorithm employed, as has already been demonstrated by authors such as J. Johnson from Sandia National Laboratory US [17]. In addition to this complex subroutines must be processed in short time, which implies the use of processors with greater capacity, thus increasing the cost of protection.

Nonetheless has to be highlighted the fact that by the addition of this type of protection adds external components to the PV system which is discouraged because this increase the number of possible failure points. It's for this reason that a detection system integrated into the converter is an option since it's not necessary to add any component to the installation, it facilitates the correct detection since it provides numerous internal measurement points that

allow determining, in a more precise way the nature of the fault. Not to mention the reduction of costs given that the converter is an essential part of the PV system, the acquisition of this protection is seeming less for the user.

1.4 Objectives

1. The main objective of this research project is to develop, simulation and implementation, of a power electronic inverter for PV applications that will achieve a higher number of levels with a reduced number of components.
2. To propose an electric DC arc fault detection technique base on the operation of the proposed PV inverter.
3. Develop an electric DC arc fault generator based on the UL1699B.
4. Validate the proposed PV inverter and the DC arc fault detector under different load conditions and arc fault locations.

1.5 Justification

The world leading tendency is to develop PV inverters with better performance, achieving this by generating a high number of levels with a reduced number of components. For this reason, the proposal of a transformerless PV inverter that generates a low harmonic nine-level AC output is presented, optimizing the interface of PV panels. The arc fault problematic is a well documented problem, for this reason, the PV inverter also integrates a novel DC arc fault detector that is critical in order to avoid catastrophic faults that have the potential of damaging a whole PV installation.

1.6 Chapters Description

Chapter 1 - The aim of this chapter is to examine the context of this thesis in the areas of power electronics and electric arc fault detection.

Chapter 2 - This chapter is dedicated to analyzing the bases for modeling of the main structure of the PV inverter, and also analyzes the historical background of arc faults and the popular detection techniques.

Chapter 3 - The guidelines, characteristics, and design of the newly developed DC/DC and DC/AC conversion topology for the PV inverter are described in detail in this chapter.

Chapter 4 - In this chapter the validation of the PV inverter with simulation and experimental results, using matlab simulink and the experimental test bench are presented with detail.

Chapter 5 - In this chapter the detection hypothesis is validated in experimentation by generating arc faults in different configuration following the UL1699B guidelines, which lay the foundations for the proposed detection technique, also detailed in this chapter.

Chapter 6 - In this chapter the concrete results of this research, the future works proposal and the main contribution of this research are presented.

1.7 Results of this Research

The results obtained throughout this period of research are presented bellow:

Journal Articles

1. B. Vidales, J. L. Monroy-Morales, J.R. Rodríguez-Rodríguez, M. Madrigal and D. Torres-Lucio, "A transformerless topology for a micro inverter with elevation factor of 1:10 for photovoltaic applications," *International Journal of Electrical Power and Energy Systems*, ELSEVIER, Volume 109, June 2019, Pages 504-512, ISSN 0142-0615.

International Congress Articles

1. B. Vidales, D. Torres-Lucio, M. Madrigal, P. Schweitzer, and S. Weber, "Analyse du comportement des Systèmes Photovoltaïques face aux défauts d'arc électrique", 14 *Colloque sur les Arc Electriques, CAE 2019*, 18-19 mars, Campus Universitaire Lahitolle, Bourges, France.
2. J. Andrea, D. Jung, P. Schweitzer, B. Vidales, E. Calderon and S. Weber, "Simulation of Arcing Fault in PV Panel Network," 2018 *IEEE Holm Conference on Electrical Contacts*, Albuquerque, NM, USA, 14-18 October 2018, pp. 329-335. doi: 10.1109/HOLM.2018.8611743.
3. A. Zavala, B. Vidales, D. Torres and M. Madrigal, "Study, analysis and optimization of multilevel inverters based in a high stepping DC/DC converter for renewable energies," 2017 *IEEE International Conference on Environment and Electrical Engineering and 2017 IEEE Industrial and Commercial Power Systems Europe*, 6-9 June Milan, Italy, 2017, pp. 1-4. doi: 10.1109/EEEIC.2017.7977559.
4. B. Vidales, S. Weber, R. Schweitzer, D. Torres and M. Madrigal, "Smart inverter arc fault protection for photovoltaic power systems," 2017 *IEEE International Conference on Environment and Electrical Engineering and 2017 IEEE Industrial and Commercial Power Systems Europe*, 6-9 June, Milan, Italy, 2017, pp. 1-6. doi: 10.1109/EEEIC.2017.7977839.
5. B. Vidales, M. Madrigal and D. Torres, "High stepping DC/DC topology for voltage source converters in low power renewable energy applications," 2016 *IEEE PES Transmission & Distribution Conference and Exposition – Latin America*, 21-24 September, Morelia, Mexico 2016, pp. 1-5. doi: 10.1109/TDC-LA.2016.7805660.

6. P. Poure, S. Weber, B. Vidades, M. Madrigal and D. Torres, "High step-up DC-DC converter for renewable energy harvesting applications," 2016 *IEEE 16th International Conference on Environment and Electrical Engineering*, 7-10 June, Florence, Italy, 2016, pp. 1-6. doi: 10.1109/EEEIC.2016.7555767.

International Research Internship

1. January 2016 - Dec 2016, Research Stay. In the Institute Jean Lamour, Universite de Lorraine, Nancy, France, Sponsored by CONACYT MIXED SCHOLARSHIP.
2. March - November 2018, and January - May 2019, In the Institute Jean Lamour, Universite de Lorraine, Nancy, France. Sponsored by International Exchange program France - Mexico ECOS NORD 2018 - 2022.

Chapter 2

Inverter for PV Applications and electric DC arc Fault Detection

2.1 Introduction

In this chapter will be presented a state of the art of power electronic converters, and the recent developments that contribute to a better performance in conditioning of DC/DC and DC/AC converters and also the state of art of electric DC arc fault detection technique.

2.2 Context of this Study

In early 2019 the Energy Information Administration (EIA) publishes the Annual Energy Outlook (AEO) where a projection of energy demand for the US are studied and modeled in order to predict with certain grade of certitude how the demand of energy will be from now to 2050, this study is based in the AEO National Energy Modeling System (NEMS), an integrated model that captures interactions of economic changes and energy supply, demand, and prices [18]. According to this study, the generation of energy by means of renewable sources as wind and solar PV are going to be the main energy source of the future, solar PV

will represent a 48 % of the total production and wind generation will 25% by the year 2050, as presented in Fig. 2.1

Electricity generation from natural gas and renewables increases, and the shares of nuclear and coal generation decrease—

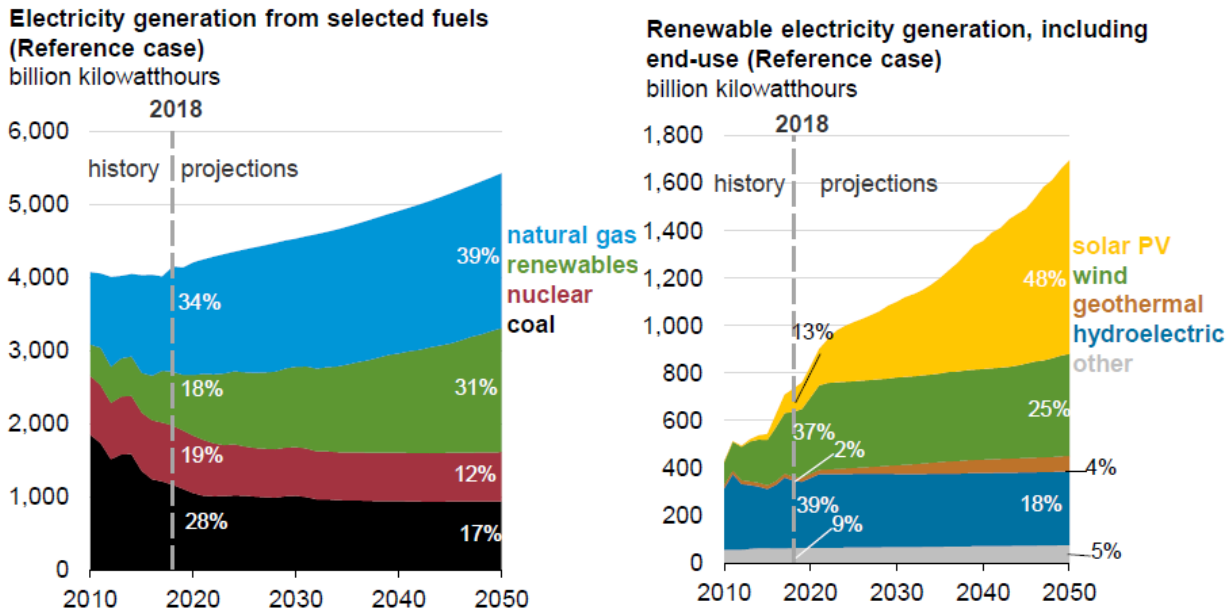


Figure 2.1. AEO report of renewable energy production projected to 2050.

The increasing capacity of solar PV installations has led to research and development of high power converters, required to interconnect the PV panels to the main grid. These power technology converters try to achieve a reduction in the number of components, high efficiency, and protection against faults among others.

2.3 Photovoltaic Installation Structure

The PV installation is built out of several components as presented in Fig. 2.2, however, a fundamental block of this type renewable energy production system is the DC/AC inverter. Since this converter is responsible for the conversion of energy, it is essential that this is performed with the highest possible efficiency index. To achieve this, the DC/AC converters have undergone a constant change over time and with the appearance of new generation components.

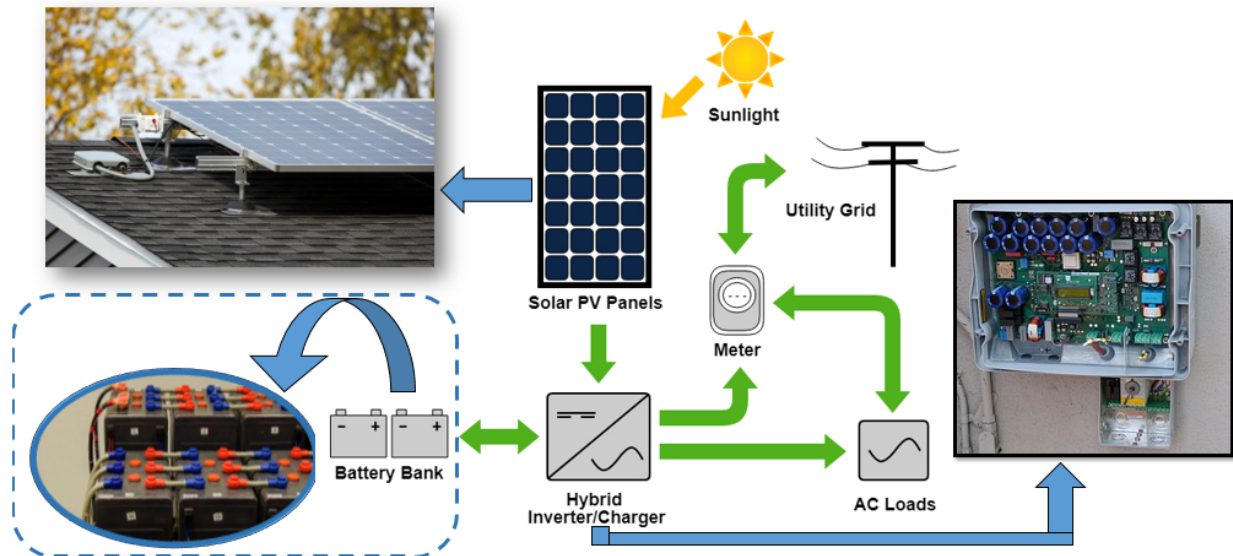


Figure 2.2. Main structure of a PV installation.

The different topologies developed have been strongly influenced by the needs of the industry. This is reflected in the first-ever publication on a three-level inverter [19]. The Multilevel Converters (MLC) were invented with the explicit aim of overcoming the voltage limit of semiconductor devices of that time. The concept of utilizing multiple small levels to perform power conversion was presented over 40 years ago [20], [21]. While the first-ever patent three-level inverters and multilevel inverter (MLI) was in 1983.

The original idea of MLI's was tantamount to connect multiple devices in series and clamp the voltages between them. An early patent appeared in 1975 [22], in which the cascaded inverter was first defined with a structure that connects separately DC-Sourced Full-Bridge cells in series to synthesize a staircase AC output voltage [23].

Following this idea and redesigning the converter with diodes blocking the sources, the diode-clamped MLI was then patented [24], [25]. This inverter was also called the Neutral Point Clamped (NPC) inverter because it was first used in a three-level inverter where the mid-voltage level was defined as the neutral point [23]. One of the main advantages provided by this new NPC inverter was doubling the device voltage without precise voltage matching, thanks to this the topology prevailed during the 1980s [23].

Although the cascade inverter was invented earlier, it had few applications until the mid-1990s. Due to the great demand for MV high-power inverters, the cascade inverter has drawn tremendous attention ever since [23], [26]. Several patented works were suggested for the use of cascade MLI in the regenerative type of motor drive applications [27–30]. However, most of the application in this area has occurred over the last few years. Despite the significant innovations in this area, there is still much more that can be done [31].

Due to the fact that the ML output voltage exhibits lower harmonic distortion in comparison with the two-level voltage, typical problems like stator winding insulation breakdown, bearing failures, and electromagnetic interference (EMI) associated with the high switching frequency can be significantly reduced when using MLCs [31], [32]. In the three-level inverters, the semiconductors have voltage ratings of only $U_{dc}/2$ and an increased voltage power ratio [31, 33–36].

MLCs have been investigated extensively, particularly for MV high-power applications [31, 32, 37–48]. They have been investigated for other applications such as utility interface for renewable energy systems [49–53], high-voltage DC transmission [48], flexible AC transmission system [54], electric traction systems, active power filtering [40], [48], unified power flow controllers, superconducting magnetic energy storage [33], and static synchronous compensators [34], [55–58]. Recently, the use of ML configurations has become more prevalent in the active rectifier field [31], [59], [60].

Among MLCs [38], the following three topologies have been successfully implemented as standard products for MV industrial drives 1) the four-level neutral point clamped (NPC) 2) the four-level flying capacitor (FLC) and 3) the cascade cells multilevel inverter (CCMI) [42], [45], [61]. These configurations are further described in the following sections.

2.3.1 Neutral Point Clamped Multilevel Inverter

For NPC inverter topology [21] the midpoint potential of a capacitive voltage divider in the DC link is used to stabilize the voltage distribution between devices with the help of clamping diodes, D_1 and D_2 presented in Fig. 2.3. The topology adds the zero level to the output voltage waveform and, thus, also serves to reduce its harmonic content. The three-level inverter topology permits operation at double voltage, which also doubles the maximum output power. Furthermore, the capacitors can be pre-charged as a group [23], [38], [41], [46]. The concept can be extended to any number of levels by increasing the number of capacitors and diodes. However, due to capacitor voltage balancing issues, the NPC inverter implementation has been mostly limited to the three-level inverter [62], [63]. This type of inverter is widely used in MV applications and is one of the most commonly applied topologies [38], [41], [62].

It characterizes a relatively small DC link capacitor, a simple power circuit topology, a low component count, and straightforward protection and modulation schemes [64]. Therefore, the three-level NPC is a competitive topology for a large variety of low and medium switching frequency applications. Additionally, the three-level NPC has the highest converter efficiency among the available solutions for the industry [39]. The NPC has found an important market in more conventional high-power AC motor drive applications like conveyors, pumps, fans, and mills, among others, which offer solutions for industries including the oil and gas, metal, power, mining, water, marine, and chemical industries [64–66].

Because all of the phases share a common DC bus, the capacitance requirements of the converter are minimized. For this reason, a back-to-back topology is possible. This configuration for regenerative applications has also been a major benefit, for example, in regenerative conveyors for the mining industry or grid interfacing of renewable energy sources like wind power [49], [67]. Although this topology has a simple circuit, usually, it needs a large inductive capacitive output filter to operate standard motors [38].

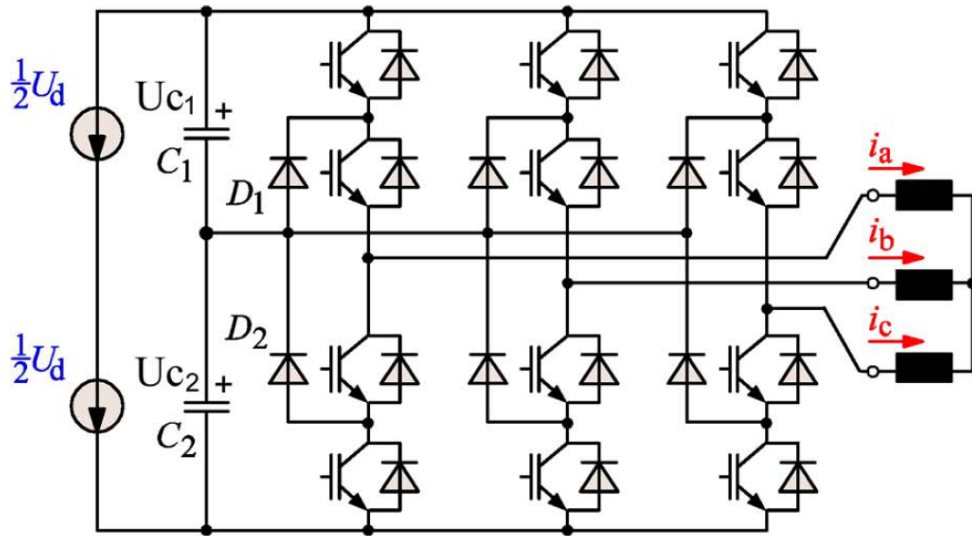


Figure 2.3. Schematic diagram of three-level NPC MLI.

2.3.2 Flying Capacitor Multilevel Inverter

Flying capacitor multiple inverter (Flying Capacitor) shown in Fig. 2.4 is another popular voltage source MLI uses the flying capacitor topology [68]. This topology offers the advantages of MLCs. However, the needs to balance the capacitors voltages and pre-charge the capacitors at the start time, in addition to a larger number of capacitors, is the disadvantages of this topology. The high capacitance values and stored energies of the flying capacitors limit the use of three-level and four-level FLC to high switching frequency applications [69]. In the FLC, the load current charges every capacitor; hence, the respective capacitor voltages change. The resulting changes must be maintained within permissible limits. Thus, the required capacitance increases approximately in inverse proportion to the switching frequency. This makes the FLC topology impractical at very low switching frequencies. Therefore, the stored energy of the flying capacitors and the dimension of the LC inverter output filter is increased by a factor of about 10 (for three-level FLC) and 20 (for four-level FLC) in comparison to three-level NPC [69]. The high cost of flying capacitors at low and medium switching frequencies is the reason that the FLC topology is not competitive in applications that only require low and medium

switching frequencies 1500-1800 Hz [69]. Nevertheless, the symmetrical switches loss distribution and the resulting high first carrier band frequency of the converter voltage make this topology attractive for some applications such as highspeed drives and test benches [39], [41], [65], [69].

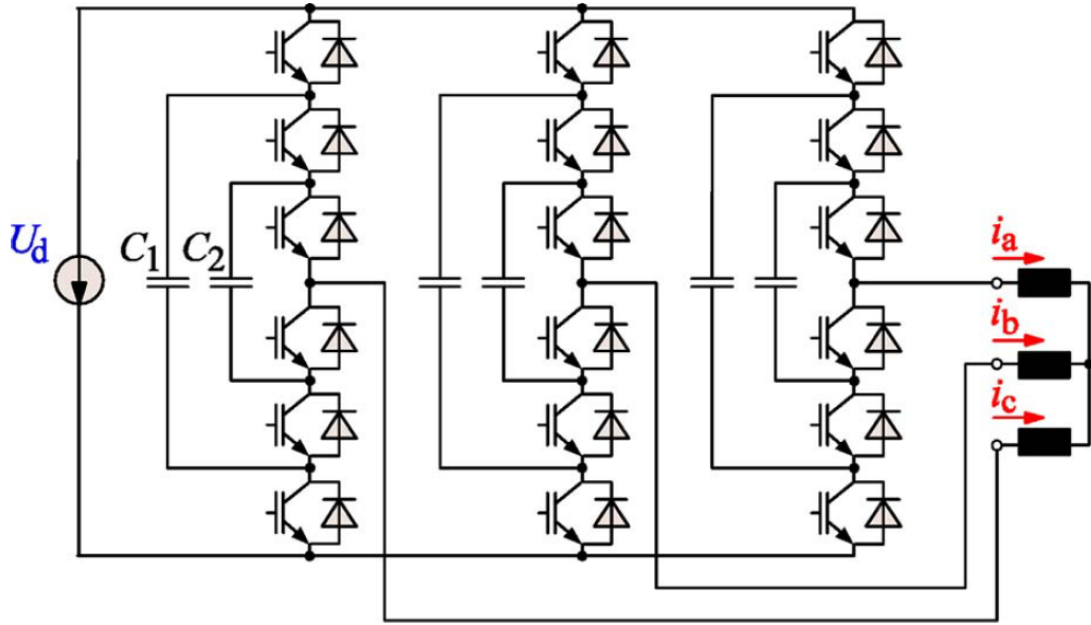


Figure 2.4. Schematic diagram of four-level FLC MLI.

In these applications, the three-level FLC is an interesting alternative to the four-level FLC due to the reduced cost of flying capacitors. At lower frequencies and high converter efficiency, neither topology is competitive compared to the three-level NPC and the five-level CCMI [38], [39].

2.3.3 Cascade Cells Multilevel Inverter

Cascade cells multilevel inverter is a topology that connect in series H-bridge that appeared in mid 1970s [22], and several recent works were registered [70], [71], [42]. Since this topology consists of series power conversion cells, the voltage and power level may easily be scaled [31]. However, a disadvantage is the large number of required isolated power supplies. However, the cells can be supplied by phase-shifted transformers (an expensive

solution) in order to provide high power quality at the utility side [31], [42]. The five-level CCMI shown in Fig. 2.5 requires the lowest switch power rating and stored energy of the LC filter. Compared to the three-level NPC, the installed switch power and the stored energy are significantly reduced (even up to 80%) [26], [39]. However, a complicated grid transformer, increased dc-link capacitance compared to the three-level NPC, and the high number of semiconductor devices are its drawbacks [38]. The absence of a common dc voltage bus is an additional disadvantage of the five-level CCMI [38]. The cascaded H-bridge has been applied for high-power and power-quality industrial requirements due to its series expansion capability [65]. This topology has also been used for active filter and reactive power compensation [23], [26], [41], [72], [73], electric vehicles [74], photovoltaic power conversion [51–53], interruptible power supplies (UPSs), and magnetic resonance imaging [65], etc. A hybrid asymmetric MLC is constructed by combining the CCMI with the NPC topologies [38]. Such a combination produces more output voltage levels with the same number of components as a symmetric MLC [38]. Although an H-bridge cell and a leg of the NPC converter provide the same output voltage levels, the hybrid asymmetric ML topology requires a smaller number of separate DC sources and H-bridge cells for the same output voltage levels [38], [40]. This topology can be operated at a low or a high switching frequency for high or low voltage applications. However, the need for a complex input transformer remains, and the control system would be too complex due to its structure therefore, it is not commercially offered [40],[75]. This is also true for the nine-level CCMI, although it is a good topology for manifold MV drives, e.g., high-speed drives [38], [69]. Other interesting and competitive topology try new methods, like combining the basic NPC and half-bridge principles. A five-level topology was proposed, where each phase of the inverter consists of two three-level NPC half-bridges connected in series. One arm is connected to the output terminal and the other is connected to the neutral point. The half bridges are supplied by isolated DC sources, which are often composed of multi-pulse diode rectifiers [76]. The topology was named NPC/H-bridge inverter. Taking into account the reviewed information of PV inverters, the proposal of this research protect is presented in

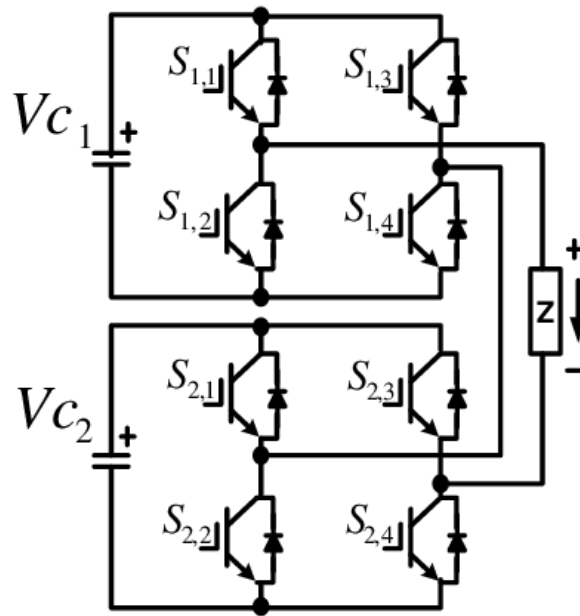


Figure 2.5. Schematic diagram of nine-level CCMI.

chapter 3 and the experimental result in chapter 4. In the next section the overall problematic related to the appearance of AF on PV panels will be discussed.

2.4 Arc Fault Modeling

Arc faults can appear in both types of PV systems new and aged installation, this due to the fact that cable insulators, panels and junction boxes are expose to the elements. Another common cause of fault is due to inadequate installation, this can cause a small separation in the conductors from its connection, producing an AF. Since this malfunction happens in the DC side, the detection can be challenging as will be analyzed in the sections below.

The dielectric constant of an insulating material defines the maximum electric field that the material can withstand before breakdown occurs. A sustained arc results if the energy produced inside the arc is higher than the energy lost due to thermal radiation, light, sound, etc. The dielectric constant of air is approximately 3 V/u, and it depends on surrounding pressure, humidity, presence of impurities, etc.[77], [78].

In addition, the initiation/sustainability of an arc also depends on the size/shape of the electrodes, the air gap between the electrodes, and presence of chemical products from the arc (e.g., melted metals from electrodes, melted/vaporized polymers from glass, wire insulation). An arc is initiated across an air gap when high electric fields ionize air molecules and accelerate the ion toward the opposite electrode. This leads to a high-velocity particle collisions, which generate additional charged particles. This runaway ion generation converts the normally insulating air medium into a conductive medium.

The voltage–current relationship of an arc is highly nonlinear. The transient behavior of a DC parallel arc in a PV array connected to an inverter decrease in voltage and increase of current during the on-set of an electric arc. In the case showed in Fig. 2.6 the arc produces a fall in the DC bus voltage, represented in purple, also the current of the whole array is affected presented in red. This drop is equivalent to the AF current and voltage levels presented in blue and green, respectively.

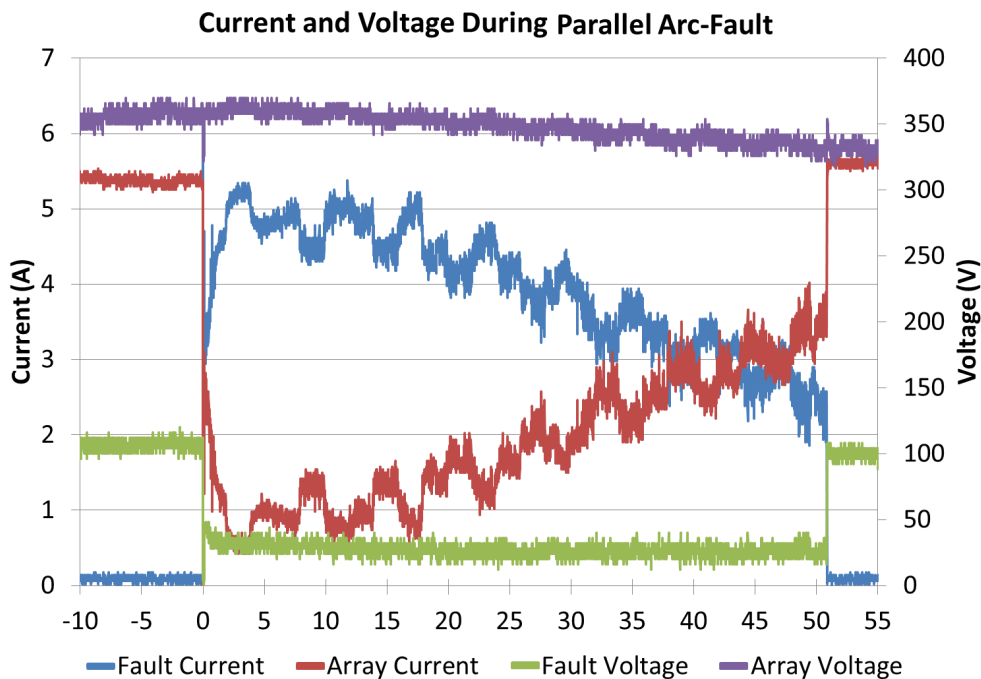


Figure 2.6. Output DC voltage and current of a PV array under normal and AF conditions.

Details of arc characteristics have been widely described in [79], where the V-I curve of an arc is presented and divided mainly into two different regions: inverse and constant voltage

regions. At the onset of an arc, the arc voltage decreases which increase the arc current (inverse region), and after arc power has a tendency to remain relatively constant. The arc voltage increases slightly with the increase in the arc current in the constant voltage region, this is presented in the Fig. 2.7. One very simplified approach to model the arc is measuring

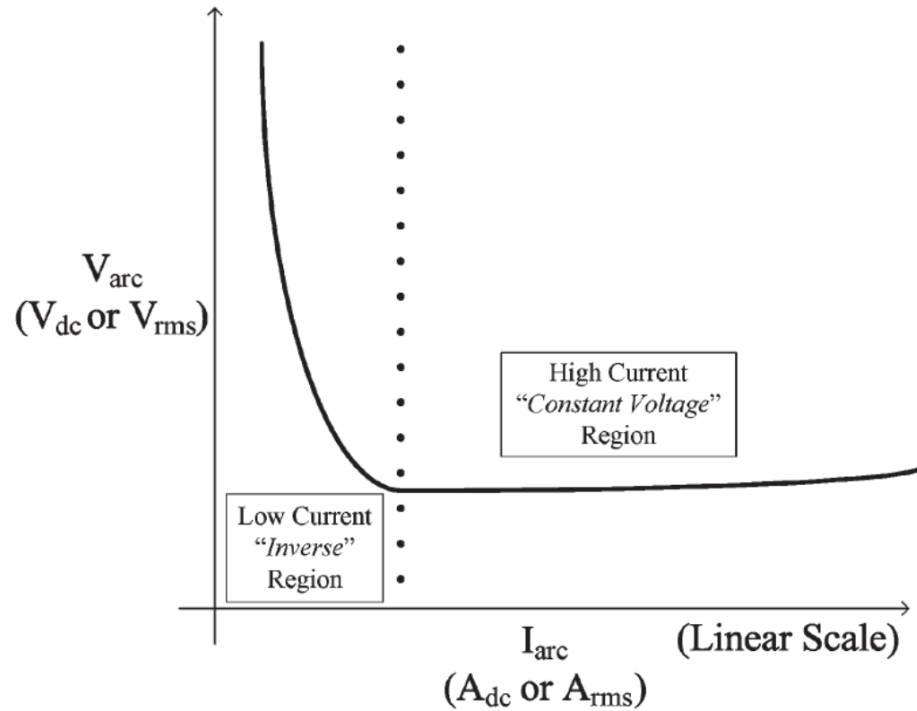


Figure 2.7. The volt-ampere (V-I) characteristics of electric arcs fault.

the average resistance of the arc at steady state deduced from the average values of the arc voltage and current [78]. Approaches with additional details for modeling this nonlinear V-I characteristics of the arc are summarized in [79], in most cases, to determine arc length empirical equations are included to find a relationship between the arc voltage and current. As an example, Yao et al. have proposed a modified Paukert form for describing the V-I relationship of arc in the PV system. As follows [78]:

$$V_{arc} = \frac{a + bL}{I_{arc}c + dL} \quad (2.1)$$

Values a , b , c and d are constants, while V_{arc} , I_{arc} , and L are arc voltage, current, and length, respectively. Two other significant aspects of PV arc faults are arc temperature and burn-through time of CCC insulation. Burn-through time depends on the temperature, power density, metals and adjacent materials, also radiative heating can ignite flammable materials near the arc fault. Therefore, use of fire-retardant materials may help extinguish the arc and abate subsequent fire hazards in a PV array [77]. Fig. 2.8 shows an DC arc fault generator. The circuit of Fig. 2.8 is defined for an arc of fixed length. In the low-current

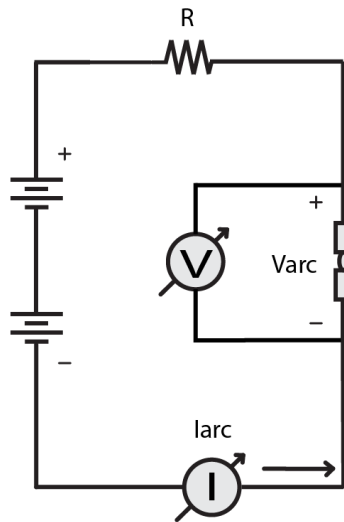


Figure 2.8. AF generator schematic diagram.

region (Limited by the dotted line in Fig. 2.7), the arc voltage drops as the arc current increases, as a result, the arc power tends to remain relatively constant in this region. For larger currents, the arc voltage increases slightly with increasing arc current. In the cases of deep study of AF behavior it exists a transition current, which defines the boundaries between the low and high-current regions that will not be discussed in this work, but more information about arc fault is mentioned in the appendix.

2.5 Arc Fault Detection Techniques

As has been already discussed that series arc faults tend to appear when there is a discontinuity between CCC's. Was discussed as well the locations where AF can appear in the PV panels, In the Fig. 2.9 the schematic circuit of a PV system is presented in order to provide a solid base to further explications and location of AF. In Fig. 2.9 are represented in blocks the main

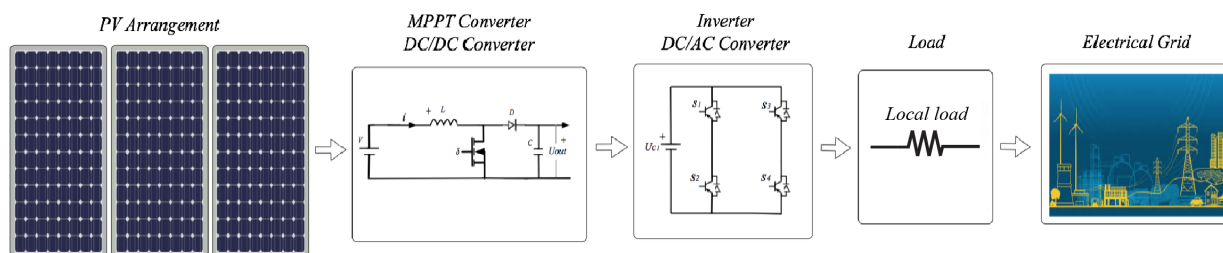


Figure 2.9. Main blocks diagram of a PV installation.

components of a PV installation. The behavior of the system follows a simple principle, and is to transform the solar irradiation received by the panels into profitable electrical energy. Solar panels have a non linear behavior, which means that the constant changes in solar irradiation will be reflected as a change in the output value of voltage and current provided. It exists a point where the maximal power can be extracted from the panels, which refer to a balance between voltage and current where the maximum power transfer is achieved by the panels.

The MPPT DC/DC converter shown in the Fig. 2.9 has the task of receiving the voltage and current generated by the panels and then, according to control algorithm, modify the DC/DC output voltage and current levels by modifying the duty cycle of the DC/DC converter, achieving a constantly track and follow of the maximum efficiency point according to the irradiation received by the panels.

After assuring that the maximum power is extracted from the panels, the DC/AC power inverter has the task to transform this DC energy into AC, this conversion of energy can be achieved in many different ways and with a wide variety of power electronics topologies,

nevertheless in Fig. 2.9 the basic topology (H Bridge) for performing this conversion is presented. Another task related to the inverters role is the synchronization with the electric grid.

The AF detection normally is using a type of algorithms, implemented in an electronic device. These types of algorithms can be developed in many different ways depending of the approach the author employs. Conventionally is perform a frequency analysis were all the harmonic content of signal are displayed and studied, based on this variations they are compared to a reference harmonic content and then be able to recognize if an AF is present in the DC system, this is the method that is proposed in the works of J. Johnson and F. Schimpf [15], [17], [80]. Some techniques to identify the DC arc faults are described below.

2.5.1 Spectrum Analysis Detection Technique

In this type of approach a Fourier analysis is perform in the current signal from the DC bus in order to extract the harmonic content, with the aims of analyzing several kHz bands (at very low frequency or low frequency) in which the baseline signals are significantly increased in the presence of an AF, this is considered one of the conventional methods that can detect DC arc faults.

During the apparition of the AF in a PV system a series of events are follow and it's possible to describe them in five main events:

1. An arc fault triggers at a specific location in the DC string and generates, $1/f$ AC noise presented in Fig. 2.10 with magenta on top of the DC current. This signal travels down the line through the system.
2. As this signal passes through the PV modules and connectors, a variable attenuation occurs in the PV modules and connectors and changes the frequency amplitude (profile) of the electrical noise as it propagates downstream.
3. Phenomena such as antenna effects, crosstalk and RF modifies the signal profile and characteristics even more.
4. The effects mentioned change the original arcing signal that reaches the AFCI, and

depending on the PV cell technology, system topology, metrological conditions, and age of the modules, this signal reaching the AFCI is different from the original arcing signal allowing the arc to pass undetected.

5. Also the inverter noise injected into the PV string. This due to the inverter switchings that generates harmonics from 1kHz to 100 kHz [81].

The Fig. 2.10 presents the frequency behavior of different signals, that represented two systems, one where the signals are represented with purple and blue colors, and second the same signals but this time with an inverter connected to the system [17].

If this two signals of Fig. 2.10 are compared, is possible to identify an important fact that is mentioned in the works of J.Johnson, F. Schimpf and Gab-Su Seo, and is that in the early base bands of frequency is easier to identify the changes on the frequency signature of arc signals. Taking the example of Fig. 2.10 is observed that the two systems have a current frequency signature with a magnitude of around -70 db, when the 2 different power inverters are added to the system this magnitude of change in the both cases to around -40 db and -20 db, respectably. It's important to note that in this comparison the AF event is not yet considerer in the analysis, nevertheless the changes in the very low and low frequency bands is noticeable. In AF case, a similar change in the frequency signature is observed, this represents the base line for the frequency analysis detection method. Depending on the PV system topology, the impact of AF's may vary. In single string tests, the operating DC current and voltage drops initially, because the string impedance suddenly increased from the AF event, this characteristic is explored to evaluate its potential for detection AF's in DC systems as proposed and explored for L. Mackay [14].

This Phenomena has been noticed as well by J. Johnson, although this happens only if measuring the voltage and currents present in a single string, in Fig. 2.11 and 2.12 are presented the signal signatures of a single string for both current and voltage respectably. In this two figures is possible to appreciate the different types of response during an AF event for a system with a resistive load bank and other with an inverter connected.

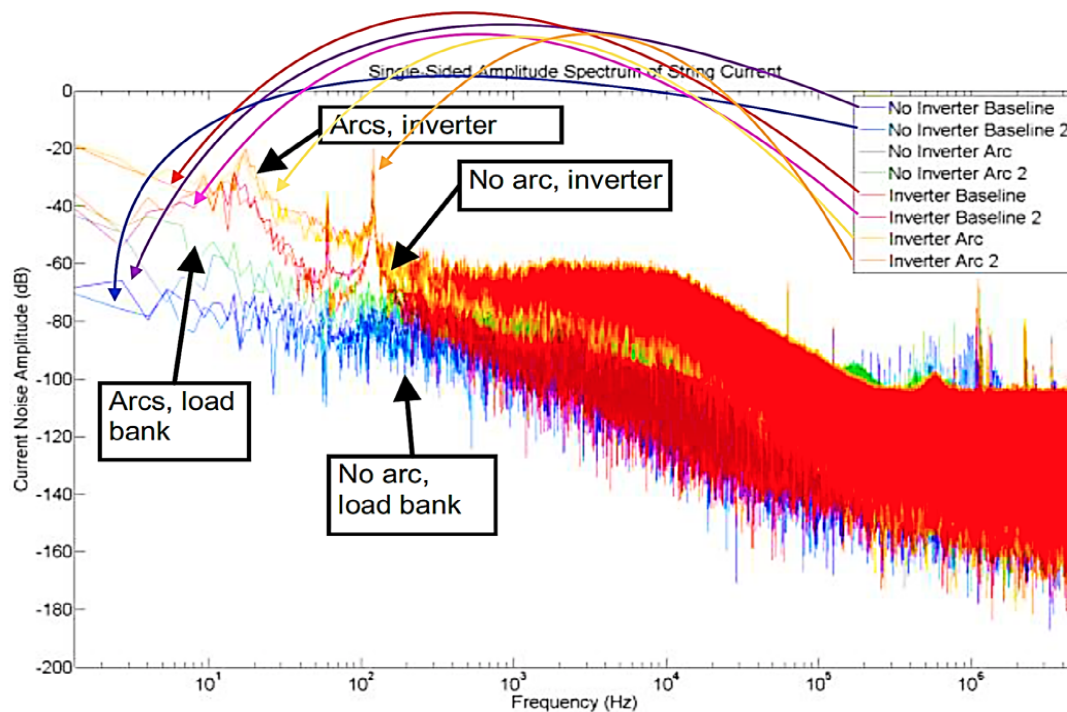


Figure 2.10. PV system current signature tested with two different inverters and without inverter, after an AF scenario.

The signals extracted from the baseline systems are stable and don't present much distortion. On the contrary when an AF appears is easily identified because the current in the string decrease from its nominal value immediately after the arc apparition. This happens also in the case where the system has an inverter connected to it.

In this work is possible to see that the noise that the power inverter injects in the system change the response of the system, the characteristics magnitude of this noise depends of converters topology, switching, frequency, power capacity, etc. To cite and example in Fig. 2.13 present the waveform signatures for six different PV system configurations detailed in Table 2.5.1. To create the ignition of an arc fault, the voltage exceeds the permittivity of free space, current begins flowing between the electrodes, and the gas ionizes to create a plasma. To determine if the initial period of the arc fault contained different frequency content than succeeding time periods, the arcing time domain was subdivided into 0.10 second blocks and the discrete fourier transformation (DFT) of each time subsection was calculated.

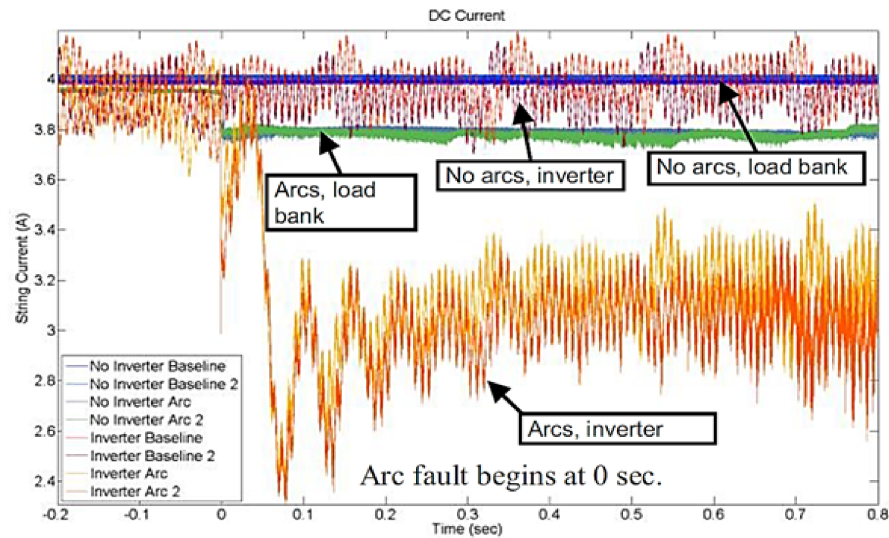


Figure 2.11. PV system current signatures tested with two different types of inverter and without it, under AF scenario.

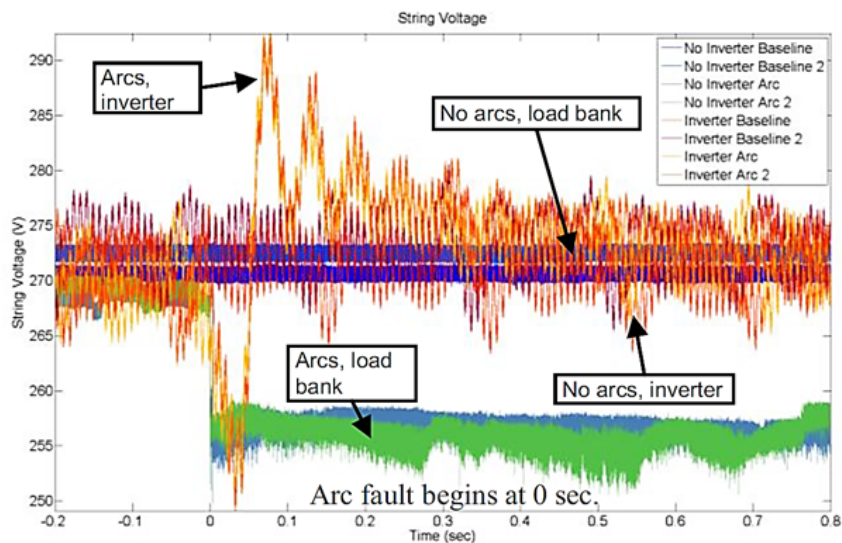


Figure 2.12. PV system current signatures tested with two different types of inverter and without it, under AF scenario.

Shown in Figure 2.14, there was a slight variation in the frequency domain as the arcing time increased. Over most of the frequency domain, and especially between 10-100 kHz, the arcing noise amplitude increased slightly over the duration of the arc fault. Since the arc was generated by separating opposing electrodes, the increase in noise may be due to the increased arc gap.

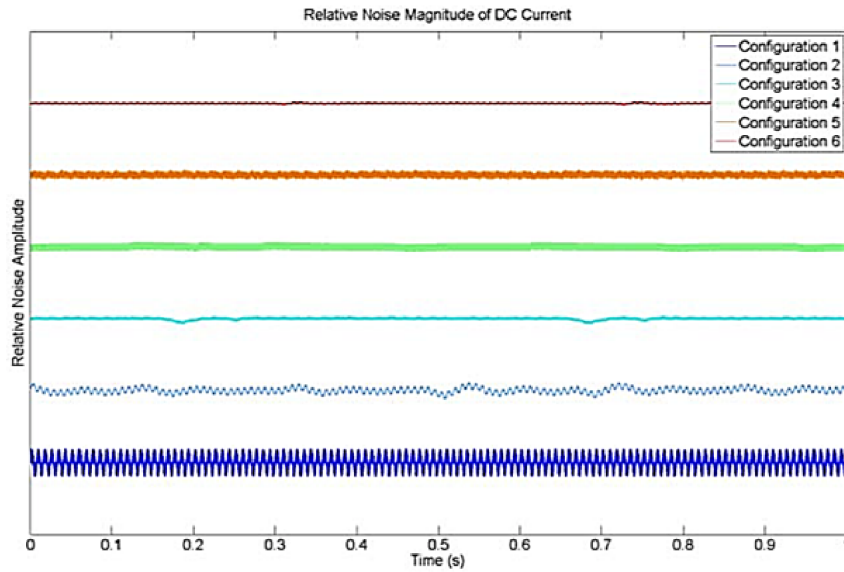


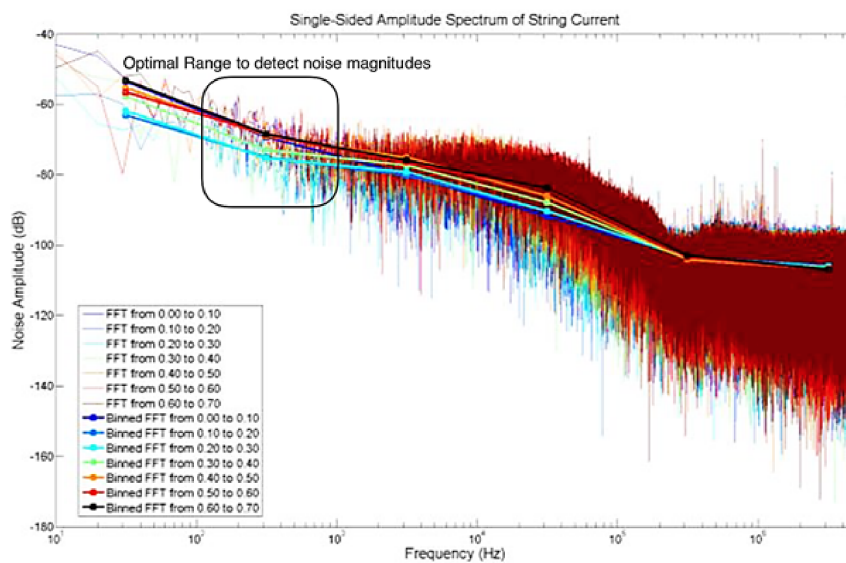
Figure 2.13. Single string current waveform for PV configurations of Table 2.5.1.

It was considered that the location of the arc fault and the location of the detector could affect the measured frequency content. The arc fault generator was located before and after each module in a 6-module string and the arcing current was measured. While the amplitude of all arcing frequencies was significantly larger than the baseline measurements, the location of the arc fault had little effect on the frequency content at the AFDD.

Likewise, when the detector was placed at the end of the string and at a location 30 m further along the conductor, there was no significant effect on the detected frequencies [17].

TABLE 2.5.1. PV Configurations.

Configuration	Inverter	Modules	Strings	Module:String
1	4.8kW	175 W c-Si	4	6
2	20 kW, 3-phase	90 W c-Si	1	21
3	20 kW, 3-phase	80 W c-Si	1	22
4	3 kW	200 W c-Si	4	6
5	75 kW 3-phase	175 W c-Si	8	12
6	4 kW	540 W a-Si, BIPV	3	2

**Figure 2.14.** String current arc signatures, applying DFT for 0.10s subsections.

The noise generated by the arc will also be affected by the material of the PV panel, and by the rated power of each panel, this was noticed by J. Jonson by testing three configurations at the Distributed Energy Technologies Laboratory (DETL), at Sandia National Laboratories. DETL has three subarrays connected to the same 3-phase inverter. The subarrays were composed of four 21 module strings of 90 W c-Si (crystalline silicon) modules, four 22 module strings with 80 W c-Si, and four 22 module 80 W p-Si (polycrystalline silicon) strings each from different module manufacturers and labeled subarray 1, 2, and 3 presented in Fig. 2.15. Baseline measurements and arcing measurements at the centers of the strings were taken.

The binned frequency content Fig. 2.16 illustrates that certain frequency ranges are exceeded

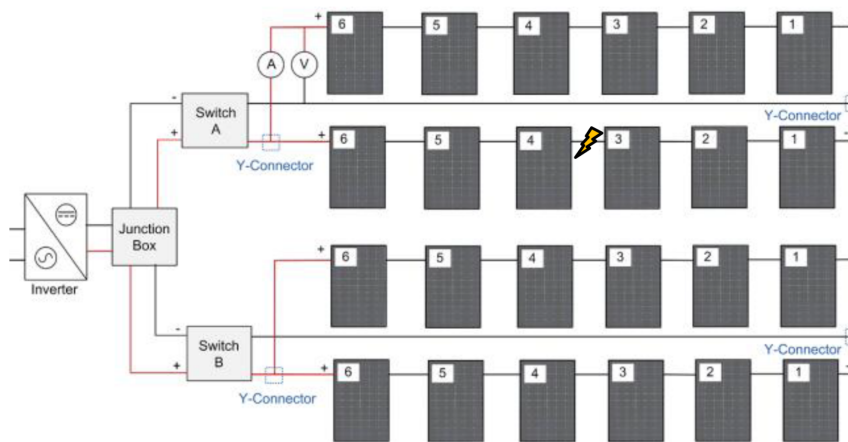


Figure 2.15. PV modules distribution for noise recording in tests of Sandia Labs.

for arc fault detection. From 1-100 Hz and 100 kHz to 5 MHz there is little or no difference in the arcing noise content when compared to the current baseline frequencies. However, for the frequencies between 100 Hz-100 kHz, there is a clear separation between the arcing noise and the baseline for all strings. Thus, it is likely that the same arc detection algorithm could be employed to these three module technologies.

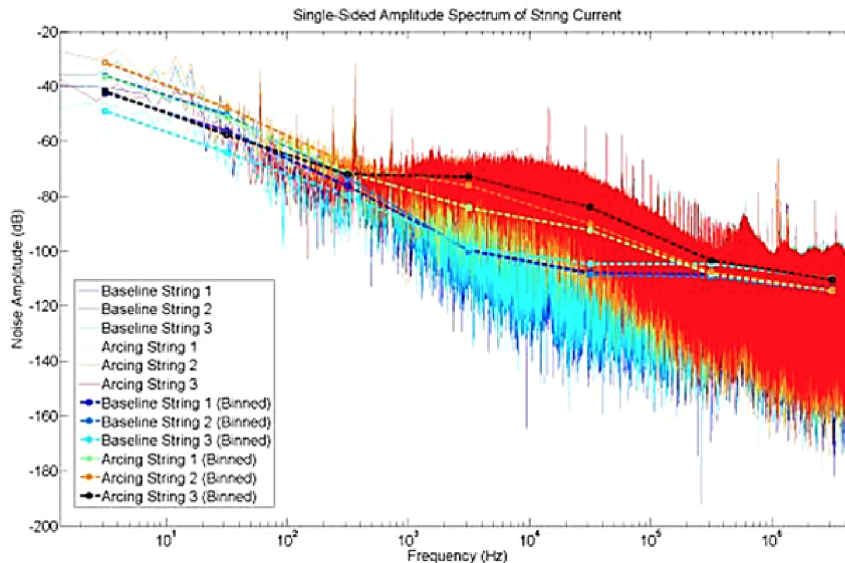


Figure 2.16. Noise recordings with AF scenario and baseline system in DETL.

The time window length (T_{ws}) selected could influence the I_{dif} waveform pattern. In Fig. 2.17 is shown the I_{dif} waveform obtained with different time window T_{sw} lengths: 1, 5, 25,

and 125 ms. These currents variance waveforms are calculated parting from the arc current trace shown in Fig. 2.18.

It can be seen that with $T_{sw} = 5$ ms and $T_{sw} = 25$ ms, there is a significant difference between no-arcing stage and stable arcing stage. With $T_{sw} = 1$ ms, the difference between arcing and no-arcing condition is relatively subtle which shows that 1 ms is too short to include enough current randomness in one single-time window. It can also be seen that with $T_{sw} = 125$ ms, the difference between arcing and no-arcing is still noticeable but is not improved compared with $T_{sw} = 5$ ms and $T_{sw} = 25$ ms.

Therefore, a T_{sw} value between 5 and 25 ms is considered appropriate because it is long enough to represent current randomness appropriately with the detection time guaranteed. T_{sw} starts from 1 ms which involves 200 data points, and is increased by the factor of 5 each

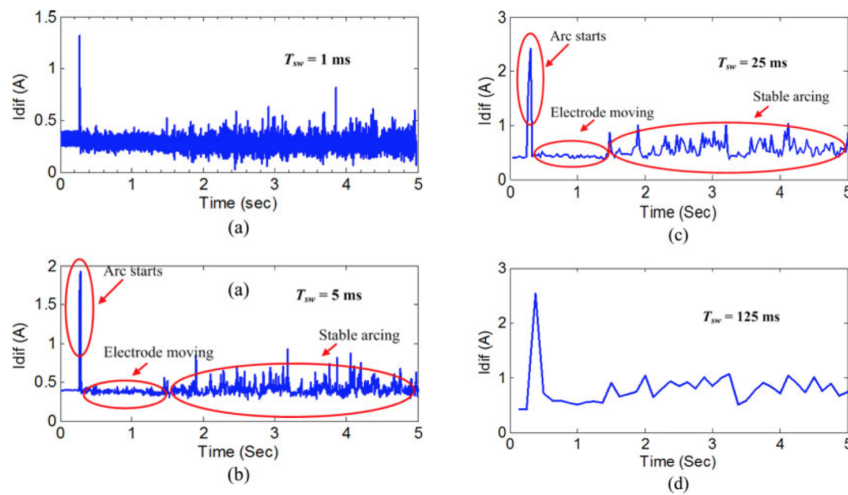


Figure 2.17. *Idif* waveform from different time window length (a) $T_{sw} = 1$ ms. (b) $T_{sw} = 5$ ms. (c) $T_{sw} = 25$ ms. (d) $T_{sw} = 125$ ms.

time until the time window is too long for a fast detection. In this way, a range within which the *Idif* value shows a significant change after arc happens can be obtained. Different T_{sw} values among the range that has been used throughout the work of Xiu Yao are, $T_{sw} = 10$ ms is used and $T_{sw} = 25$ ms to feed the detection algorithm. It is important to note that the choice of proper T_{sw} is unique as long as it is in the proper range. Frequency characteristics of the current before and during arcing are studied in this work through discrete wavelet

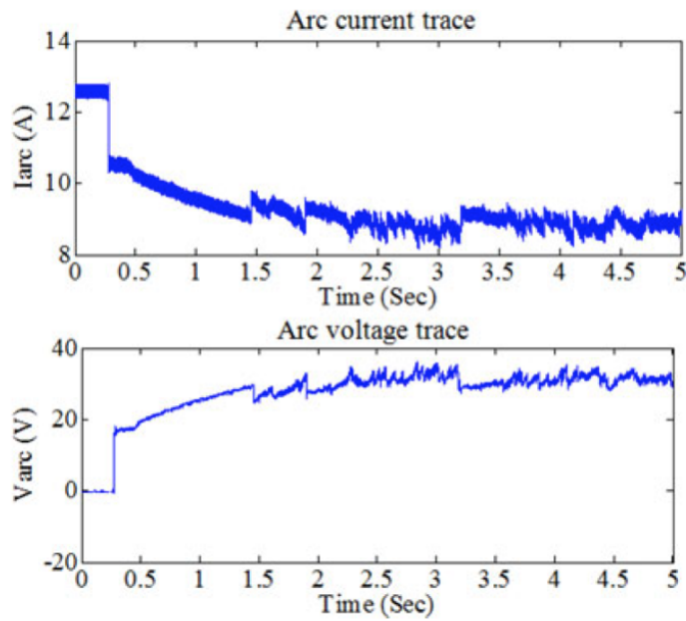


Figure 2.18. Baseline AF signature to perform calculations.

transform. This transformation is a multi-resolution analysis which states that any signal in the space of square integral functions, can be written as a linear combination of a countable orthonormal basis, known as the "mother wavelet".

All the DC fault detection techniques presented in this chapter are exclusively focus in the study of signals coming from the DC side. Nonetheless the proposal of this thesis project will analyze the response of the PV inverter under DC arc fault hoping to find a innovative approach for fault detection.

Chapter 3

Inverter Proposal for PV Applications

3.1 Main Structure of the Proposed Inverter Topology

As presented in chapter 1 and 2, recent developments in power converters aim for better performance and efficiency by employing the least number of components as possible. This idea is retained in order to correctly select each of the conversion stages of the proposed inverter and also to incorporate the features needed to be integrated into the modern grid. It's judged that the inverter should have a voltage conditioning feature, which implies a DC/DC conversion stage. After regulating the input DC voltage at the desired level a DC/AC stage will perform the transformation to AC. The topologies selected to achieve these tasks and the justification behind its choice is described in the following sections of this chapter. In Fig. 3.1 and 3.2 the schematic diagram of the two variants (Buck and Boost) of the proposed inverter is presented. The description of both inverters is also explained in the following sections.

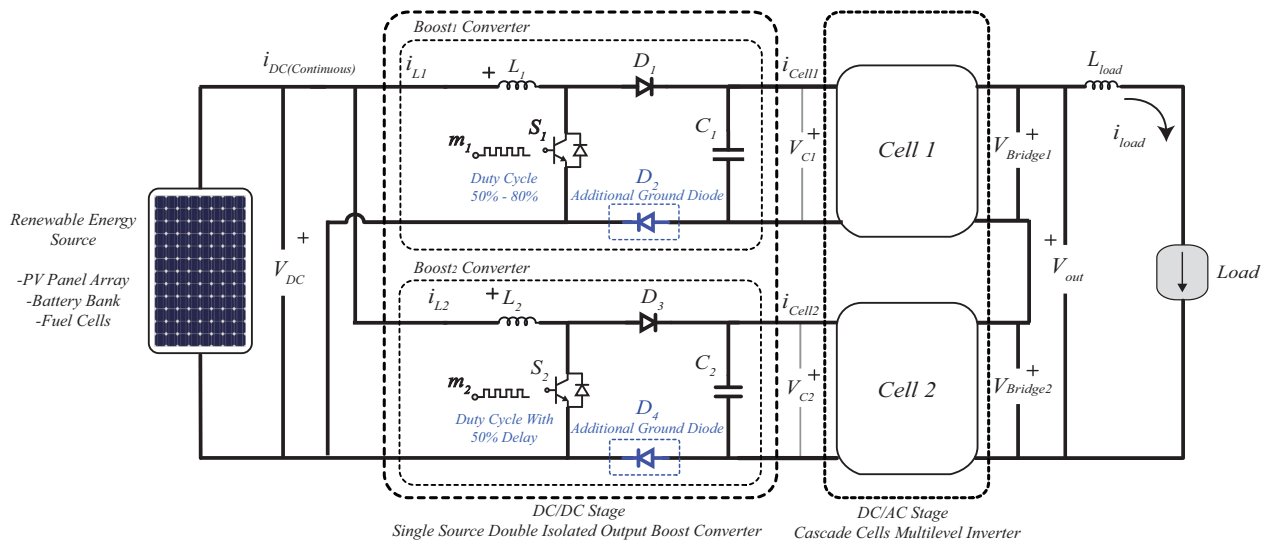


Figure 3.1. Inverter proposed system schematic diagram, Boost variant.

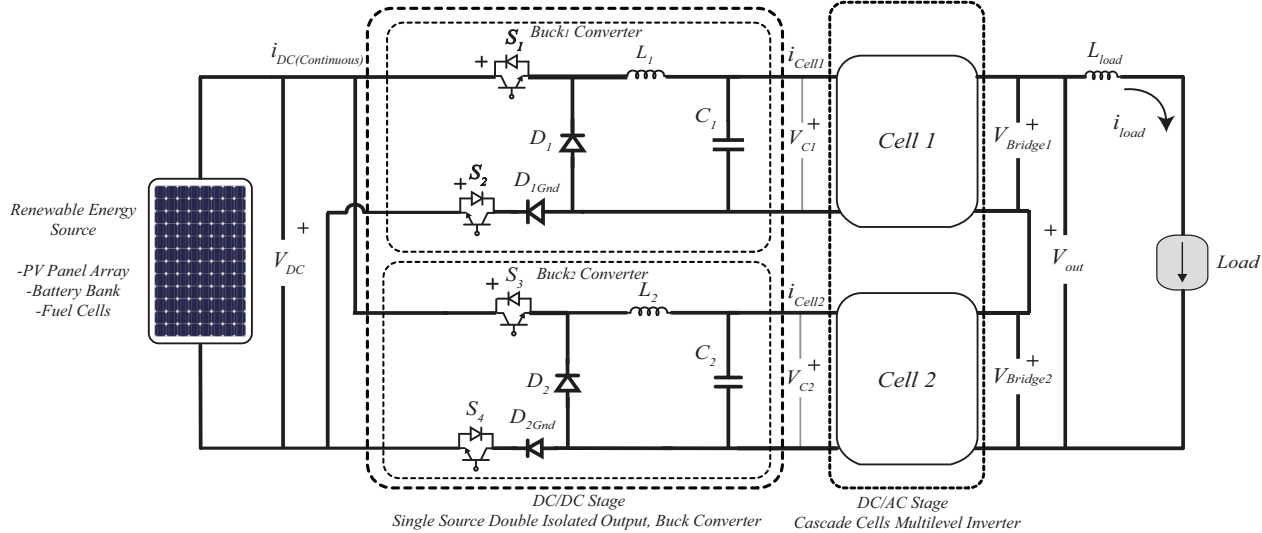


Figure 3.2. Inverter proposed system schematic diagram, Buck variant.

3.2 Development of the DC/DC Stage

The DC/DC stage proposal has the capacity of voltage regulation to no more than 400V for security reasons. Considering that the output voltage of the whole system needs to be suited for interconnection with the grid in the range between 150V-250V AC (50 and 60 Hz grids) in order to ensure a proper transfer of energy. The task of reducing voltage can be achieved with a buck converter topology. However, the DC/AC inverter stage of this proposal needs two isolated DC inputs, one for each cascaded cell (Full H bridge) in order to properly

generate the multilevel output. The use of additional DC sources is considered a disadvantage because it leads to employ additional components such as, voltage and current sensors for monitoring, additional PWM control, etc. All together decreasing the reliability, increases complexity and cost of the converter. A commonly employed solution to this issue is replacing DC sources with pre-charged capacitors, nevertheless, this replacement generates unbalance voltages between DC levels which will increase the output harmonic distortion. In order to achieve a transformerless inverter topology that will integrate the advantages of solid state electronics into the inverter, the development of a novel modified DC/DC converter capable of producing two controlled and isolated DC voltages from a single DC voltage source was needed. This novel architecture of converter was developed in two variants each described in the next two sections.

3.2.1 Isolated Double Boost Converter for DC/DC Stage

In this section and the next, the theoretical functioning for both buck and boost variants of the proposed DC/DC converter are described with detail.

Operational Principle of Double Boost Converter

In the schematic of Fig. 3.1, $boost_1$ and $boost_2$ converters have two possible functioning states, one when switch S_1 is in *conduction (on)* ($S_1 = 1$) state and second state when is *open (off)* ($S_1 = 0$). Due to this, four topological states can be generated when connected in parallel, as showed in Table 3.2.1. These converters extract power from the sources in alternate times, which is achieved with a phase delay of 50% between control signals m_1 and m_2 as illustrated in Fig. 3.3. In order to operate this proposed topology, switching state where $S_1 = 0$ and $S_2 = 0$ has to be avoided, in order to conserve ground isolation between $boost_1$ and $boost_2$.

TABLE 3.2.1. Boost Variant Switching States.

States	S_1	S_2	iL_1	iL_2	i_{D_1}	i_{D_2}	i_{D_3}	i_{D_4}
1	0	0	$\frac{(V_{DC}-V_{C_1})(1-Duty_1)T}{L_1}$	$\frac{(V_{DC}-V_{C_2})(1-Duty_2)T}{L_2}$	on	on	on	on
2	0	1	$\frac{(V_{DC}-V_{C_1})(1-Duty_1)T}{L_1}$	$\frac{(V_{DC}Duty_2)T}{L_2}$	on	on	off	off
3	1	0	$\frac{(V_{DC}Duty_1)T}{L_1}$	$\frac{(V_{DC}-V_{C_2})(1-Duty_2)T}{L_2}$	off	off	on	on
4	1	1	$\frac{(V_{DC}Duty_1)T}{L_1}$	$\frac{(V_{DC}Duty_2)T}{L_2}$	off	off	off	off

One advantage of the boost variant over the buck variant [3] is the possibility to work with a duty cycle higher than 50%. This feature allow the converter to achieve a maximum elevation ratio of 1:10 times the input V_{DC} , when both duty cycle m_1 and m_2 are set to 80%. This achievement represents one of the main contributions of this topology, compared to conventional boost converter elevation capacities of only three times input V_{DC} .

The PWM control signals and variables involved in this converter are presented in Fig. 3.3 (a)-(g). The $Carry_1$ and $Carry_2$ are sawtooth signals which are compared to a DC signal in order to achieve the desired duty cycles. For m_1 and m_2 , the output voltages of $boost_1$ and $boost_2$ V_{C_1} and V_{C_2} are controlled. The generation of m_1 and m_2 is based on equations (3.1) and (3.2). These pulses are applicable to switches S_1 and S_2 . As showed in Fig. 3.3(a) and (c), $Carry_1$ and $Carry_2$ are out of phase in order to obtain the alternated behavior of this proposal which is described in the next section. The currents in the inductors iL_1 and iL_2 are shown in Fig. 3.3 e) and f) respectively. As shown, these boost converters are working in a continuous conduction mode. Equation (3.3) shows the possible combinations between S_1 and S_2 .

$$m_1 = \begin{cases} 1 & \text{when } Duty_1 > Carry_1 \\ 0 & \text{when } Duty_1 < Carry_1 \end{cases} \quad (3.1)$$

$$m_2 = \begin{cases} 1 & \text{when } Duty_2 > Carry_2 \\ 0 & \text{when } Duty_2 < Carry_2 \end{cases} \quad (3.2)$$

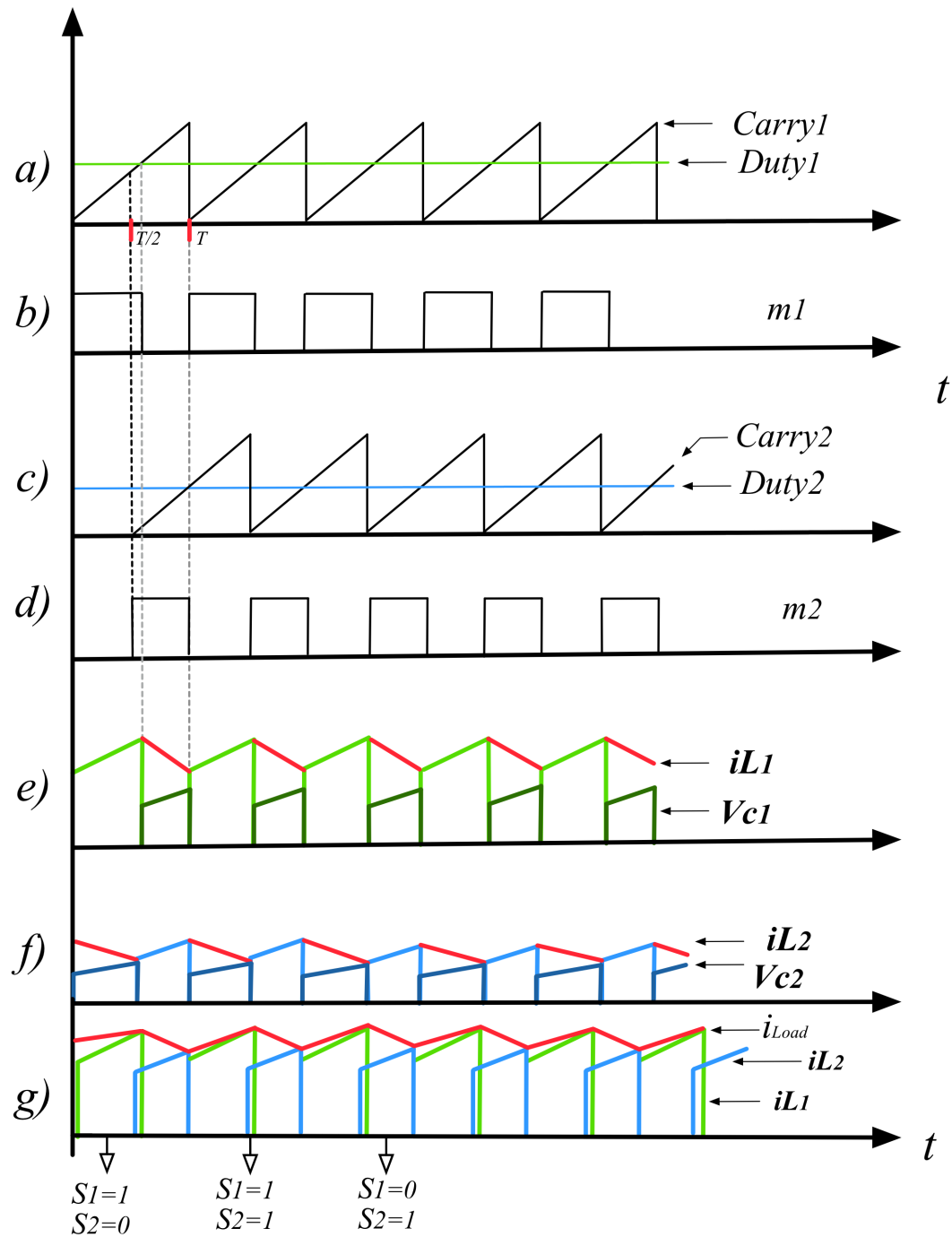


Figure 3.3. Control strategy for boost variant converter; a) $Carry_1$ and $Duty_1$, b) Pulse m_1 c) $Carry_2$ and $Duty_2$, d) Pulse m_2 , e) i_{L1} and V_{C1} , f) i_{L2} and V_{C2} g) i_{Load} .

$$\begin{aligned}
S_1 = 0 \quad S_2 = 0 & \text{ Prohibited State} \\
S_1 = 1 \quad S_2 = 0 \\
S_1 = 0 \quad S_2 = 1 \\
S_1 = 1 \quad S_2 = 1
\end{aligned} \tag{3.3}$$

Considering the eqs. (3.1)-(3.3), when the S_1 is in logical state 1, the current through the inductor L_1 results in an energy storage expressed as:

$$\Delta i_{L_{1on}} = \frac{1}{L_1} \int_0^{Duty_1 T} V_{DC} dt = \frac{Duty_1 T}{L_1} V_{DC} \tag{3.4}$$

When S_1 is in logical state 0, the current through the inductor L_1 is expressed as,

$$\Delta i_{L_{1off}} = \int_{Duty_1 T}^T \frac{(V_{DC} - V_{C_1}) dt}{L_1} \tag{3.5}$$

$$\Delta i_{L_{1off}} = \frac{(V_{DC} - V_{C_1})(1 - Duty_1)T}{L_1} \tag{3.6}$$

In Table 3.2.1 the conduction state of the diodes in each switching combination is presented.

The output voltage for the converter can be expressed as:

$$V_{C_1} = \frac{V_{DC}}{1 - Duty_1} \tag{3.7}$$

Although in any moment that the switch S_1 or S_2 holds a logical state 0, the complementary boost output voltage will depend for a short period on the capacitor resulting in the circuit of Fig. 3.4.

Where $Cell_1$ acts as a drain current for C_1 , as a consequence, the output voltage during that time will fall. The capacitor C_1 must be able to maintain the voltage for a long period of time when the load is light, otherwise, in order to maintain the voltage, the value of the capacitor has to be wisely selected.

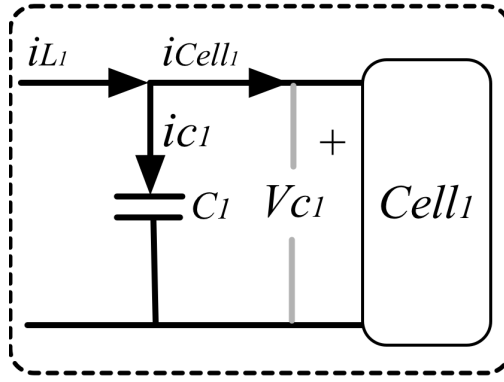


Figure 3.4. Discharging circuit during state 0.

The capacitor voltage is related to currents i_{C_1} and i_{Cell_1} , both are needed to determine the boost converter output V_{C_1} supplied to $Cell_1$. The i_{C_1} current for the capacitor is given by:

$$i_{c_1}(t) = C_1 \frac{dV_{C_1}(t)}{dt} \quad (3.8)$$

The capacitor voltage V_{C_1}

$$V_{C_1}(t) = \frac{1}{C_1} \int i_{c_1}(t) dt + V_{C_1}^0 \quad (3.9)$$

$$V_{C_1}(t) = \frac{1}{C_1} \int (i_{L_1}(t) - i_{Cell_1}(t)) dt + V_{C_1}^0 \quad (3.10)$$

When S_1 change from logical 0 to 1, the current $i_{DC_1}(t)$ becomes zero. Thus, the capacitor voltage during this disconnection time is,

$$V_{C_1}(t) = -\frac{1}{C_1} \int i_{Cell_1}(t) dt + V_{C_1}^0 \quad (3.11)$$

The equations described in this section serve as a mathematical fundament for the first boost converter and the same equations can be applied to describe the behavior of the second boost converter by expressing the equations in terms of $boost_2$. In order to obtain

the components values, since the alternating behavior of this proposal bases its functioning in a power extraction from the DC source at alternated stages, this behavior doesn't have a repercussion in the interaction between both converters, hence the conventional equations to determine the values of components can be employed.

Double Boost Proposal Switching States

To illustrate the proposed system operation. In Fig. 3.5 are highlighted the current paths corresponding to state 3 of Table 3.2.1. In $boost_1$, D_1 and D_2 are not polarized, so the current flows only through the inductor L_1 , meanwhile, the capacitor C_1 is maintaining output V_{C_1} for $Cell_1$. Also $boost_2$ transfers energy saved in the precedent cycle in L_2 to

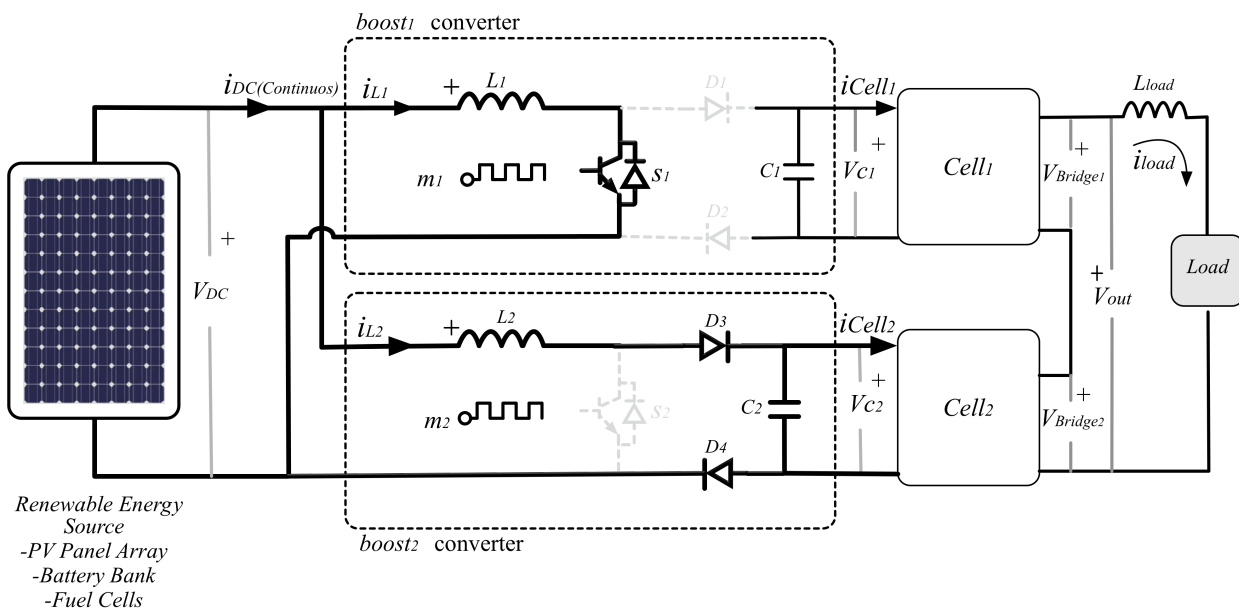


Figure 3.5. Proposed topology in switching state 3 where $S_1=1$, $S_2=0$ with highlighted currents paths.

charge C_2 and supply V_{C_2} for $Cell_2$. When switching state change from state 3 to state 2, the operation of the topology is inverted. The current i_{L_1} from $boost_1$ flows directly to charge C_1 and supply the V_{C_1} to $Cell_1$, meanwhile diodes D_3 and D_4 are not polarized, and inductor L_2 accumulate energy. So V_{C_2} for $Cell_2$ is maintained with C_2 , as presented in Fig. 3.6.

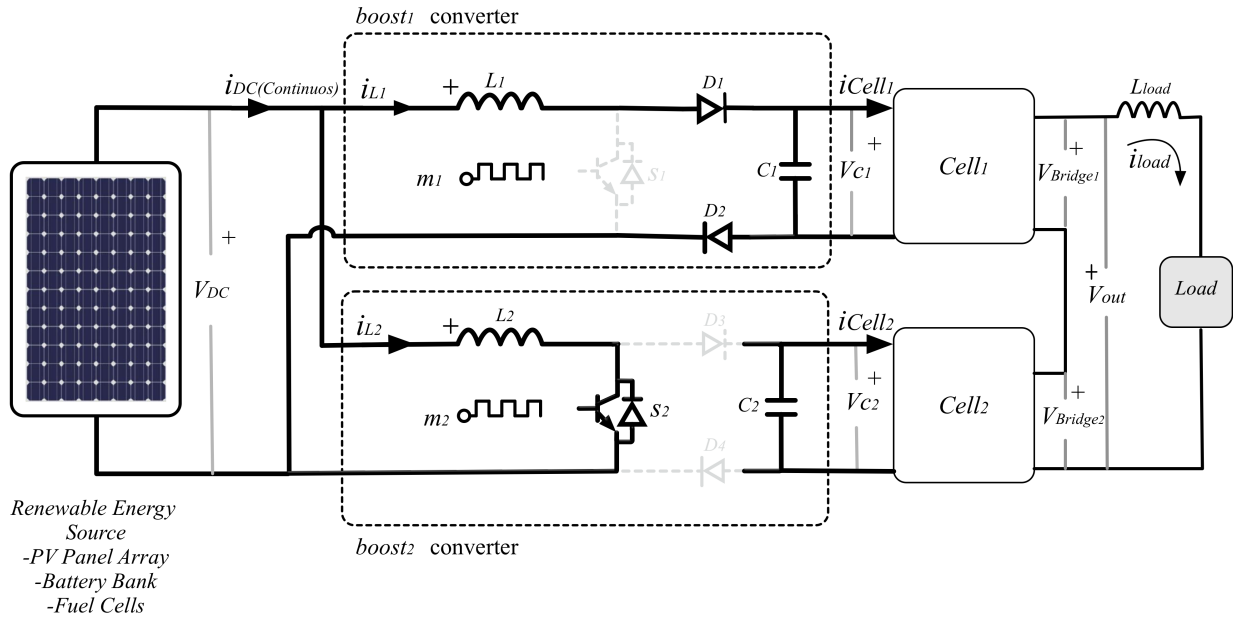


Figure 3.6. Proposed topology in switching state 2 where $S_1=0$, $S_2=1$ with highlighted currents paths.

Now the state 4 is presented in Fig. 3.7, during this state $S_1=1$ and $S_2=1$. Both S_1 and S_2 are in conduction, and diodes D_1 , D_2 , D_3 and D_4 are not polarized. As a result, V_{DC} transfers the maximum current to the inductors L_1 and L_2 , generating energy storage for posterior use, and capacitors C_1 and C_2 maintain V_{C1} and V_{C2} for both $Cell_1$ and $Cell_2$.

An important contribution of this proposed topology is that both converters are able to work beyond 50% of the duty cycle, unlike topologies in [3]. Consequently, a high elevation factor of 1:5 is used in this thesis but a maximum elevation can be attained to reach a ratio of 1:10 by setting $m_1=80\%$ and $m_2=80\%$.

3.2.2 Isolated Double Buck Converter for DC/DC Stage

Operational Principle of Double Buck Converter

In the proposed topology of Fig. 3.2, $buck_1$ and $buck_2$ converters have two possible functioning states each, one when switch S_1 and S_2 (S_3 and S_4 for buck 2) are in conduction state

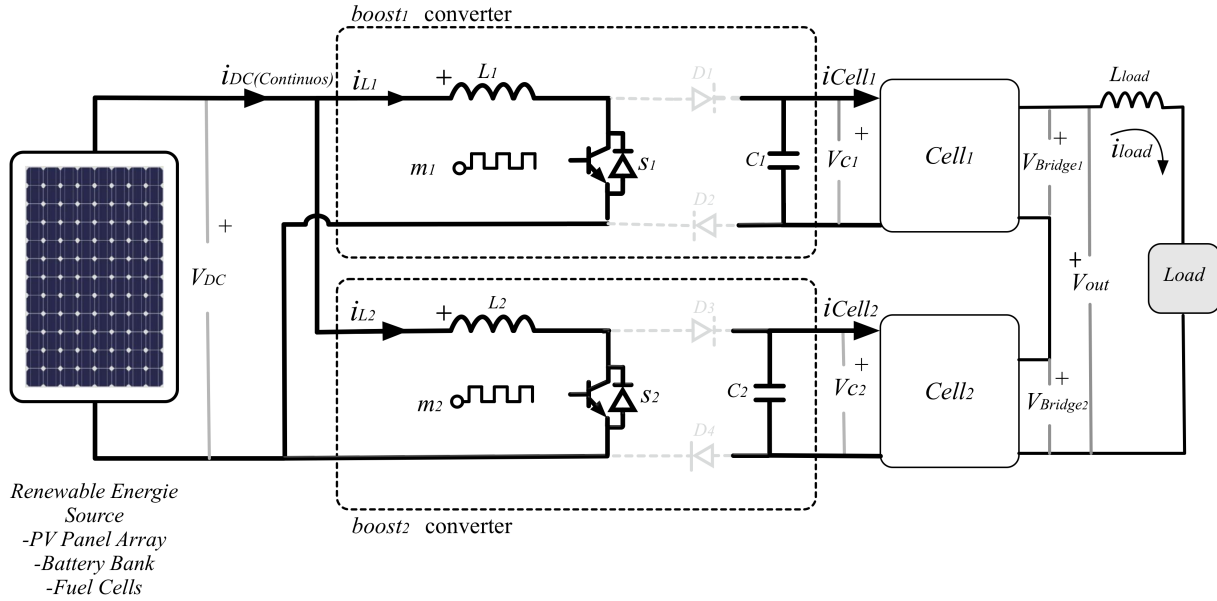


Figure 3.7. Proposed topology in switching state $S_1=1$, $S_2=1$ with highlighted currents paths.

(on) ($S_1 = 1$ $S_2 = 1$) and a second state when is open (off) ($S_1 = 0$ $S_2 = 0$). The four possible topological combinations that can be achieved for this configuration of parallel connected converters, is shown in Table 3.2.2. These converters extract power from the sources in alternate time, and this is achieved thanks to a phase delay of 50% between control signals m_1 and m_2 as described in equation (3.12) and (3.13). The state $S_1 = 1$ $S_2 = 1$ and $S_3 = 1$ $S_4 = 1$ where both converters will be (on) at the same time has to be avoided to conserve the isolation between $buck_1$ and $buck_2$. This is one limitation of this parallel buck topology, since the maximum duty cycle is of only 50%.

The state 3 of Table 3.2.2 where $S_1 = 1$ and $S_2 = 1$ is presented in Fig. 3.8, considering that current i_{DC1} flows from the power supply V_{DC} , from collector-emitter of switch S_1 , followed by the inductor L_1 to the capacitor C_1 , closing the circuit to ground by D_{1GND} and the extra switch S_2 . It is noted that for this current mesh, the diode D_1 is not polarized. Parallel to this process the $buck_2$ converter is in state i_{L2off} , this current is only dependent of voltage V_{C1} , described in equation (3.15) and when the S_1 is in logical state 1, the current through the inductor L_1 results in an energy storage expressed in equation (3.14).

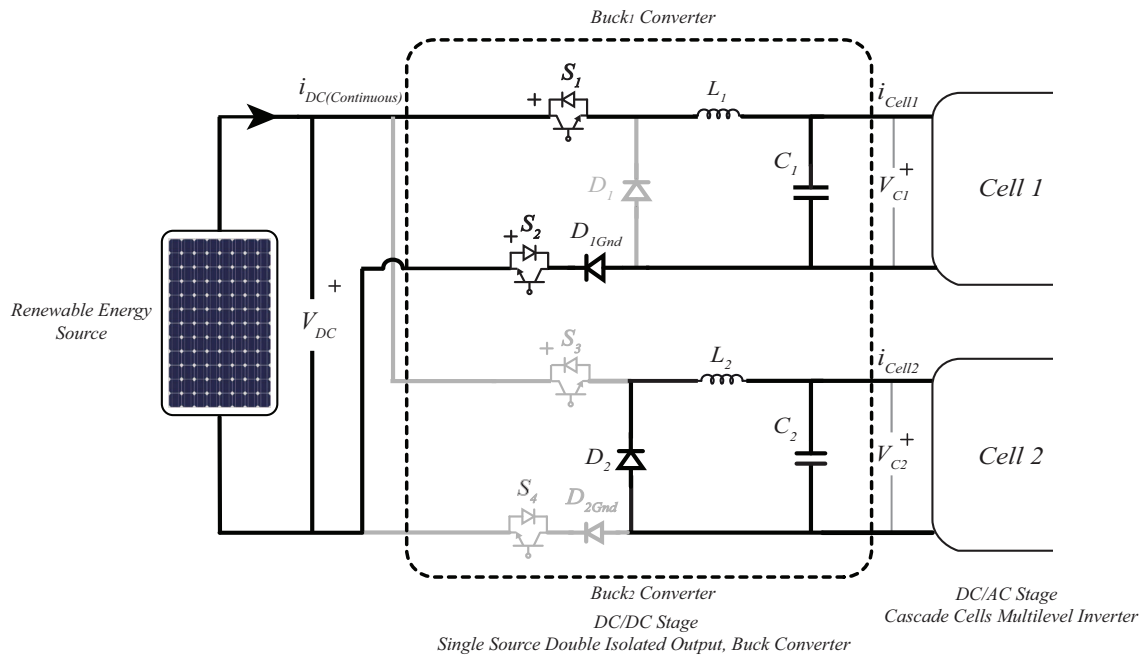


Figure 3.8. Proposed topology buck variant in switching state $S_1=1, S_2=0$ with highlighted currents paths.

TABLE 3.2.2. Buck Variant Switching States.

States	S_1	S_2	i_{L_1}	i_{L_2}	i_{D_1}	i_{D_2}
1	0	0	$\frac{V_{C_1} t_{1off}}{L_1 T}$	$\frac{V_{C_2} t_{2off}}{L_2 T}$	on	on
2	0	1	$\frac{V_{C_1} t_{1off}}{L_1 T}$	$\frac{(V_{DC}-V_{C_2}) t_{2on}}{L_2 T}$	on	on
3	1	0	$\frac{(V_{DC}-V_{C_1}) t_{1on}}{L_1 T}$	$\frac{V_{C_2} t_{2off}}{L_2 T}$	off	off
4	1	1	Prohibited	Prohibited	off	off

Considering that:

$$m_1 = \begin{cases} 1 & \text{when } Duty_1 > Carry_1 \\ 0 & \text{when } Duty_1 < Carry_1 \end{cases} \quad (3.12)$$

$$m_2 = \begin{cases} 1 & \text{when } Duty_2 > Carry_2 \\ 0 & \text{when } Duty_2 < Carry_2 \end{cases} \quad (3.13)$$

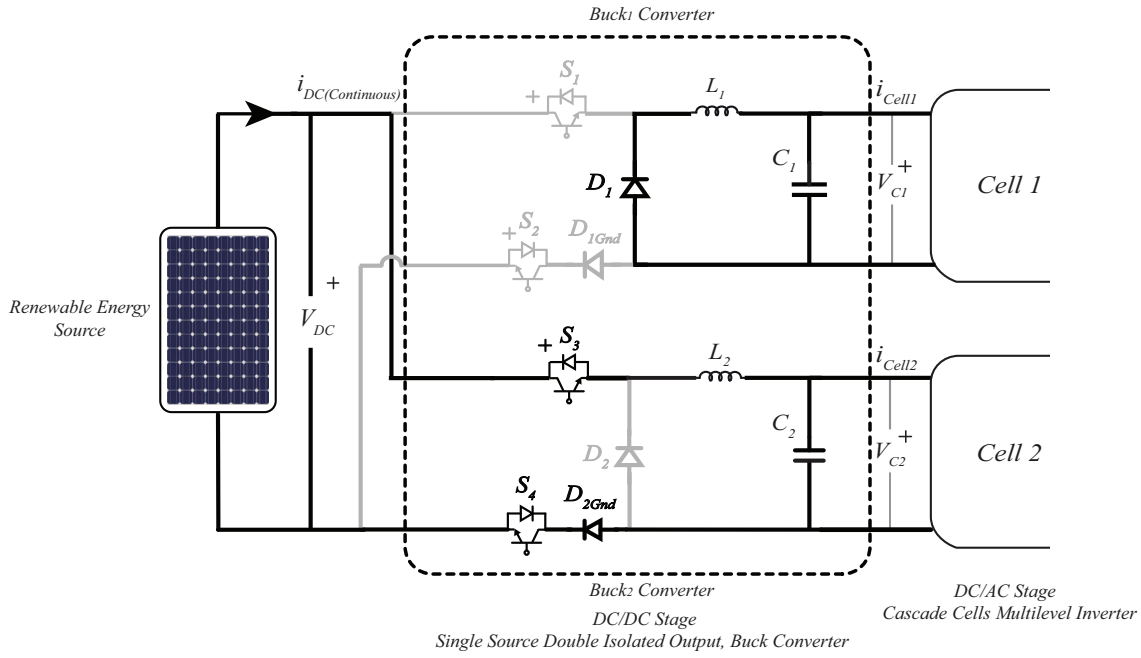


Figure 3.9. Proposed topology buck variant in switching state $S_1=0$, $S_2=1$ with highlighted currents paths.

$$\Delta i_{L_{1on}} = \frac{1}{T} \int_0^{Duty_1 T} \frac{(V_{DC} - V_{C1})}{L_1} dt = \frac{(V_{DC} - V_{C1})}{L_1} \frac{t_{1on}}{T} \quad (3.14)$$

When S_1 is in logical state 0, the current through the inductor L_1 is expressed as,

$$\Delta i_{L_{1off}} = \frac{1}{T} \int_{Duty_1 T}^T \frac{-V_{C1}}{L_1} dt = \frac{-V_{C1}}{L_1} \frac{t_{1off}}{T} \quad (3.15)$$

The state 2 of Table 3.2.2 where $S_1 = 0$ and $S_2 = 1$ is presented in Fig. 3.9, considering that current i_{DC_2} flows from the power supply V_{DC} , from collector-emitter of switch S_3 , followed by the inductor L_2 to the capacitor C_2 , closing the circuit to ground by D_{2GND} and the extra switch S_4 . It is noted that for this current mesh, the diode D_2 is not polarized. Parallel to this process the *buck*₁ converter is in state $i_{L_{1off}}$, this current is only dependent of voltage V_{C_2} .

In Table 3.2.2 the conduction state of the diodes in each switching combination is also presented. Although in any moment that the switch $buck_1$ or $buck_2$ holds a logical state 0, the complementary buck output voltage will depend for a short period on the capacitor resulting in the circuit of Fig. 3.4. This novel DC/DC topology with the two variants boost and buck, is ideal to be used with multilevel DC/AC inverters as an elevation stage capable of generate two isolated DC outputs from a single source, capable of elevating up to ten times the input with no extreme duty cycles and performing it with fewer components compared to similar capacities topologies.

3.3 Multilevel DC/AC Stage

As mentioned multilevel inverters are the tendency in the development of power electronics, and cascade cells topology contributes with the best features without compromising number of components and performance in the DC/AC conversion, in this selection the DC/AC stage of the PV inverter is presented.

3.3.1 DC/AC Proposal Operational Principle

The DC voltage, produced by the PV panel is conditioned with the modified double buck topology presented in this research, afterwards both DC levels are used to feed an asymmetrical cascade cell multilevel topology in order to perform the conversion into AC. This inverter incorporates the advantage of being transformerless, and use only eight IGBT's to achieve DC/AC conversion. Accomplishing a high power density, low harmonic distortion and nine-level output waveform as showed in Fig 3.10. The generation of a nine-level output voltage V_{out} results from the combination of possible states between $Cell_1$ and $Cell_2$. Both cells can adopt three states $+V_{C_1}$, 0 , $-V_{C_1}$ for $Cell_1$ and $+V_{C_2}$, 0 , $-V_{C_2}$ for $Cell_2$. Taking into account the asymmetrical values of V_{C_1} and V_{C_2} nine combinations between the two cells are possible, which are presented in Table 3.3.1, also the required logic value for switches in $Cell_1$ and $Cell_2$ are presented.

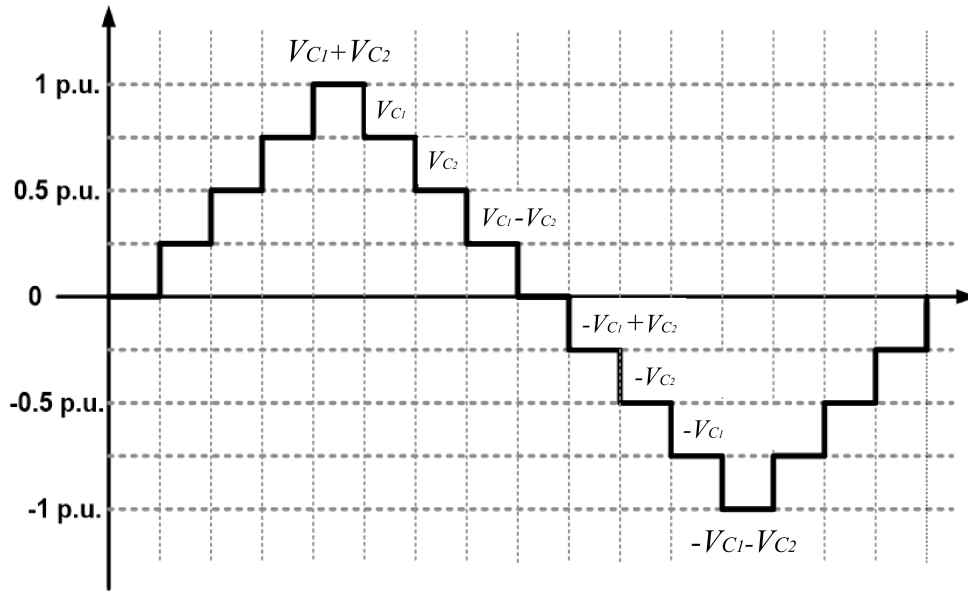


Figure 3.10. Multilevel V_{out} for cascaded converter.

The voltages V_{C_1} and V_{C_2} have to satisfy the asymmetrical ratio determined by:

$$V_{C_1} = \frac{3}{2}V_{C_2} \quad (3.16)$$

TABLE 3.3.1. Stepping Logic for a Nine-Level Converter.

$Cell_1$	$Cell_2$	Combinational
S_1, S_2, S_3, S_4	S_1, S_2, S_3, S_4	Levels
1,0,0,1	1,0,0,1	$V_{C_1} + V_{C_2}$
1,0,0,1	0,1,0,1	V_{C_1}
0,1,0,1	1,0,0,1	V_{C_2}
1,0,0,1	0,1,0,1	$V_{C_1} - V_{C_2}$
0,1,0,1	0,1,0,1	0
0,1,0,1	1,0,0,1	$-V_{C_1} + V_{C_2}$
0,1,0,1	0,1,0,1	$-V_{C_2}$
0,1,0,1	0,1,0,1	$-V_{C_1}$
0,1,0,1	0,1,0,1	$-V_{C_1} - V_{C_2}$

3.3.2 Nine-Level SPWM Modulation

The employed multilevel modulation technique in this paper uses eight modulating waves carriers. These signals can be constant voltage levels to generate a multiple pulse width modulation (MPWM), triangular, sawtooth or sinusoidal waveforms to generate a sinusoidal pulse width modulation (SPWM). This process is illustrated in Fig. 3.11.

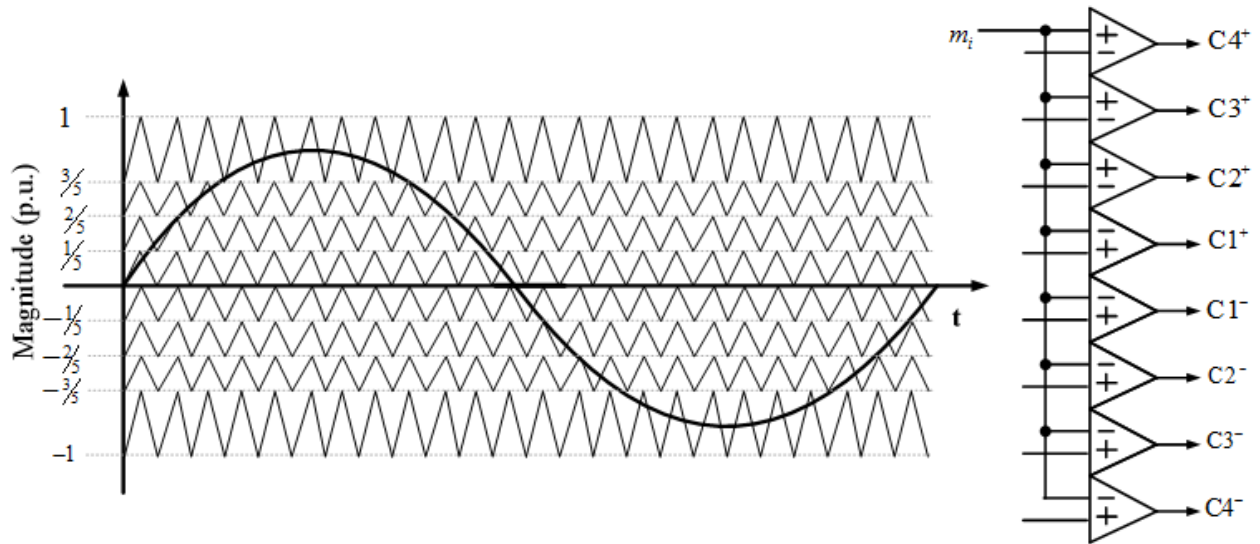


Figure 3.11. Nine-level SPWM technique.

The comparisons of the carriers against the sinusoidal 60 Hz fundamental signal will create a pulse that will be employed later to generate the eight signals that will command the IGBT's of this inverter. The schematic circuit for the cascade cells and the boolean logic to obtain each IGBT signal is presented in Fig. 3.12a and Fig. 3.12b.

$$c_i^+ = \begin{cases} 1 & \text{when } carry_i^+ < m_i \\ 0 & \text{when } carry_i^+ > m_i \end{cases} \quad (3.17)$$

$$c_i^- = \begin{cases} 1 & \text{when } carry_i^- > m_i \\ 0 & \text{when } carry_i^- < m_i \end{cases} \quad (3.18)$$

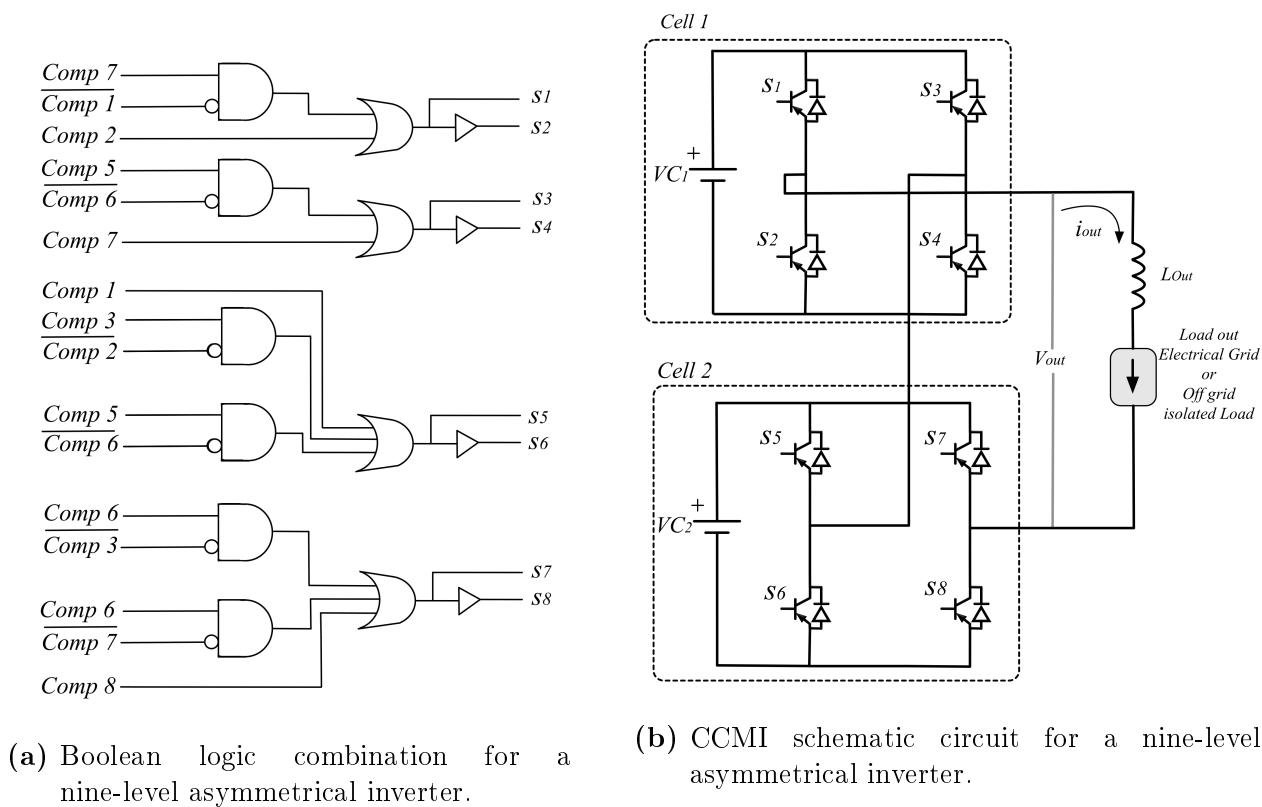


Figure 3.12. Cascade cells multilevel inverter topology and control.

Each pulse that drives an IGBT ($S_1 - S_8$) has its own characteristic waveform that will result from a combination of the boolean logic using as source the comparisons signals ($Comp1 - Comp8$) at different levels of the AC fundamental as presented in Fig 3.11.

With the detailed description of modeling, control and functioning for both buck and boost DC/DC variants and also for the DC/AC chosen inverter topologies in the next chapter will be presented the simulation and experimental results of the proposed PV inverter.

Chapter 4

Inverter Simulation and Experimental Results

4.1 Introduction

In this chapter, the functioning of the proposed inverter is evaluated in both simulation and experimental test bench. The results are obtained using *Matlab Simulink* and the series of test performed are detailed in the following sections.

4.2 Simulation Results

In order to evaluate the response of the DC/DC buck and boost variants of the proposed inverter, both are connected to the asymmetrical CCMI, by this the quality of the output is studied. Considering that the voltage generated by each DC/DC stage posses a ripple instead of being constant, the impact of this in the nine-level AC output is evaluated.

4.2.1 Inverter Buck Variant

In order to perform the simulation of the inverter structure, the software *Matlab Simulink* is employed, all the parts that need to be included in this simulation are: the new developed of DC/DC stage, the asymmetrical cascade cell multilevel topology, and the respective control strategy for each stage, which was presented in Fig. 3.12a.

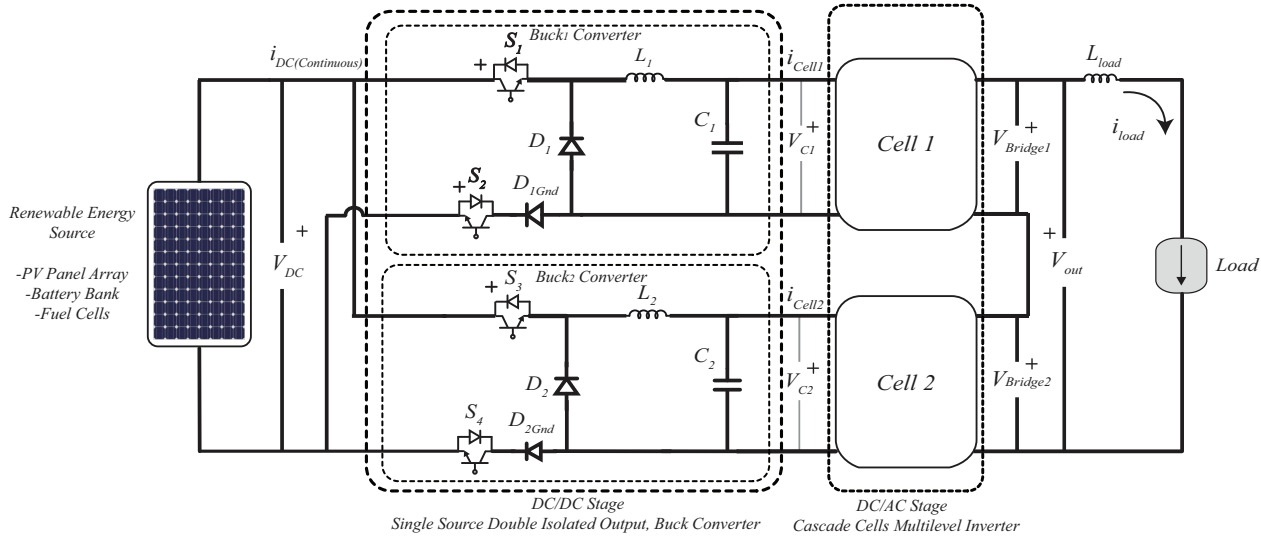


Figure 4.1. Schematic diagram of the smart inverter buck variant.

In order to perform the simulation, the schematic of Fig. 4.1 is employed, which include the CCMI DC/AC stage of Fig. 3.12b and the DC/DC buck stage. With all parts connected together in the simulation the resulting schematic is shown in Fig. 4.2. The resulting signals of the buck DC/DC stage are presented in Fig. 4.3, the waveforms presented are V_{C1} , iL_1 , V_{C2} and iL_2 . In this signals can be appreciated that the ripple voltage of both V_{C1} and V_{C2} is of 0.8 V which may seem elevated nonetheless it doesn't affect the integrity of the output generated by the DC/AC stage. The output waveforms of the DC/AC stage are shown in Fig. 4.4, were $V_{Bridge1}$, $V_{Bridge2}$, V_{out} and I_{out} waveforms is present. Thanks to these signals it can be concluded that both DC/DC and DC/AC stages of the proposed inverter, are functioning as expected.

In order to obtain these results the simulation values employed are enlisted in Table 4.2.1.

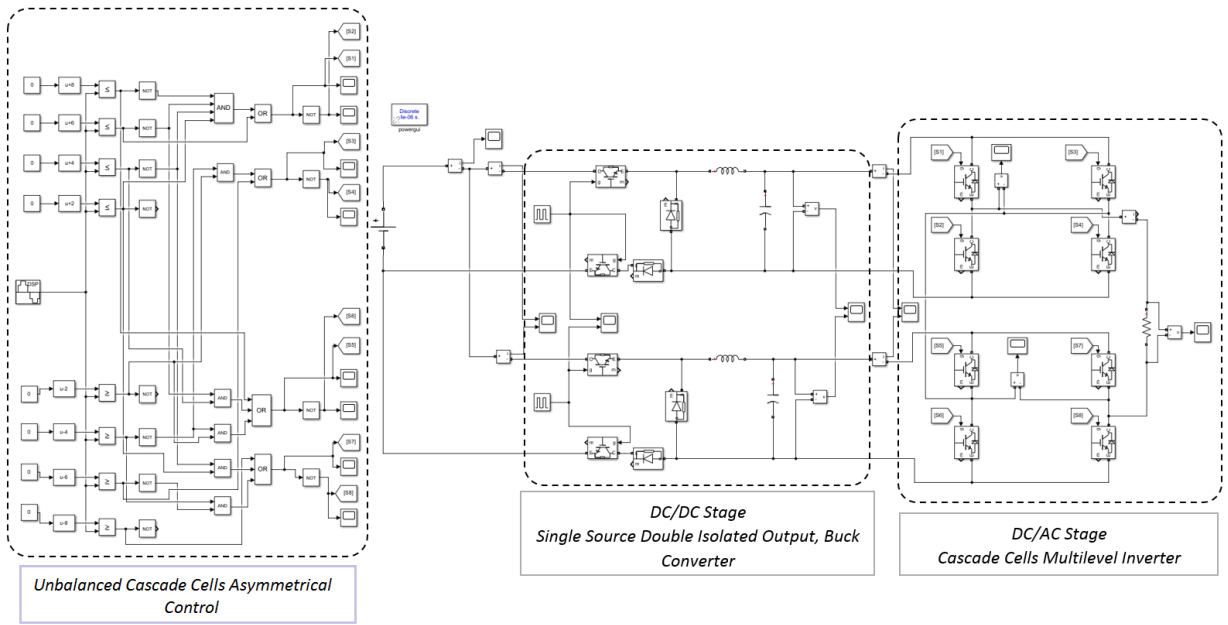


Figure 4.2. Simulink resulting schematic diagram of the Fig. 4.1.

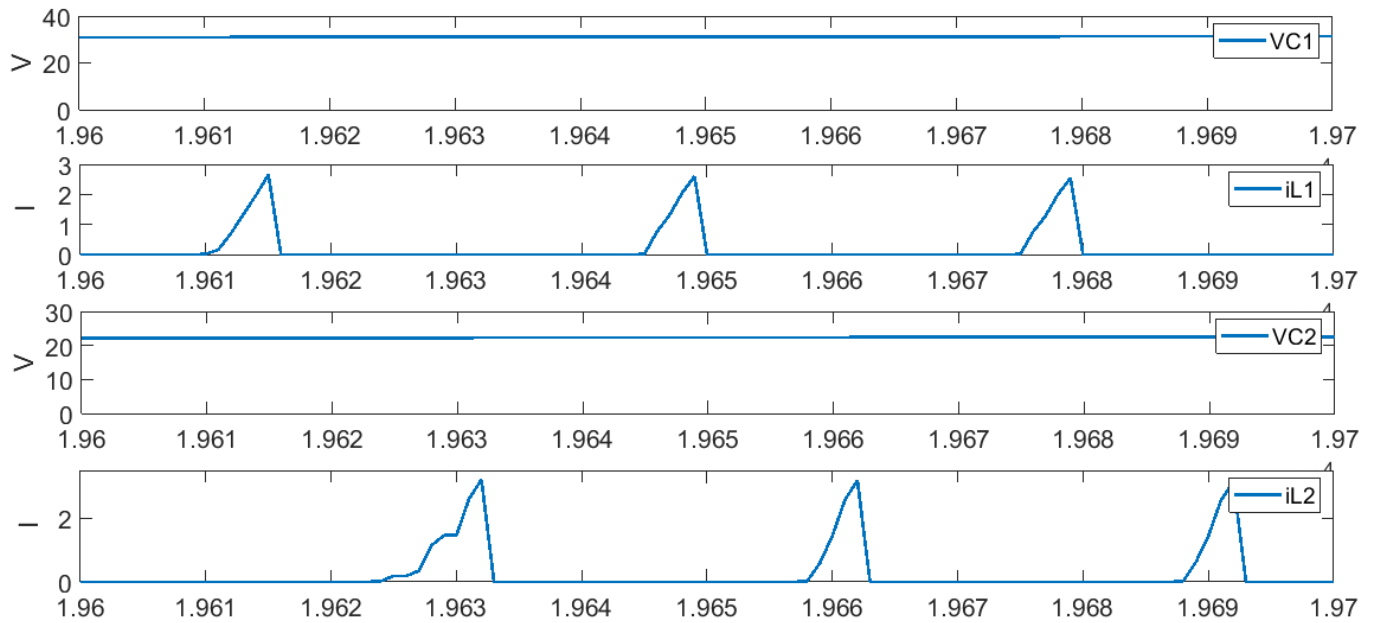


Figure 4.3. Stimulation results of the DC/DC stage a) V_{C1} b) i_{L1} c) V_{C2} d) i_{L2} .

To obtain these results was used for the buck variant of the inverter, although depending on the application, the DC/DC stage can be changed to its boost variant.

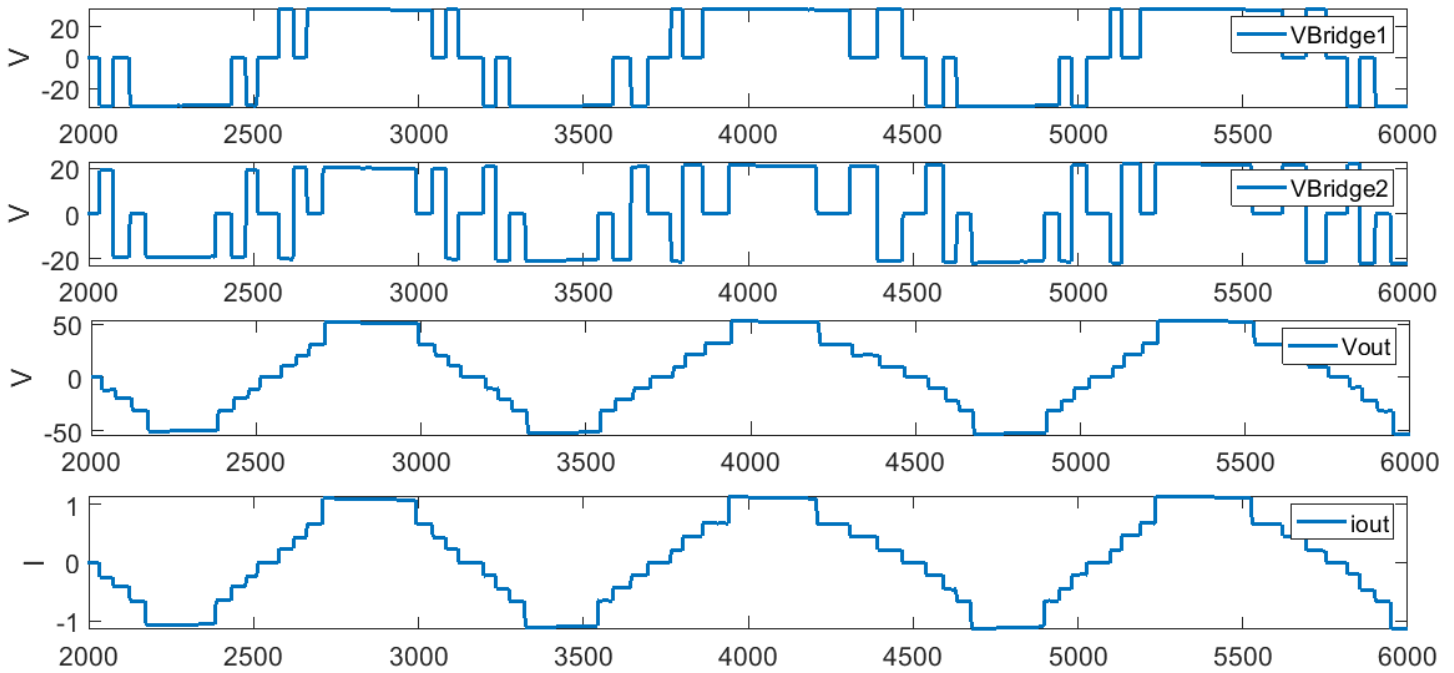


Figure 4.4. Stimulation results of the DC/AC stage a) $V_{Bridge1}$, b) $V_{Bridge2}$, c) V_{out} , d) I_{out} .

TABLE 4.2.1. Simulation Components Values.

<i>Components</i>	<i>Value</i>
<i>Frequency</i>	$2kHz$
<i>DutyCycle1</i>	45%
<i>DutyCycle2</i>	32%
L_1	$438\mu H$
L_2	$438\mu H$
C_1	$2200\mu F$
C_2	$2200\mu F$
<i>Load</i>	47Ω
V_{out}	$50V_p(100V_{pp})$

4.2.2 Inverter Boost Variant

In this section are to be submitted the simulation results obtained with the inverter, employing the DC/DC boost variant. To obtain these results the schematic of Fig. 4.5 is employed, by representing all components needed in *Matlab Simulink*, the resulting schematic diagram is shown in Fig. 4.6. With this configuration are obtained the results of

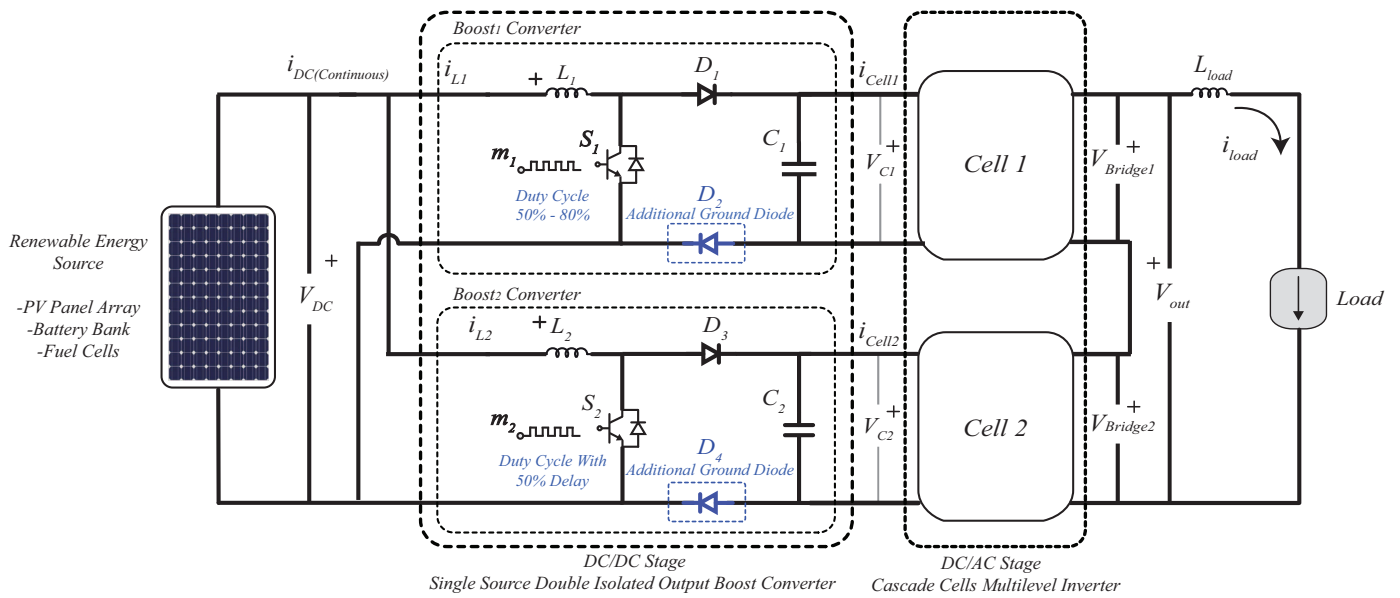


Figure 4.5. Schematic diagram of the inverter boost variant.

Fig. 4.7, in this graphic are presented the same signals as for the simulation of the buck variant, V_{C1} , i_{L1} , V_{C2} , i_{L2} , and i_{DC} , the only difference is that the voltage levels reached are higher, given the nature of this DC/DC stage. One of key advantages of using this variant, is a constant current supplied to the DC/AC stage, as can be appreciated in Fig. 4.7. Concerning V_{C1} and V_{C2} it can be seen that the voltage generated is constant, which help to keep the integrity of the multilevel output.

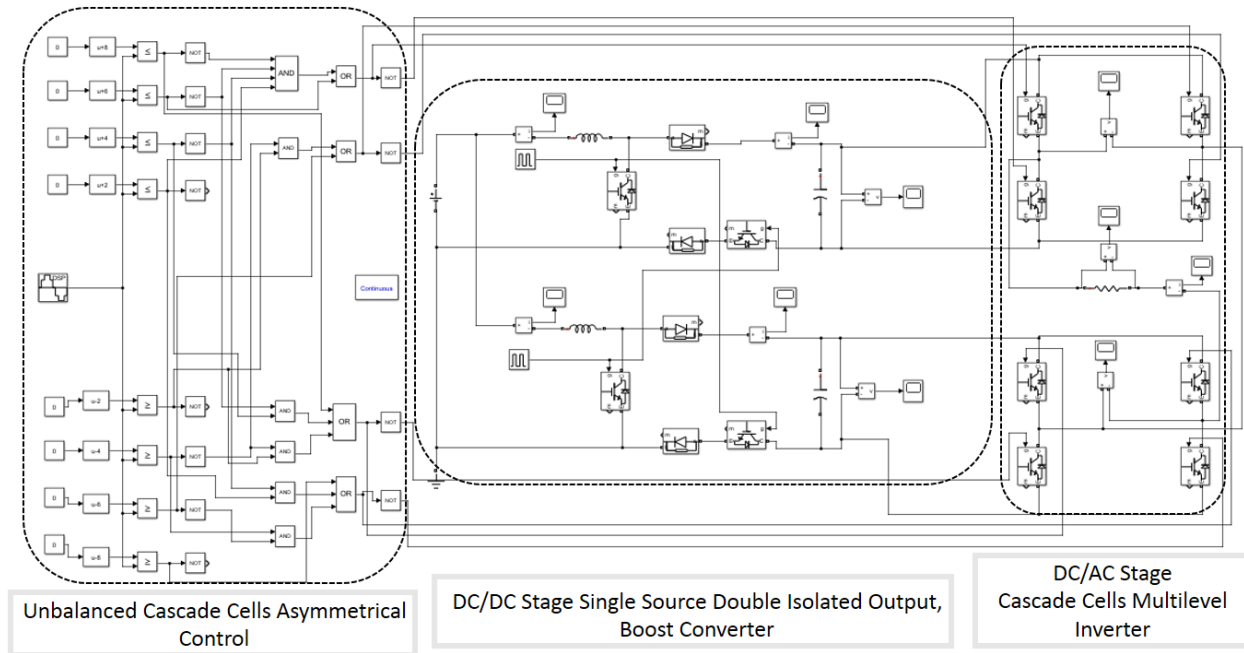


Figure 4.6. Simulink resulting schematic diagram of the Fig. 4.5.

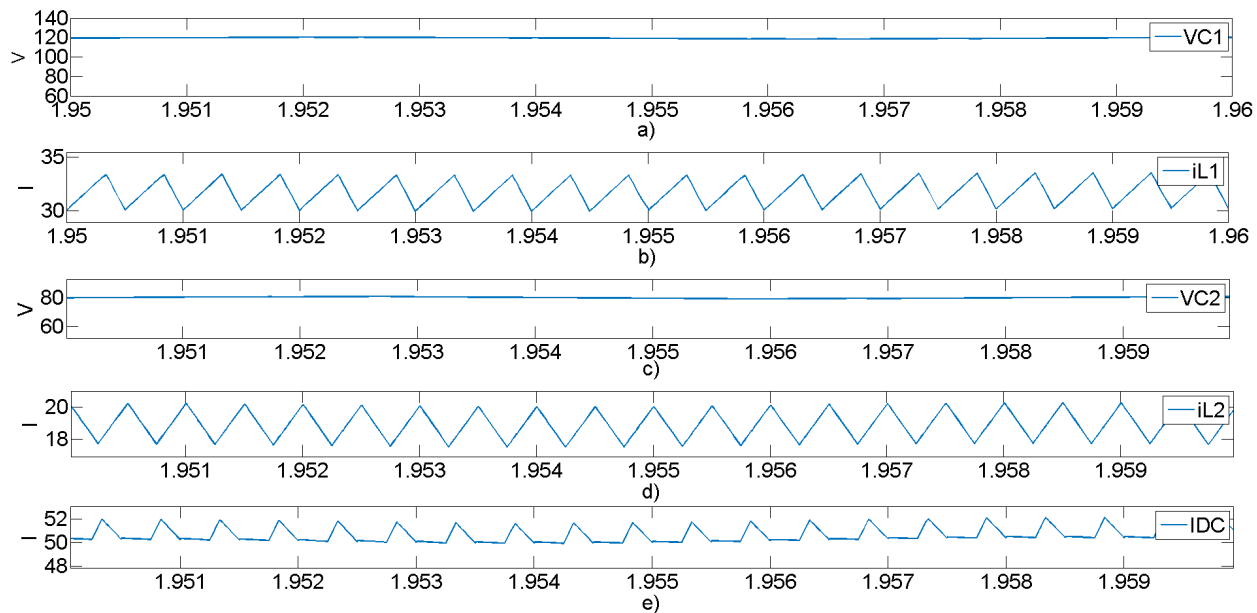


Figure 4.7. Simulation results of the DC/DC stage
a) V_{C1} b) i_{L1} c) V_{C2} d) i_{L2} e) i_{DC} .

In order to obtain these results the components values employed are enlisted in Table 4.2.2. This simulation is rated to a power of 2 kW. With the results obtained and described in this simulation scenario, the validation of functioning for both inverter variants is completed.

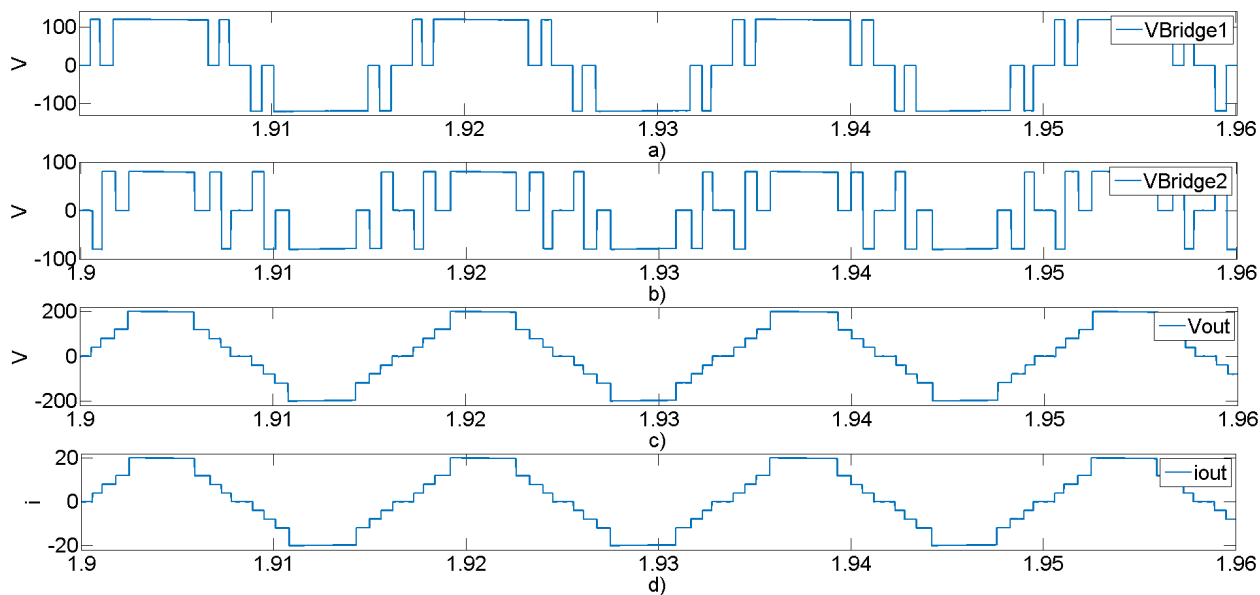


Figure 4.8. Simulation results of the DC/AC stage a) $V_{Bridge1}$, b) $V_{Bridge2}$, c) V_{out} , d) I_{out} .

And with the gathered data, the next step is to design the experimental boards for each of the variants, and evaluate the results. These are presented and studied in the appendix section.

4.3 Inverter Experimental Implementation Results

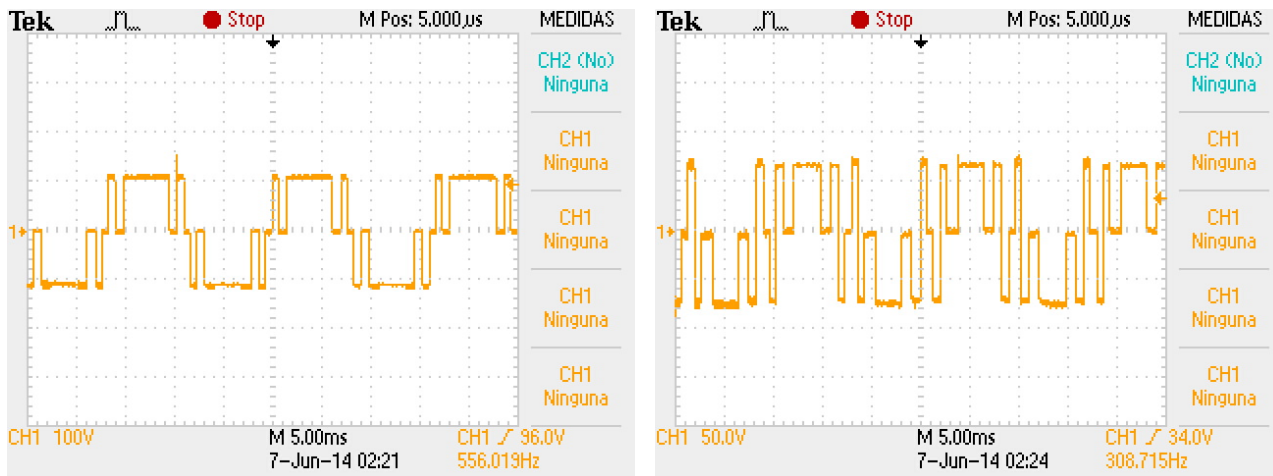
In this section will be presented the result obtained by the test of all the converters designed and constructed, which are presented in the appendix section. Each sub-section will describe the behavior of the inverter with buck and boost variants, for each of the different tests the list of components employed to obtain the results is presented.

4.3.1 Inverter Buck Variant

As can be seen in Fig. 4.9a, 4.9b and 4.10, the signals waveforms obtained in the experimental results for the buck variant of the inverter are consistent.

TABLE 4.2.2. Component Values and Settings.

Components	Simulation
Frequency	2000 Hz
$m1$	66%
$m2$	50%
$L1$	4mH
$C1$	20, 200 μF
$L2$	4mH
$C2$	20, 200 μF
R_{Load}	10 Ω
$Boost1$	120V
$Boost2$	80V
V_{DC}	40V
V_{out}	200V _p (400V _{pp})
i_{out}	20A _p (40A _{pp})
P_{out}	1993.7W
THD	15.45%

(a) Voltage and current waveforms of $V_{Bridge1}$ (b) Voltage and current waveforms of $V_{Bridge2}$ **Figure 4.9.** $V_{Bridge1}$ and $V_{Bridge2}$ signals obtained using DC/DC Buck variant.

4.3.2 Inverter Boost Variant

Similar to the results of the last section it can be seen in Fig. 4.11a, 4.11b and 4.12, the signals waveforms obtained in the experimental results for the boost variant of the inverter are consistent as well.

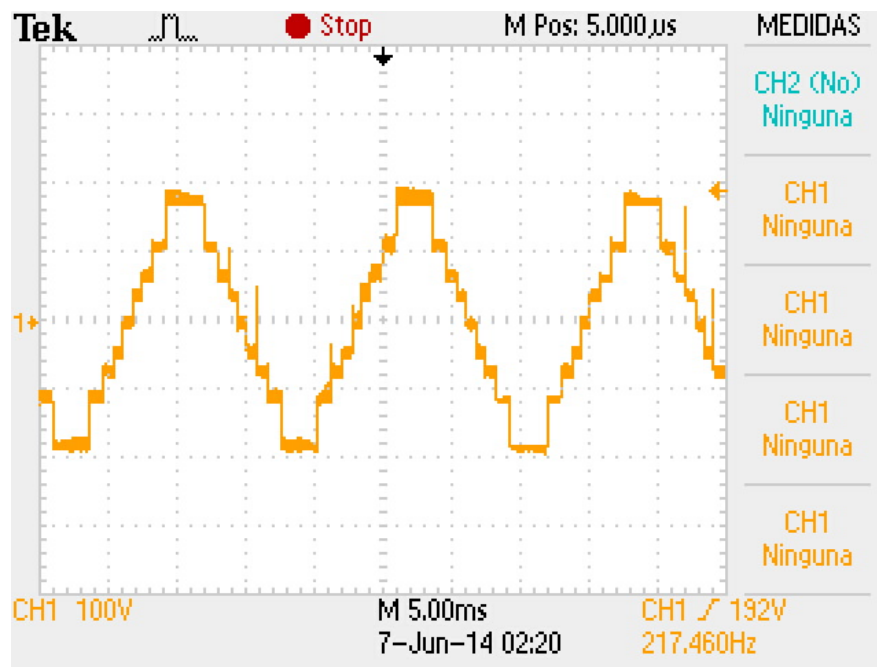
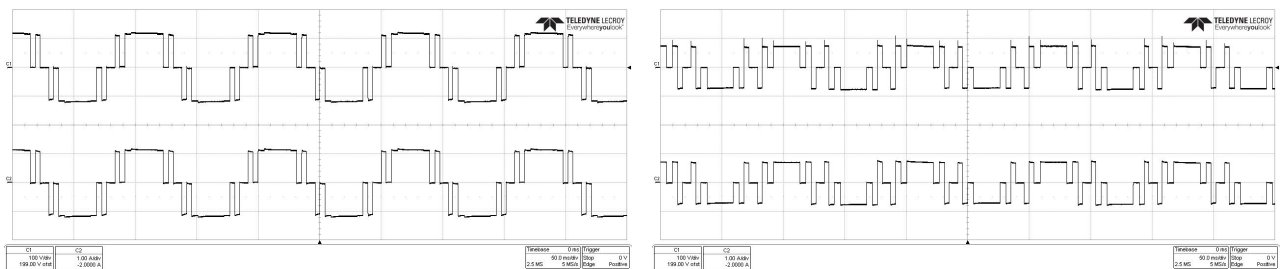


Figure 4.10. Voltage and current waveforms of the nine-levels AC output, using buck variant



(a) Voltage and current waveforms of *VBridge1*. (b) Voltage and current waveforms of *VBridge2*.

Figure 4.11. *VBridge1* and *VBridge2* signals obtained using DC/DC boost variant.

These results were performed in the experimental test bench shown in the Fig. 4.13, presented from right to left, the AF generator based in the UL 1699B norm, the DC source, the oscilloscope that serves as a data acquisition system, the proposed PV inverter topology implemented, the Texas Instruments DSP C2000 for interface with Matlab Simulink, and the loads. With the positive results obtained in this section is possible to validate the correct operation of the proposed inverter in both scenarios simulation and experimental. The next step in this work is to test the behavior of the proposal facing different cases of arc fault. The different types of loads, and the different configuration employed for the study will be analyzed in the next chapter.

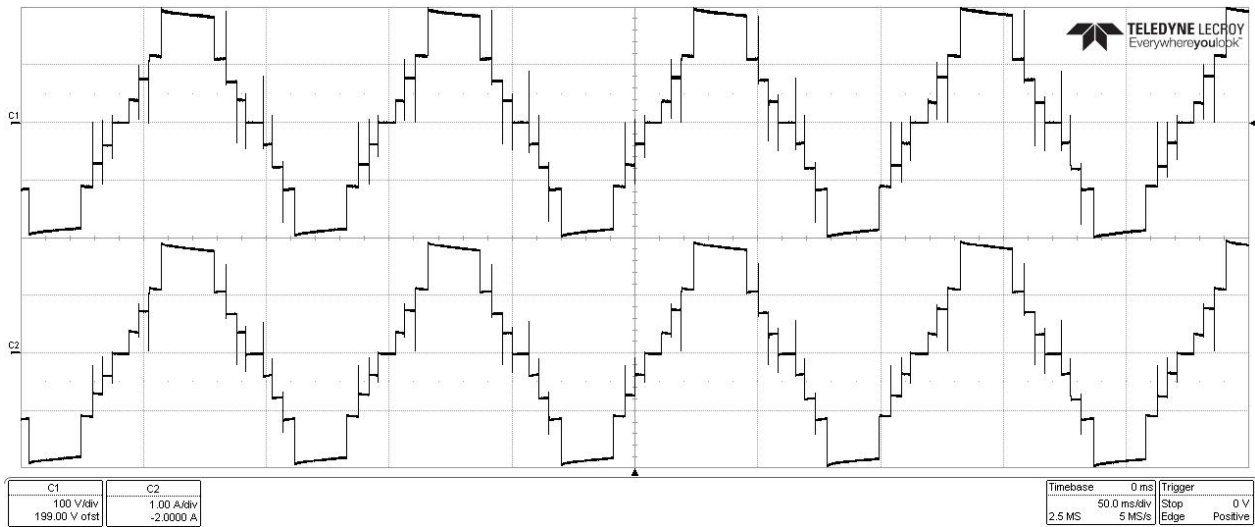


Figure 4.12. Voltage and current waveforms of the nine-level AC output, using boost variant.

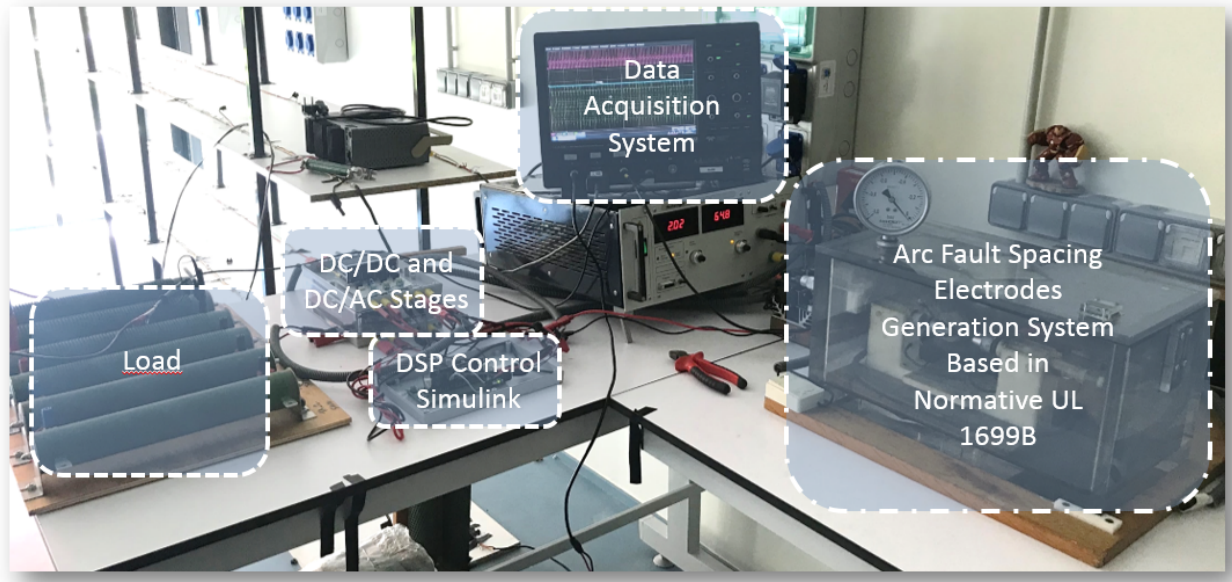


Figure 4.13. Experimental test bench.

Chapter 5

Analysis of Internal Signal Perturbations in DC/DC and DC/AC Converters Under AF

5.1 Introduction

In this chapter, the response of the proposed topology of PV inverter facing a DC series arc fault is analyzed. The results are obtained by generating an electric AF in different DC side placements, this is performed with the designed generator based in the UL1699B patent. The experimental results of this chapter will allow us to identify a novel detection technique that is detailed in chapter 6.

5.2 DC Arc Fault Generation

In order to study the electric DC AF phenomena, the standard UL1699B defines the operational modes necessary to study different AF types: Series, parallel, types of loads involved, detection time, and the method how properly to generate an Arc Fault (AF).

5.2.1 Series Arcing Test Connection

In this work the effect of series AF will be studied, using the AF generator device presented in Fig. 5.1. In order to perform the generation of an series AF the description of the main characteristics of the device is described.

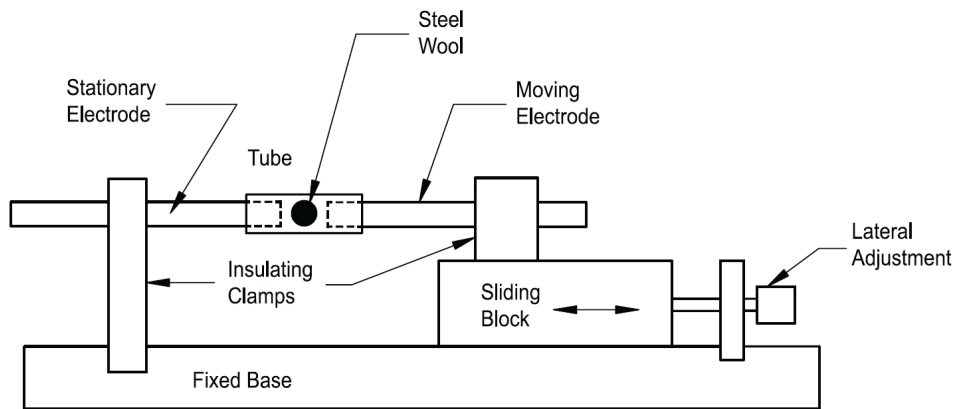
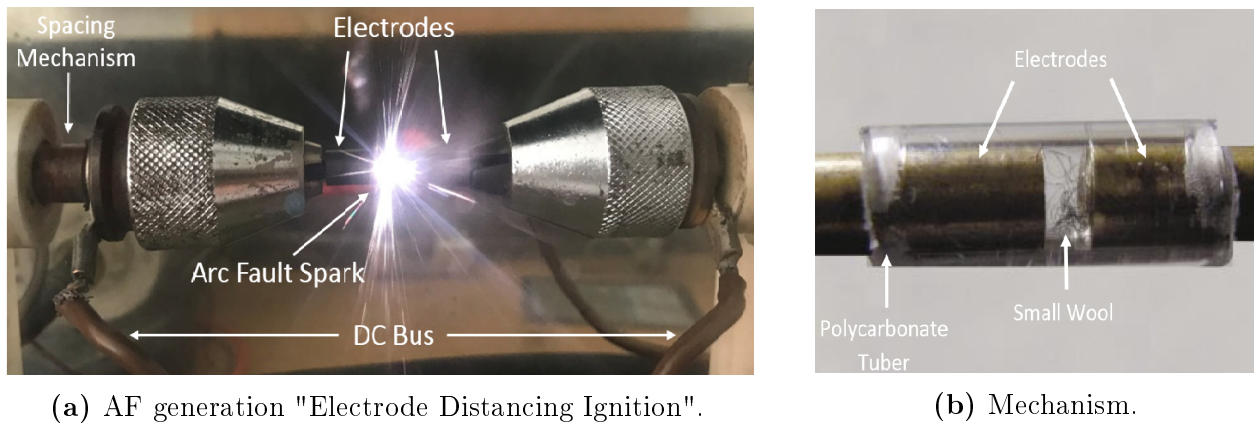


Figure 5.1. UL1699B AF generator mechanism diagram

a) For this apparatus, the electrodes, one moveable and one stationary, are made of solid copper, of 6 mm diameter. Two AF generation techniques exists, the "Fixed Distance Ignition" and "Electrode Distancing Ignition". If the first technique is employed the AF generator electrodes shall be thinned approximately 0.254mm to allow the arcing gases to escape from the tube described in Fig. 5.2 below.

b) The electrodes can be separated by using the lateral adjustment mechanism, to position the moveable electrode to a desired gap.

c) For test purposes of the first technique called "Fixed Distance Ignition", a polycarbonate



(a) AF generation "Electrode Distancing Ignition".

(b) Mechanism.

Figure 5.2. AF generation "Fixed Distance Ignition".

tube of 19 mm long can be employed as insertion over the electrodes. The tube has an outer diameter of 9.5 mm, and an inner diameter of 6.35 mm, and a wall thickness of 1.6 mm as presented in Fig. 5.2 b).

d) In the second case called "Electrode Distancing Ignition", two adjustable fixing knobs are added to the apparatus at the end of the copper electrodes as presented in Fig. 5.2. a) This method of AF generation is adopted for the experiments performed in this work, by employing copper and carbon electrodes of 6 mm at the end tip for contact.

e) For the arcing test, the circuit under test and arc generator are connected to a source of PV power to achieve the desired circuit test arc voltage and arc current. The source of PV power consist of PV modules connected in a series or series/parallel array, or a simulated PV DC power source having characteristics similar to a PV array. Then the inverter topology and load type choised are connected in order to complete the circuit under study.

The simplest AF case of study will result in the schematic circuit presented in Fig. 5.3, this circuit will allow to study the voltage and current signatures of series arc fault type, for an specific type of load. The electrode gap can be adjusted to achieve the desired arc behavior. The test is conducted by connecting the arc generator in series with the device under test using 6 mm electrodes. An AF generator, build according to standard 1699B specification is employed to perform the experimental results presented in this chapter as shown in Fig.

5.1.

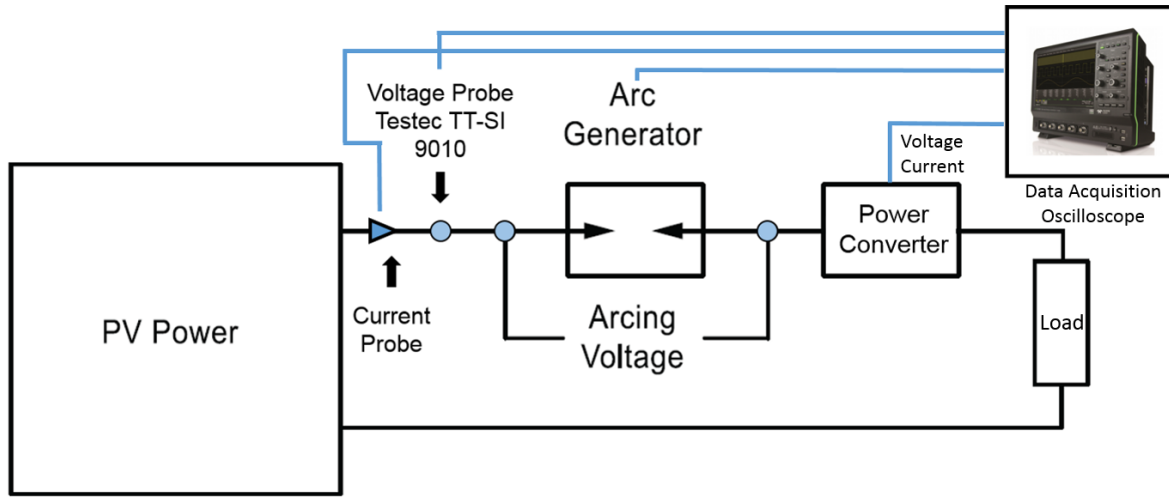


Figure 5.3. AF Load Study Schematic Diagram.

5.3 Converter Configuration for Arcing Test

In order to perform the test that will be presented in the following sections of this work the schematic diagram of Fig. 5.4 will be employed. In this configuration the source is adjusted to 40 V output that is the MPPT controller voltage limit that will be included in the experiments.

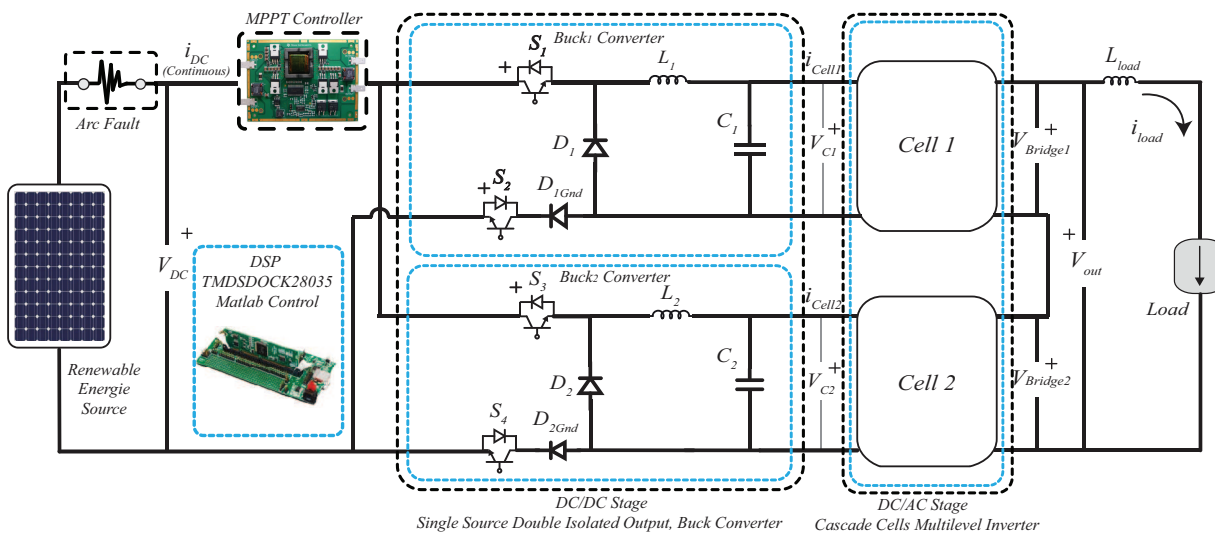


Figure 5.4. UL1699B AF generator mechanism diagram

The AF generator is immediately connected after the source in series with the main converter circuit, then both DC/DC and DC/AC conversion stages are connected and controlled by using Matlab simulink rapid prototyping board Texas Instruments TMDSDOCK28035. During the experiments, the gap between electrodes will be adjusted to two different lengths 1 mm and 2 mm, by varying the distance of the arc the harmonic spectrum patterns that change which will be analyzed in the following sections. The ambient temperature of the test bench is set to 20 C° (Celsius degrees). In order to perform the acquisition the different voltage and current values the equipment employed is: The general values employed in the AF experiments are summarized in Table 5.3.1.

5.4 Converter Behavior under DC Arc Fault

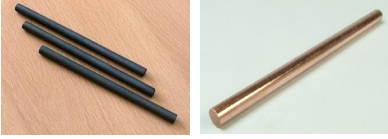
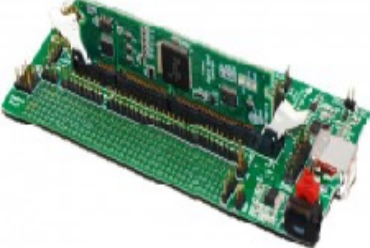




In this section the behavior of the DC/DC and DC/AC stages of the PV inverter facing an electric DC AF is studied. This signals were extracted from the experimental test bench and signals measured for each case are indicated in the schematic diagrams respectably.

5.4.1 DC/DC converter

In order to conceptualize an innovative DC arc detection strategy, it's fundamental to understand the waveforms involved in each stage of the PV inverter. Also, a deep comprehension of the changes involved in the system with the AF apparition is needed. For this an observatory stage of analysis is described below, were the different parts involved in the proposed system are studied when facing a series AF. The goal of this observatory stage is to evaluate the possible exploits for an effective detection criteria.

In order to study the AF effect, the observation stage is separated in the study of the DC/DC and DC/AC stages of the system. The test is performed by generating an AF located in the DC bus. In Fig. 5.5 is presented the schematic diagram of the DC/DC stage test, with highlighted measurement points, the values measured are V_{C_1} , i_{C_1} , V_{arc} and i_{DC} .

TABLE 5.3.1. Test Bench Equipment and Values.

<i>Componet</i>	<i>Value – Image</i>
<i>Temperature</i>	20C°
<i>Electrodes Material</i>	 <p>(a) Carbon (b) Copper</p>
<i>Electrodes Distance Gap</i>	1 mm & 2 mm
<i>Protective Case Material</i>	10 mm acrylic box
<i>Texas Instruments DSP Matlab Simulink</i>	
<p><i>High Definition</i> <i>Oscilloscope LeCroy HD4096</i> 12 – bit resolution up to 8 GHz and 20 GS/s</p>	
<p><i>Voltage Probe TESTEC TT – SI 9010</i> 7000 V 70MHZ</p>	
<i>Arc Fautl Generator UL1699B Based</i>	
<p><i>Current Probe CP030A</i> 30 A 50 MHZ</p>	
<i>Load Type tested</i>	<i>R, RL, Complex Motor</i>
<i>Load Values Tested</i>	<p>$R = 22\Omega, 47\Omega$ $L = 20mH, 141mH$ Universal Motor = 1200 W Hammer Drill Universal Motor = 600 W Vacum Cleaner</p>

The DC/DC converters are well known for modifying the input current waveform due to their switching behavior, this change the constant input current i_{DC} from the DC source to the presented waveform of Fig. 5.6.

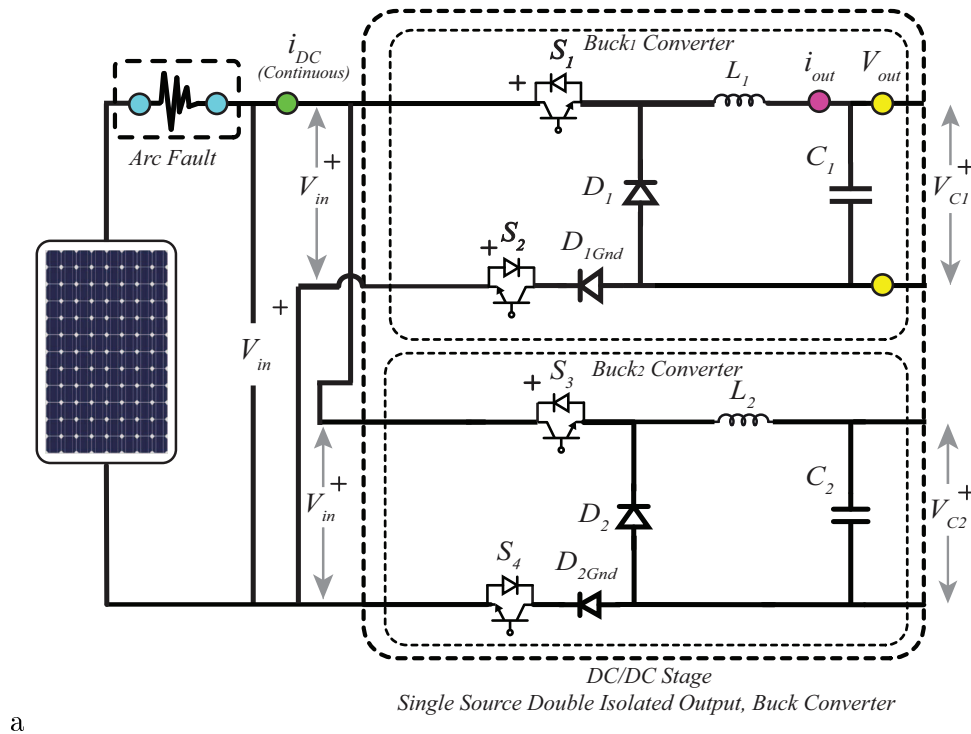


Figure 5.5. DC/DC stage (Buck variant), with highlighted measuring point.

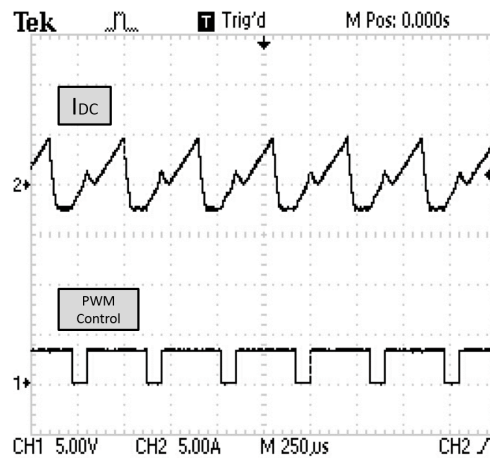


Figure 5.6. Current waveform i_{DC} delivered for the DC/DC stage.

The amplitude of this distinctive waveform is directly proportional to the duty cycle employed to control the DC/DC stage. When an AF appears, the aleatory drain of current produced, alters this typical waveform, thus perturbing the extraction of energy of the DC/DC stage. This is one example of the impact of AF in the PV inverter.

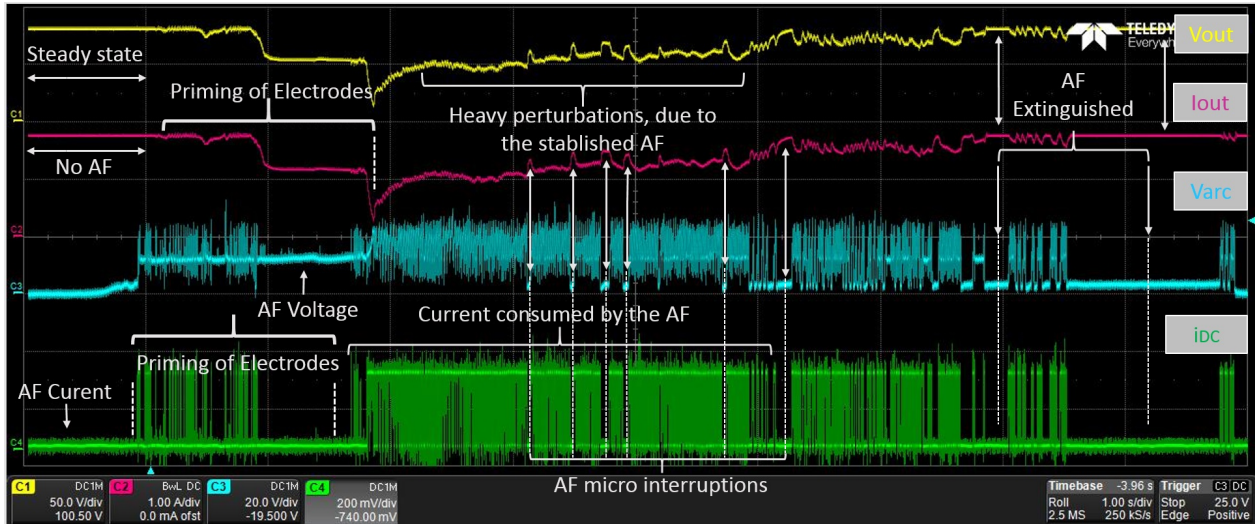


Figure 5.7. Conventional DC/DC boost converter behavior, before and after an AF.

The response of the converter is presented in Fig. 5.7. In the first stage of this experiment it can be seen that the output voltage V_{out} measured in channel 1 (C1) and current $i_{(out)}$ in channel 2 (C2) are constant just before the AF occurs. When the AF ignites, both voltage and current slightly modified during the electrodes priming, during this process the current required by the arc is not elevated due to the fact that the AF as not stable yet, but soon after, when the arc reaches a sustained state, it can be seen that both voltage and current are severely affected, and strong perturbations are visible.

Nonetheless, during these perturbations can be noticed that the AF suffers micro interruptions where no current nor voltage is consumed by the AF, these phenomena can be caused by bonded points in the electrodes due to the rise of temperature of electrodes. Since no regulation algorithm is implemented in this DC/DC stage the converter will follow the fluctuations of the arc as long as the arc persists.

The V_{arc} in channel 3 (C3) and i_{DC} in channel 4 (C4) presented also in Fig. 5.7 help to determine if the disturbances present in V_{out} and i_{out} are truly caused by the presence of an AF, this is achieved by verifying if V_{arc} is different from zero during the time t under study.

Using this process for the study of signals we can accurately perform the interpretation of the converter signals and the perturbations that an AF cause in the system, in the next section the DC/AC stage facing an AF is studied.

5.4.2 DC/AC converter

As presented in the 5.4.1 section the AF perturbations produces fast and strong voltage and current variations in the DC/DC converter. In this section the DC/AC converter implementation presented in Fig. 5.8 is studied under AF as well. The strategic point of measure for this case are V_{arc} , i_{Cell_1} , i_{out} and V_{out} highlighted in Fig. 5.8.

The results obtained with this converter facing an AF are presented in Fig. 5.9 where we can observe on the left side of the figure a near perfect nine level waveforms measured in C1 and C2 representing V_{out} and I_{out} . In center of Fig. 5.8 when the AF occurs, the voltage V_1 and current i_{Cell_1} fluctuates figure right side. In C3 is presented the arc voltage V_{arc} and in C4 we observe the current delivered from the source to $Cell_1$.

The signal V_{out} suffer an important deformation with the appearance of the AF, this chaotic and fast variations also observed with the DC/DC converter, affects the balance ratio needed between V_1 and V_2 to generate a balanced nine-level AC output. This interesting phenomena is present in both V_{out} and I_{out} , where the number of levels and symmetry of the signal change from its typical waveforms. This fluctuations produce a change in the default harmonic content of a nine level signal.

Both signals V_{out} and I_{out} doesn't seem to be perturbed during the brief millisecond of the electrodes priming before the AF is fully established. Nonetheless, immediately half cycle after the AF appears, the signal V_{out} passes from nine levels to only five levels, and a complete cycle after the AF, it passes to seven levels.

In C4 current I_{out} experience similar changes when the AF is established. In this case, the most noticeable change is that the signal losses the totality of the upper switching steps, and

during the last cycle, we also observe a width steps change. This effect is more pronounced when the V_{arc} variations amplitude become higher.

This lost in the number of levels generated by the multilevel inverter, and the the technique to exploit it for AF detection will be analyzed and explained in chapter 6. From Fig. 5.8 when the arc is established the I_{arc} that in reality is the current supplied to $Cell_1$ also suffer the disturbances losing its periodic characteristic which are explained with the aid of Fig. 5.6.

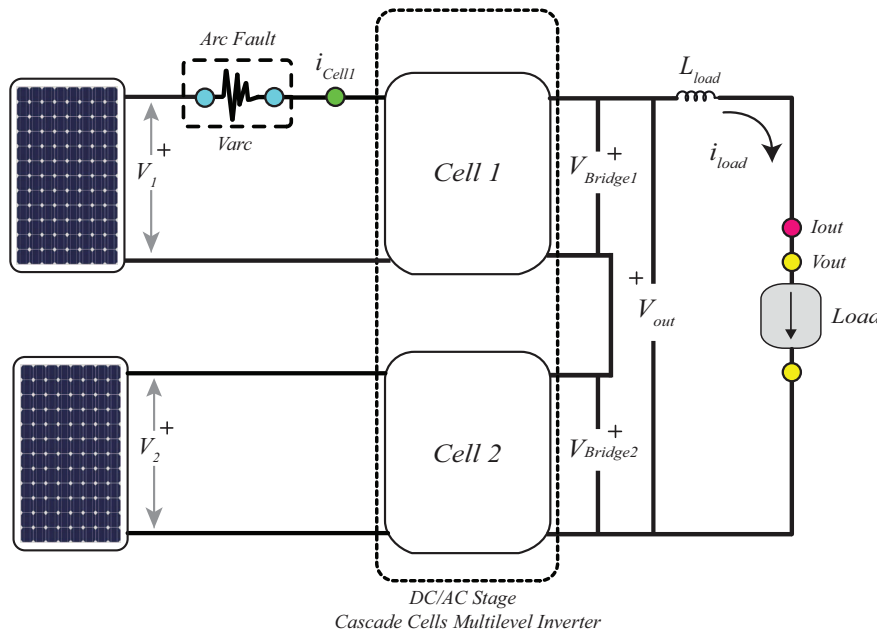


Figure 5.8. Cascade cells configuration for AF testing.

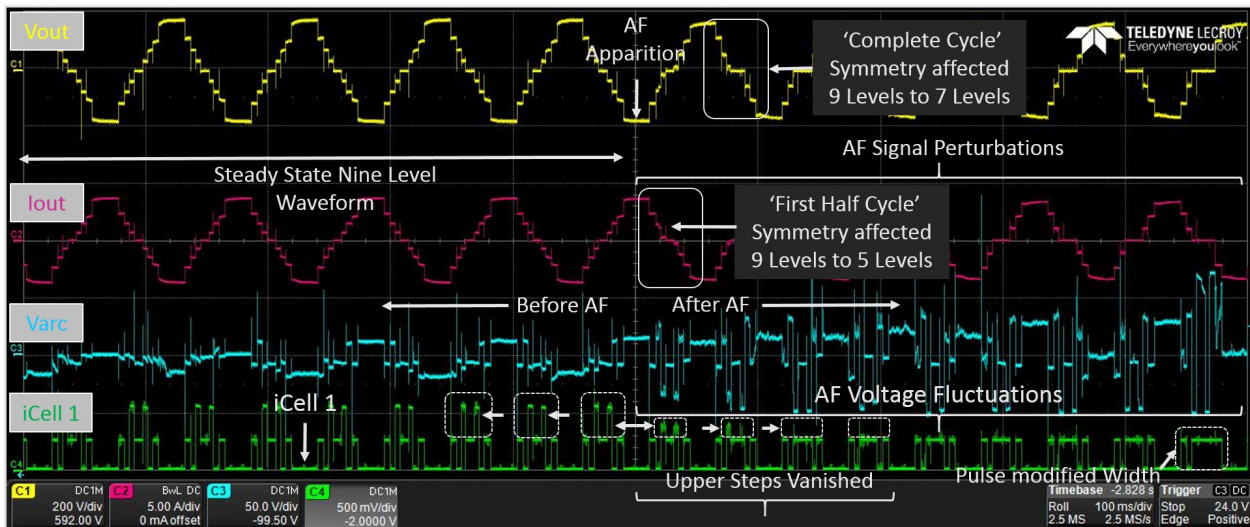


Figure 5.9. Multilevel waveforms obtained under AF.

Considering that both types of converters DC/DC and DC/AC are affected by the appearance of the AF, the changes in voltage and current, and the lost of symmetry can be exploited to achieve detection of the AF, nonetheless another factor that needs further study is the influence of a common energy extraction optimization algorithm present in most renewable energies systems, and is the MPPT tracking system. The influence of this control during a series AF is studied in the next section.

5.5 Arc Fault Influence in a MPPT Tracking System

To ensure the optimum power extraction of solar panels, a DC/DC converter is often employed called MPPT tracking. This additional converter can be connected individually for each panel or also installed in series with the DC bus (when panels are arrange in series and parallel to meet the system V/I requirement) by using a single converter. For the next experiments we will employ a single MPPT in series with the source, two possible configurations are studied, with an AF influence tested by generating it before and after the MPPT converter.

5.5.1 MPPT Arc Fault Test Considerations

In order to perform the experimental tests with a complete structure of the system, the values presented in TABLE 5.5.1 are employed. The selection of components was based in the operating values of the chosen MPPT control module ('SM72445' by Texas Instruments) presented in Fig 5.10. This module is capable of a constant regulation of up to 40V.

With this parameters considered the test are performed by generating a series AF in two different scenarios. In the first case the AF is generated before the MPPT controller, and second the AF in generated after the MMPT. The changes and perturbations observed are described with detail for each case in the next section.

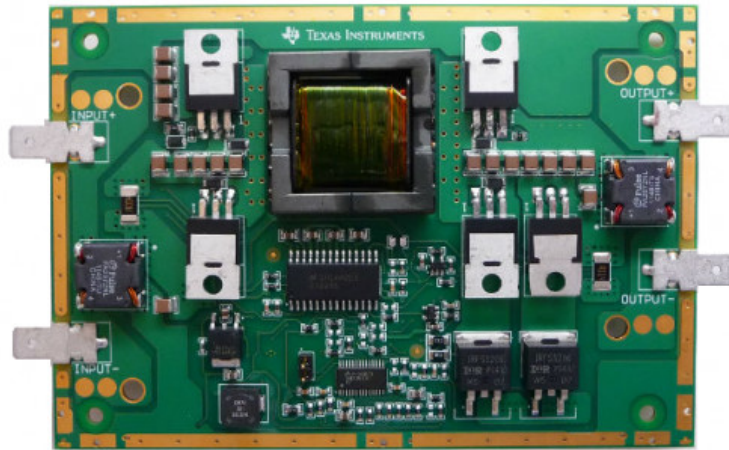


Figure 5.10. Texas Instruments MPPT Prototyping Board.

TABLE 5.5.1. Experimental Values for MPPT Test.

<i>Components</i>	<i>Value</i>
<i>Frequency</i>	$2kHz$
<i>DutyCycle1</i>	45%
<i>DutyCycle2</i>	32%
L_1	$438\mu H$
L_2	$438\mu H$
C_1	$2200\mu F$
C_2	$2200\mu F$
<i>Load</i>	47Ω
V_{in}	40V
V_{out}	$50V_p(100V_{pp})$

5.5.2 Single Phase Arcing before MPPT Module

To analyze the influence of an AF in the first case where the arc is located before the MPPT converter, the schematic diagram presented in Fig. 5.11 is employed, in this test the data acquisition of three waveforms is performed, the first point of measure corresponds to $V_{Bridge1}$ measured with C1 in Fig. 5.12, in C2 the V_{arc} is measured, essential signal to confirm if the fluctuations in C1 and C3 are related to the AF appearance. Finally in C3 the input current I_{in} is measured.

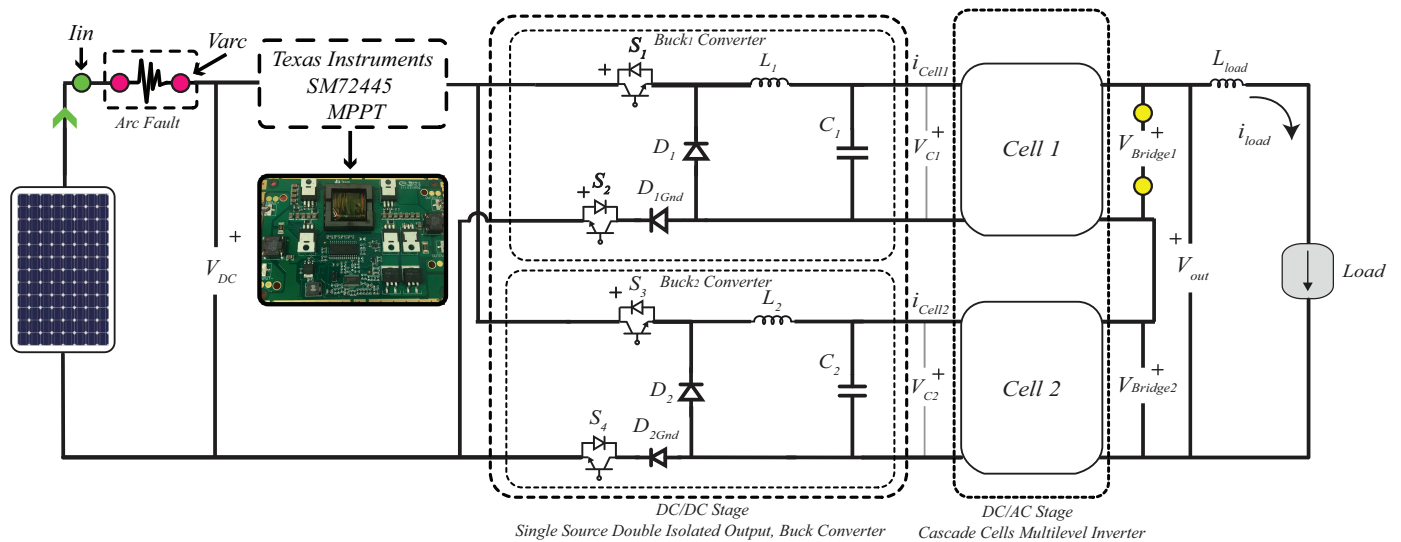


Figure 5.11. Schematic diagram for AF testing with AF before MPPT module.

With the experimental signals obtained in Fig. 5.12, an AF is generated in the DC bus and signals are acquired across a 5 seconds time length. In this figure we can observe in C1 a drop on the $V_{Bridge1}$ output voltage related to the AF ignition, this voltage drop is equivalent to the AF sustained voltage.

In C2 we observe the V_{arc} , which remains constant until the MPPT controller starts to compensate the loose of voltage caused by the arc. Although, the MPPT control module will attempt to keep the output voltage constants at 40V, regardless of the AF apparition this regulation has no success since it's limited by the elevation capabilities of the converter.

This behavior can be observed in Fig. 5.12, when the voltage drop surpass the converter capability to regulate, and then the control ability to regulate the voltage is loose and limits the regulation to follow the fluctuations generated by the AF only.

Even if the arc is extinguished, the algorithm of the MPPT converter is not capable of recovering its initial stable regulation, so the voltage is distorted even more after the fault has stopped. This phenomena can be observed in the current I_{in} presented in C4.

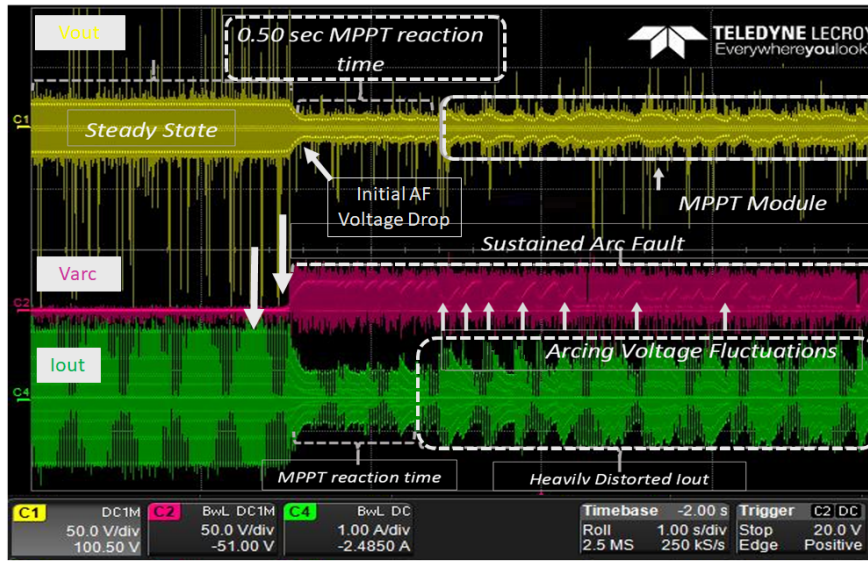


Figure 5.12. Experimental results of arcing before MPPT module.

5.5.3 Single Phase Arcing After MPPT Module

The implemented schematic for this experiment is presented Fig. 5.13. In this section the acquisition of signals will be focus on V_{out} , V_{arc} and I_{out} . The reason behind this change is to validate that the fluctuations generated by the AF also affect these points of measure in the converter.

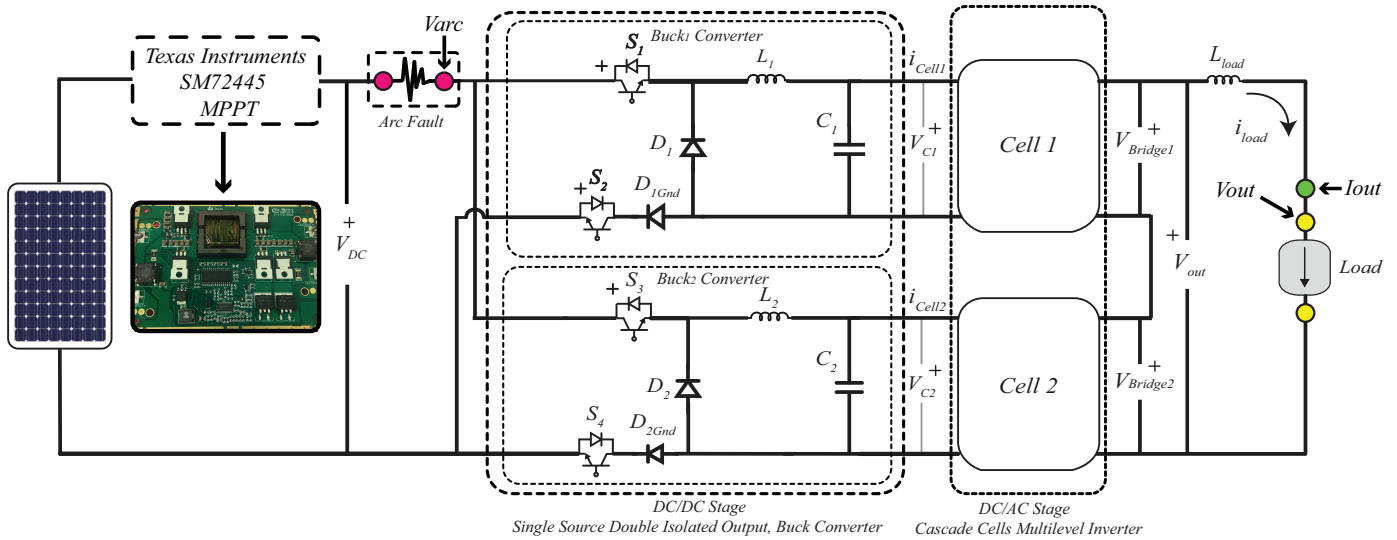


Figure 5.13. Schematic diagram for AF testing with AF after MPPT module.

In this case the MPPT presents a similar behavior to the previous case, as presented in Fig. 5.14. In C1 is presented the signal V_{out} , in C2 the V_{arc} and in C3 the I_{out} . For this case is observed that the control algorithm assumes a more active voltage regulation behavior. Nonetheless, the control is still limited by the amount of current that can be delivered by the MPPT controller.

Because of this limitation, after approximately 0.5 seconds (that is the average reaction time of the MPPT module) of the initial V_{out} drop, the MPPT detect this change, which is traduced in a increased current consumption of the system. In an effort to raise the loose in voltage and thus compensate for the drop detected, the MPPT module will deliver more current, this starts a vicious loop, because by increasing the delivered current, the AF will proportionally augment its current consumption.

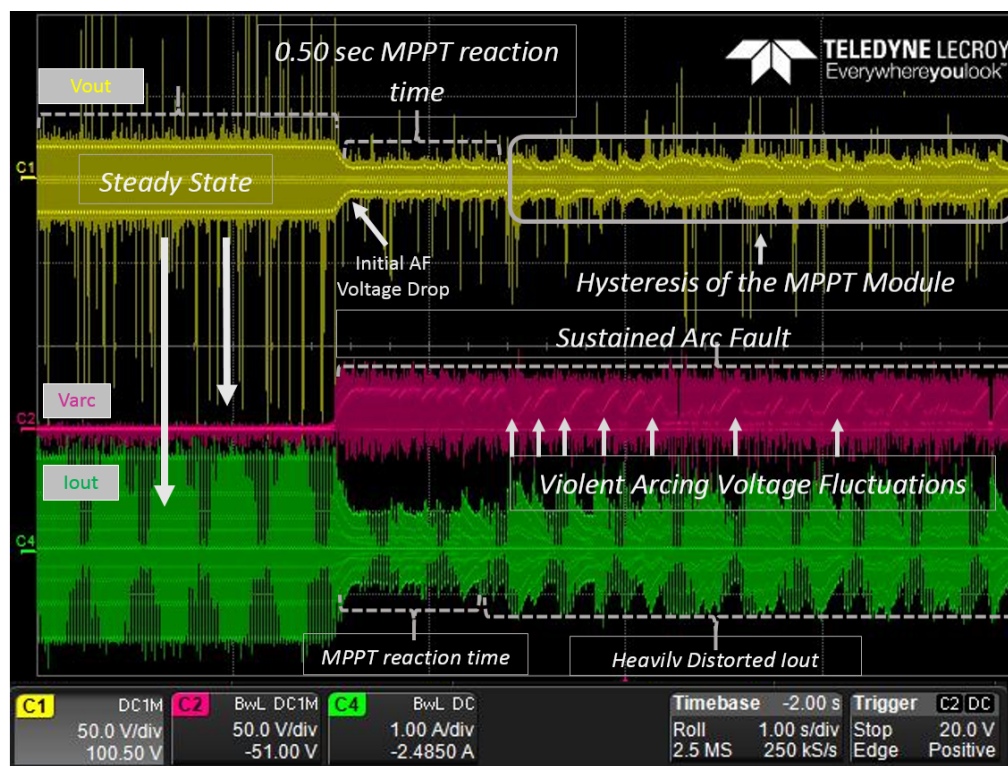


Figure 5.14. Experimental results of arcing after MPPT module.

This explains why the fluctuations in V_{arc} increased after the MPPT reaction time, which is also visible in I_{out} in C4 of Fig 5.14. With the observations studied for both cases of MPPT facing an AF, it can be concluded that the AF has an important impact on the MPPT system. The control loop malfunctioning of the MPPT facing the AF, caused stronger fluctuations in V_{arc} , thus affecting in a important manner V_{out} and I_{out} gradating the THD of the output signals.

This behavior was observed whether it appears before or after the module, being the failure after the MPPT the more problematic of these two cases. This because it favors the maintenance of the arc, given that the control algorithm will try to deliver more current to the system in an effort to raise the voltage, current that will be consumed by the arc.

With the results obtained in this chapter, we can conclude two facts: the first is that the internal signals in both types DC/DC and DC/AC converters are affected by the appearance of an AF, and second that the use of a MPPT module in the system does not provide any advantage in the prevention of AF, instead the control algorithm worsened the AF behavior when trying to regulate the voltage drop generated by the AF.

With these is possible to proceed with the development of a detection technique that can take advantage of the AF disturbances in the power converter. This will be presented in next chapter, for both cases: an isolated PV system and for a grid interconnected.

Chapter 6

Study of Harmonics Decomposition Technique in Both PV Isolated and Interconnected Systems Using Experimental Signals

6.1 Introduction

In this chapter will be presented the study of the frequency analysis applied to experimental signals measured on the new multilevel proposal in different configurations. Commonly used stand alone and grid interconnected systems will be considered in order to validate the results, these will allow to validate the harmonic decomposition detection technique for AF in low power DC systems.

This frequency analysis will be applied specifically to signals $VH2$ and I_{out} , the points of measure are detailed further into this section in Fig. 6.3. The developed test bench, is prepared according to the values in table 5.5.1. The experiments for stand alone systems are performed in normal conditions and on presence of AF considering each type of load.

The current and voltage signals are extracted from the experimental test bench by sampling at 1M samples/sec. The harmonic analysis of experimental signals are made using Matlab code.

In order to perform the grid interconnected system, the load type is changed at the output of the converter, this since the LCL filter detailed in section 6.5.3 remains the same throughout the different tests.

6.2 Harmonics in AC Systems Under Normal Operation

In order to fully exploit the changes that appear in the system when facing an AF, the main symmetry characteristics of the inverter have to be studied during normal operation.

The Total Harmonic Distortion (THD) index is employed to study these signals. This represents the measurement of the harmonic distortion present in a signal and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

In conventional AC electric grids, in common configuration or with inverters, the current and voltage waveforms are periodic functions, and they possess half wave symmetry in normal operation. In this condition, the harmonics components that make up the signal is of type *Odd*.

With the different variety of perturbations that can appear on this systems, the half-wave symmetry remains unaffected, nonetheless, in case of an AF this symmetry of the signals are affected, hence a detection approach can be proposed based on this perturbations, as will be analyzed throughout the next sections.

Where V_h is defined as the harmonic of order h and θ_h has the angle of the harmonic.

For a periodical signal, the THD is defined in equations 6.1 and 6.2 for voltage and current:

$$THD_V = \frac{\sqrt{\sum_{h=2}^N V_h^2}}{V_1} \times 100\% \quad (6.1)$$

$$THD_I = \frac{\sqrt{\sum_{h=2}^N I_h^2}}{I_1} \times 100\% \quad (6.2)$$

$$IHD_h = \frac{V_h}{V_1} \times 100\% \quad (6.3)$$

Equation 6.3 define the individual harmonics distortion for harmonic h . Equation 6.1 can be rewritten as:

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + \dots}}{V_1} \times 100\% \quad (6.4)$$

The THD for even and odd harmonic can be defined as:

$$THD_{even} = \frac{\sqrt{V_2^2 + V_4^2 + V_6^2 + \dots}}{V_1} \times 100\% \quad (6.5)$$

$$THD_{odd} = \frac{\sqrt{V_3^2 + V_5^2 + V_7^2 + \dots}}{V_1} \times 100\% \quad (6.6)$$

The THD's defined in 6.4, 6.5 and 6.6 are used to analyze the AC voltage (since this signal is less affected by the feed load) response of the PV converter under DC AF conditions. The theoretic basis for this is presented in appendix.

It should be noted that under AF conditions, the output AC multilevel signal suffers aleatory loose of levels, then changing the THD, increasing the inexistent THD_{even} . This phenomena results of the half-wave symmetry lost.

In power electronics, the main goal of multilevel converters is to generate as few harmonics as possible, by employing the fewer number of electronics components. With the generation of a stepped waveform (employing cascade cell multilevel topologies as presented in sections 5.5.2 and 5.14) the converter is generating a signal of 60 Hz whose THD is 15.45 % as shown in Fig. 6.1. To obtain this result the nine levels output voltage is analyzed using Matlab Simulink taking into consideration 5 cycles of the steady state signal. Since the total number of levels generated is a odd number, the harmonics components in the signal will be excursively composed of odd harmonic. This is a key factor to highlight for further analysis of the signals presented in this chapter.

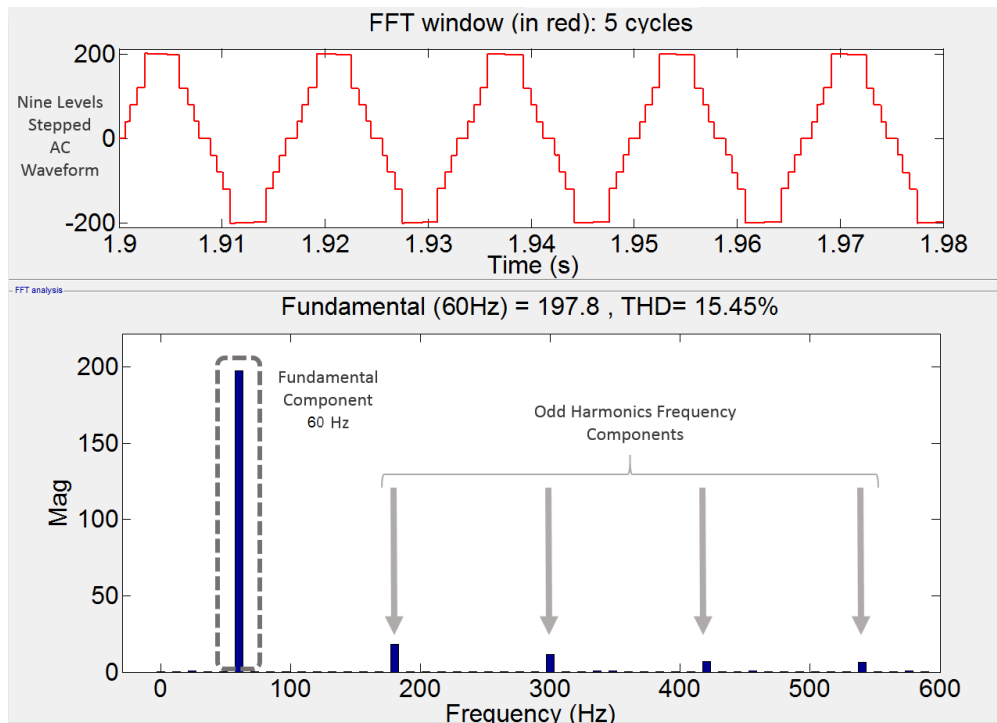


Figure 6.1. THD study of multilevel waveform.

In the next section this knowledge will be put into practice by analyzing both type of system, stand alone and grid interconnected systems from a harmonics perspective, which will serve as an ideal introduction to the detection technique proposed in this work.

6.3 Signals Analysis Guidelines for Stand Alone System Tests

The initial test is performed using resistive a load, with this configuration the signal obtained is presented in Fig. 6.2. The method employed for the analysis of experimental signals is performed using Matlab. First the experimental signals $V_{Bridge2}$ and I_{out} are sampled at 250ks/s across 2.5 sec ($T=4166$ samples), and in this particular case a zoomed window of 9 period (since the output of the converter is a 60 Hz $T=16.66\text{ms}$ [$9T=149\text{ms}$]) is presented where the AF is triggered in order to visualize the change in harmonics and exploit these as a detection criteria for series AF.

Then the FFT calculation (represented across time) is performed to the entire length of the experimental signals and presented in Fig. 6.2 b). We observe the converter operating under normal conditions from time 0 - 49.8 ms, where the voltage presents no alteration and the nine-level waveform is generated without perturbation.

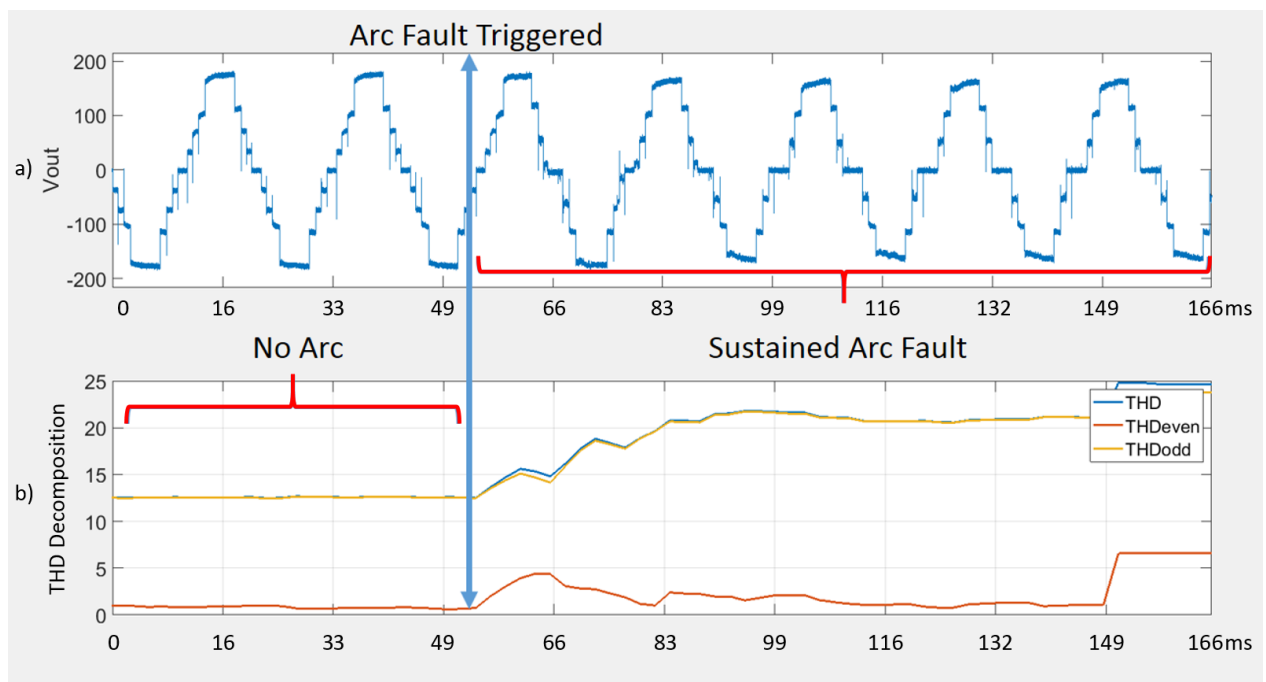


Figure 6.2. THD decomposition in THD_{even} and THD_{odd} before and after an AF.

In the other hand when an AF is produced between time 49.8 - 166 *ms*, it can be seen that the arc fault is affecting the waveform of V_{out} . The AF caused a significant increase of 10-12 % in the total THD, these changes can be easily visualized. With the constant and random variations produced by the arc in the supplied voltage of the multilevel inverter, the balance of voltage between cells ($V_{Bridge1}$ and $V_{Bridge2}$) is altered. This affects symmetry of the signal, during this perturbation we can observe a loose of levels in V_{out} and also a the zero crossing time of the voltage is increased.

The multilevel converter generates a nine-level stepped signal, this waveform is the result of the addition of voltage waveforms $V_{Bridge1}$ and $V_{Bridge2}$, generated by $Cell_1$ and $Cell_2$ of the converter topology. In the graphic of Fig. 6.2 b), the frequency spectrum analysis of V_{out} is presented in blue.

However, has to be noted that the change in this value can easily be modified by several factors that are not related to an AF (Type load, variations in irradiation, instant load changes, etc.). However the THD is composed of two main groups of harmonics, even (THD_{even}) and odd (THD_{odd}), which can be studied independently, as necessary as presented in Fig. 6.2 b).

When employing a cascade cells multilevel inverter, usually the last cell generates a more complex commutated signal, hence more sensible to perturbations which is ideal for this study. For this reason the voltage $V_{Bridge2}$ is the signal employed in the study of experimental tests, this since the perturbations will be more visible as mention before due to the commutation pattern of the converter. A second advantage of measuring this voltage in terminals of each cell, is that the signal doesn't suffer any modification despite the type of load.

In addition to this signal, the use of a complementary signal will be explored by measuring I_{out} in the system, this in order to improve the overall performance of the detection. The schematic employed and the points of measurement are presented in Fig. 6.3.

The harmonics decomposition technique presented in Fig.6.2 b) results fundamental for the proposed detection technique. The base of this relies in the fact that, the voltage output is a nine-level signal. This is translated into a frequency spectrum that is purely composed by "odd" harmonics. Then when an AF appears, it clearly the complete THD spectrum, but more specific due to the symmetry lost of the original 'purely odd harmonics'(nine-levels) THD_{odd} signal, the THD content is contaminated with pair harmonics. This increase in $THDe$ after the AF appearance can be exploited by using the converter internal signals.

Ideally, the content of even harmonics in the signal is 0%, however when dealing with real signal, has to be considered that disturbances of the dv/dt type are present due to the IGBT's switching, and other irregularities that will slightly increase this index. This phenomena happen only when an AF in generated in the system, nor changes in the load, radiance modifications or complex loads like motors affect this criteria of detection, as validated and presented in the experimental test bench. The harmonic content of the THD_{even} is a suitable criterion for detection since its only triggers when an arc fault appears.

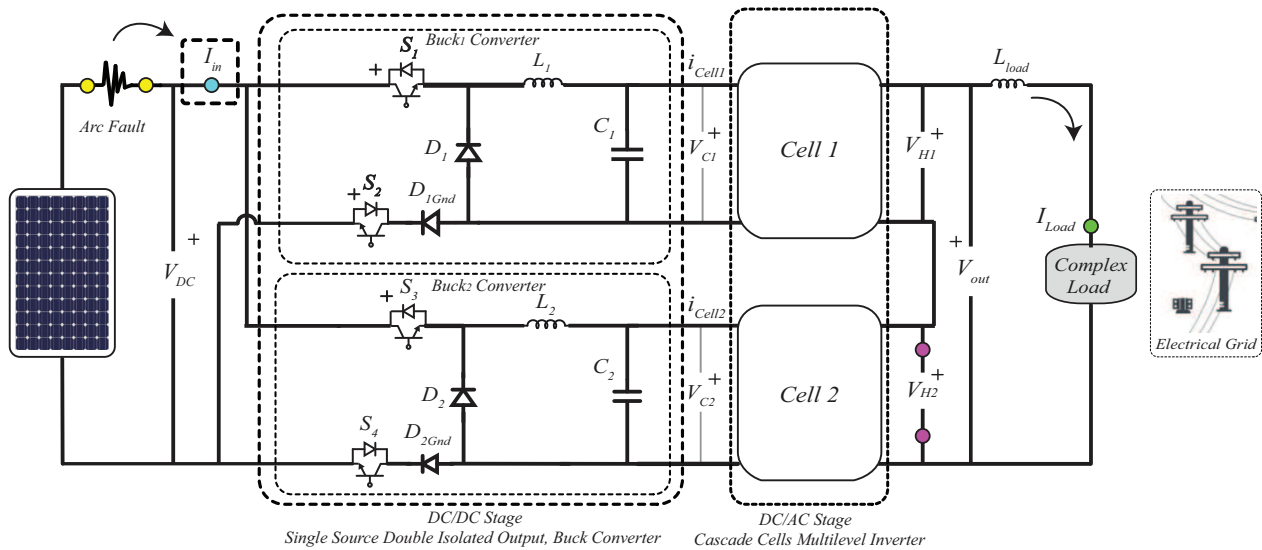


Figure 6.3. AF Testing protocol for different loads, with highlighted measuring points.

Since the DC/AC conversion stage generate an approximative waveform of a 60Hz perfect sinusoidal waveform the Fourier analysis can also e applied to $V_{Bridge1}$ (V_{H1}) and $V_{Bridge2}$ (V_{H2}) because this two signals shares the same T of the 60Hz fundamental.

Clearly the THD will be high, but if this content is studied by isolating the THD_{even} component, will be obtained a detection criterion that will remain unaffected by changes in the load, irradiation and with a fast response time.

For the experiment performed in Fig. 6.2 a resistive load was used, which has little influence on the output waveform. In a real scenario, the inverter will face far complex loads of the RLC type. Therefore, to assess the efficiency of this criterion, the topology of the inverter is proven by generating arcs with the following four combinations of complex loads: RL, RL, Drill-motor, Vacuum-motor.

6.4 AF Influence Study in a Stand Alone Isolated PV System

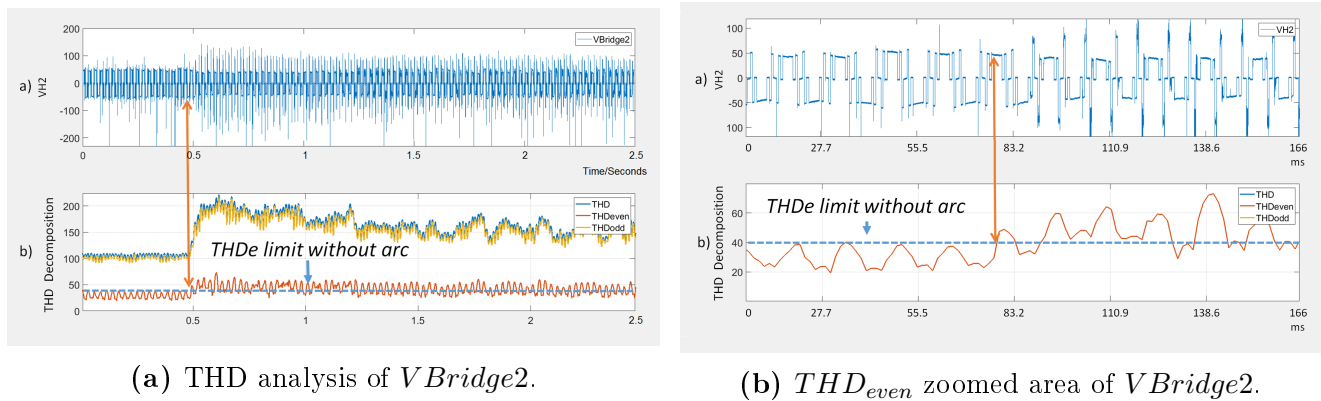
In this section both signals $V_{Bridge2}$ and I_{out} are considered and analyzed in order to study the variations in $THDe$ when an AF occurs, its fundamental to verify if the $THDe$ is not modified despite the different type of load feed.

6.4.1 THD Case (1) - Resistive and low inductive load (22ohms + 20mH)

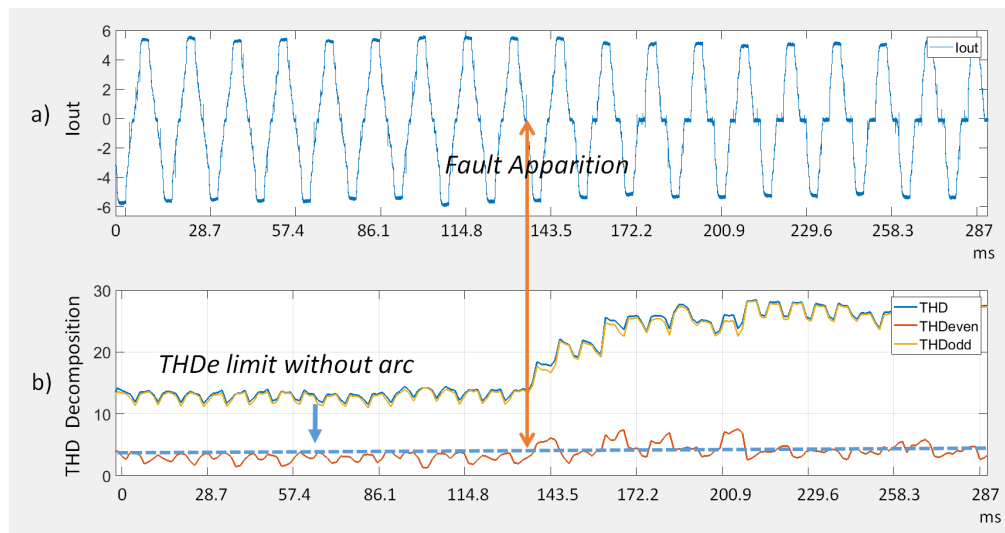
The FFT analysis of $V_{Bridge2}$ and the harmonics analysis of THD_{even} and THD_{odd} are presented in 6.4 a). When the arc ignites THD strongly rises, above its usual value on steady state. In Fig. 6.4 b) is presented the same harmonic analysis in the zoomed area when the arc appears. During steady state the $THDe$ oscillates between 1% and 18%, but when the arc ignites this oscillations increased to reach a max of 60%.

In Fig. 6.5 the analysis is performed on I_{out} . Given the inductive nature of the load, the stepped multilevel is smoothed close to a sinusoidal shape.

The I_{out} THD, increases from 14% to 25% with the appearance of the arc, and the THD_{even}

(a) THD analysis of $V_{Bridge2}$.(b) THD_{even} zoomed area of $V_{Bridge2}$.**Figure 6.4.** $V_{Bridge2}$ harmonics decomposition.

risers only about a 3% during ignition. The use of this signal as a main detection criteria is not suitable, nonetheless exploitable as a complementary signal.

**Figure 6.5.** I_{out} THD Decomposition technique.

6.4.2 THD Case (2) - Resistive and strong inductive load RL Load (22ohms + 141mH)

In this case of study, a heavy inductive load is employed, to stress the converter and evaluate if $V_{Bridge2}$ will still be reliable at terminals of the converter. In Fig.6.6 a peculiar phenomenon is observed, once the arc is initiated, after passing 1 second the $THDe$ of $V_{Bridge2}$ returns to its nominal value. This means that if an arc is triggered during the feeding of an extreme inductive load, the detection system needs to have a response time of

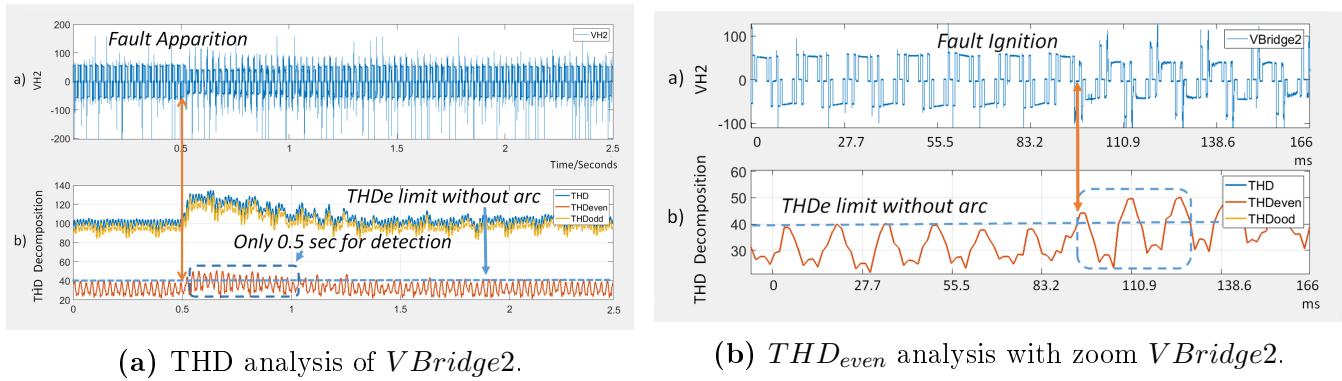


Figure 6.6. VBridge2 harmonics decomposition.

less than 1 sec to be able detect the fault. otherwise the system will continue to operate while the fault continues damaging the photovoltaic infrastructure. The inductive effect of the load transform completely the signal I_{out} into a sinusoidal. Nonetheless a small peak in the $THDe$ is still present during the AF ignition, which validate that even under this difficult circumstances the employment of THDe remains a validate criteria to perform AF detection. Ones the behavior of the THDe is validated with this load, the next experimentations performed will include complex loads such as motors to study further the behavior of the THDe.

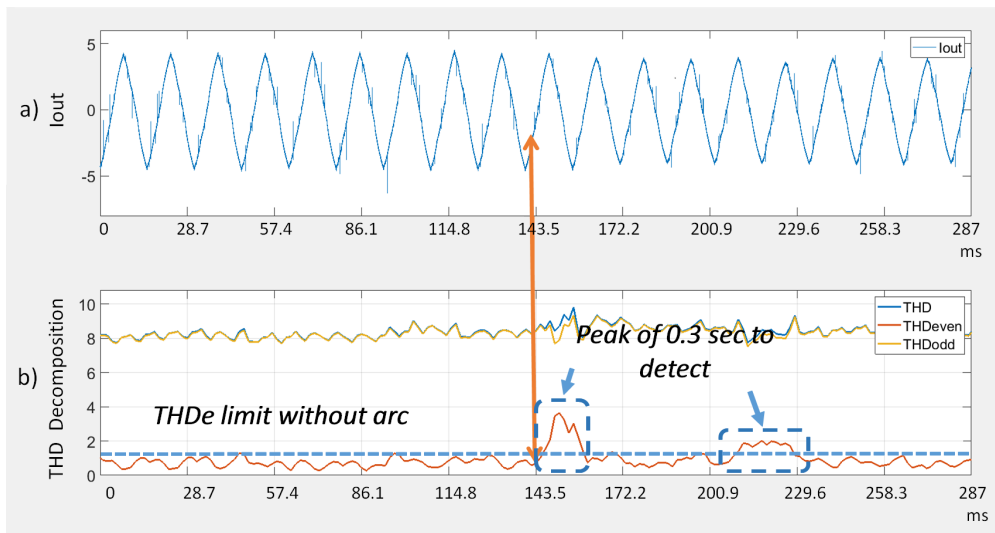


Figure 6.7. I_{out} Harmonic Decomposition.

During the operation under an important inductive load the increase in $THDe$ still has the potential to achieve detection, this given the increased of $THDe$ of 27% during AF ignition. We can observe a similar behaviour in the variations of $THDe$ related to the appearance of the AF. As presented in Fig. 6.6 b), these results are the same as for the low inductive load presented in Fig 6.4, the only difference is that the variation of $THDe$ only last for 0.5 seconds.

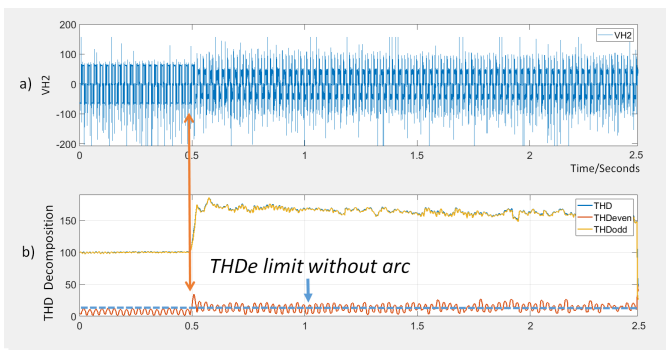
Also in Fig.6.7 the harmonic study of I_{out} is presented, which follows the same behavior of the last experiment presented in Fig. 6.5 with only a small increase of 3% in the THD_{even} during arc ignition.

6.4.3 THD Case (3) - 1200W Hammer-Drill Test

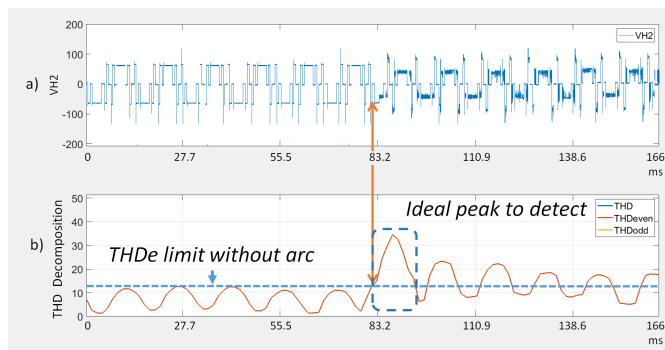
To perform the evaluation of this technique, in detailed and complete manner, a hammer-drill with a power rate of 1200 W is employed as complex load. Despite the fact of being feed not whit his nominal value due to the power to which the inverter is tested, this represents a challenging load since it injects a large amount of distortion type di/dt into I_{out} . The results obtained are presented and analyzed in a similar manner. As for RL type load tested before. In Fig. 6.8 a) the evolution of $VH2$ during a lapse of 2.5 sec is presented. For this load, the amplitudes of the the THD oscillations increases from its amplitude from 1-18% to 5-33%. Given this observation the AF detection can be perform. Despite disturbances of the di/dt generated by this load, the $THDe$ index obtained by the FFT on I_{out} , will still give a accurate detection indication as presented in Fig. 6.9.

6.4.4 THD Case (4) - 1200W Vacuum Cleaner Test

For the final test, a vacuum cleaner of 1200W is employed as load. In Fig. 6.10 a) and b) it's possible to observe the changes in $VH2$ before and after the AF. In this test an increase in the oscillations of THD_{even} is observable, similar to the drill test, since the index increased from 1-18% of amplitude to 5-30%.



(a) THD analysis of $VH2$.



(b) THD_{even} analysis with zoomed area of $VH2$.

Figure 6.8. $VH2$ harmonics decomposition.

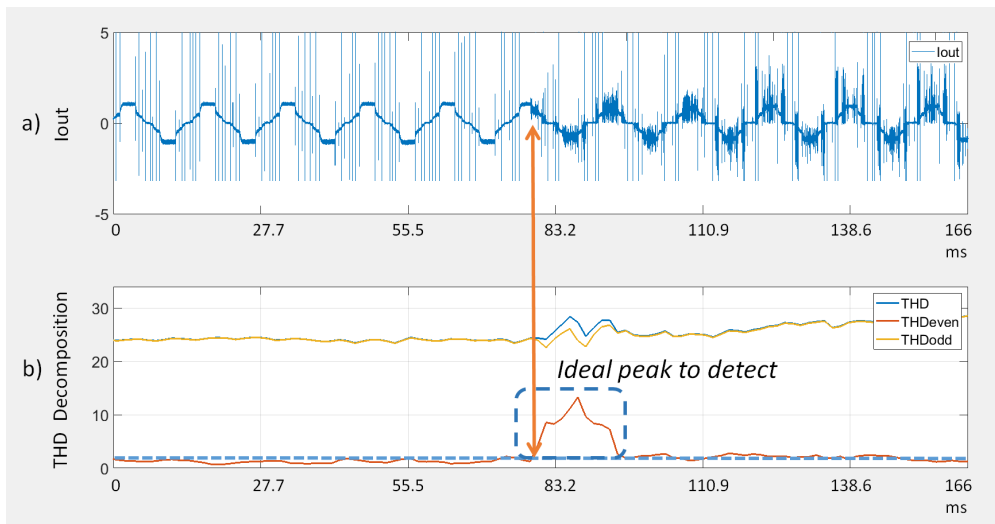
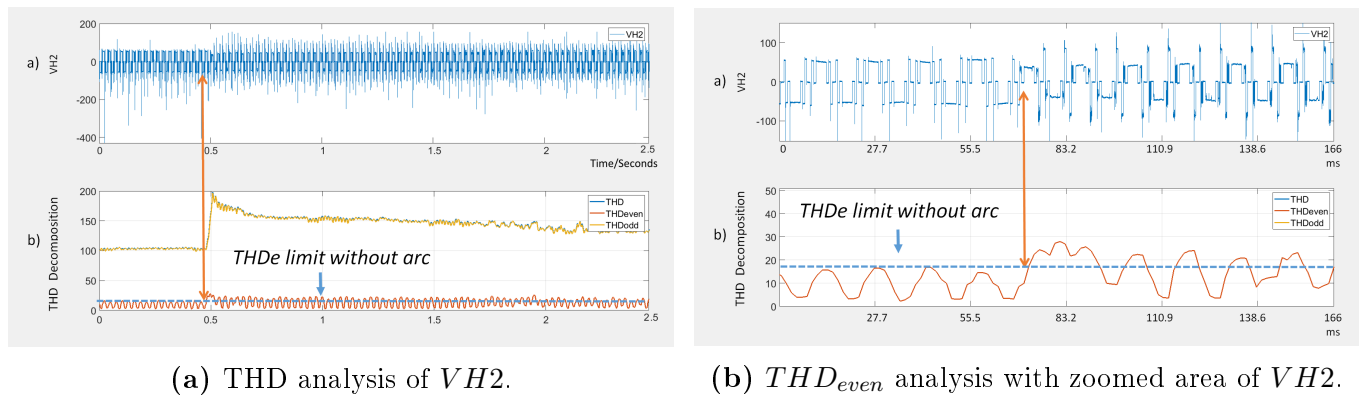
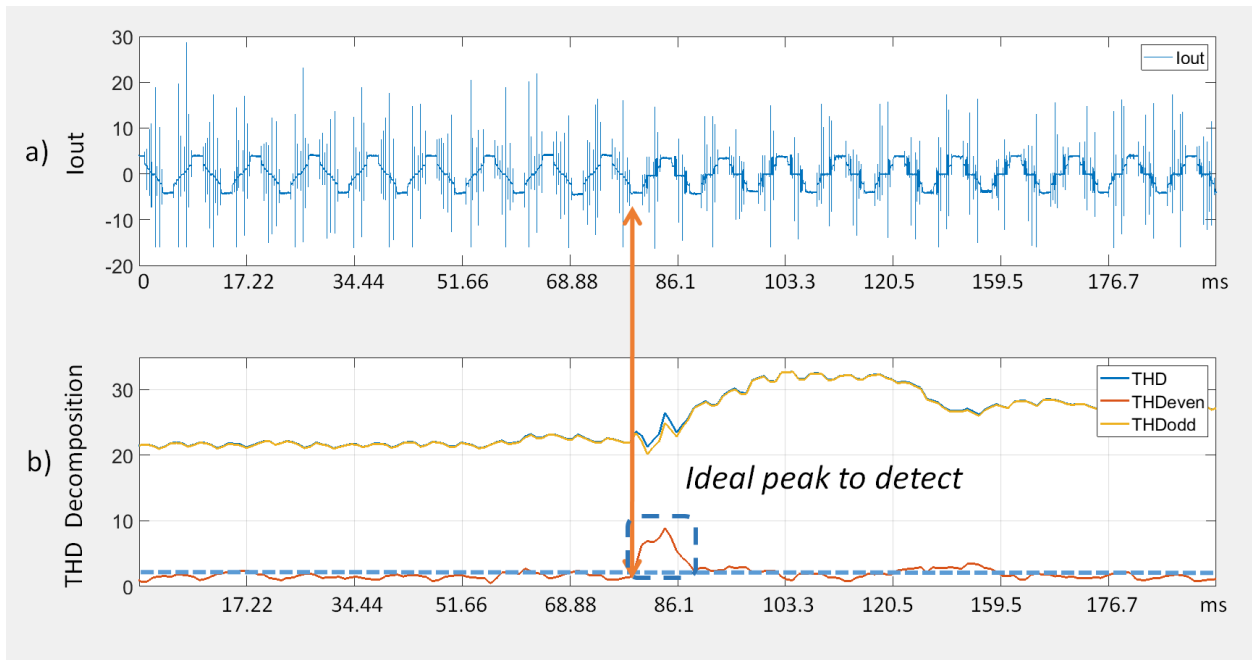


Figure 6.9. I_{out} THD analysis for hammer-drill load.

(a) THD analysis of $VH2$.(b) THD_{even} analysis with zoomed area of $VH2$.**Figure 6.10.** $VH2$ harmonics decomposition.**Figure 6.11.** I_{out} THD analysis for vacuum load.

And in the analysis of I_{out} is possible to conclude that the increase in THD_{even} only during arc ignition is clearly detectable with a peak reaching 8%, as presented in Fig. 6.11.

6.4.5 Stand alone test conclusion

With the results obtained in the analysis of experimental signal $VH2$ for the stand alone system, two important facts can be concluded. The first is that the $VH2$ signal is reliable to be used as a detection criteria by employing the THD decomposition technique. The reason behind this conclusion is that the experiments tested, as soon as the arc fault is triggered, the appearance of a perturbation in the $THDe$ is observed, even under extreme conditions with an important value of inductive load.

Thanks to precedent experiments the summary of changes in the THD, $THDeven$ and $THDodd$ for both $VH2$ and $Iout$ facing an AF is presented in Fig. 6.12. For the overall cases an increment in the $THDeven$ of approximately 13% is observed in signal $VH2$ when facing the AF. By considering $Iout$ we also noted that the average increment in $THDeven$ was only of 3% since this value is strongly affected by the load type connected to the inverter. Nonetheless, this data can eventually be used as an auxiliary criterion to achieve a better detection performance.

Signals	Without Arc	Without Arc	Without Arc	With Arc	With Arc	With Arc
THD Type	THD	THDo	THDe	THD	THDo	THDe
$Iout$ 22 Ohms + 20mH	11-14%	11-14%	2-4%	25-29%	25-29%	5-8%
$VBridge2$ 22 Ohms + 20mH	110-115%	95-110%	20-40%	150-220%	145-210%	38-65%
Criterion of 3% of increment						
$Iout$ 22 Ohms + 141mH	8%	8%	0.5-1%	8-10% Only during ignition	8-10% Only during ignition	0.5-4% Only during ignition
$VBridge2$ 22 Ohms + 141mH	110-115%	90-100%	22-40% 0.5sec during ignition	120-130%	110-115%	35-50%
Criterion of 13% of increment in THDe						
$Iout$ Hammer-Drill	24%	24%	1-2%	26-29%	26-29%	8-13% Only during ignition
$VBridge2$ Hammer-Drill	100%	100%	1-12%	165-195%	165-195%	8-35%
$Iout$ Vacuum	22%	22%	3-4%	26-34%	26-34%	9% Only during ignition
$VBridge2$ Vacuum	100%	100%	5-13%	145-200%	145-200%	10-29%

Figure 6.12. Summary of Results for AF Tests.

Another observation is that the output voltage I_{out} is unreliable to be exploited as a main detection criteria, since the THD is perturbed by the type of load that is connected to the system. Thanks to this a different alternative to improve detection will be explored and detailed in the section 6.6.

6.5 AF Influence Study in a Grid Synchronized PV System

6.5.1 Introduction

In the precedent section the tests to explore the possibility of using $VH2$ and I_{out} as detection criteria was presented. Nonetheless, in most cases the real PV installation will be interconnected to the electrical grid, which may eventually affect the detection signals employed with the THD decomposition technique. In the precedent analysis only the study of complex loads operating in a stand alone configuration was performed. This is for this reason that in this section is presented the experimental results obtained by using a grid connected system. This is achieved by studying the theory needed to achieve the grid coupling of the proposed inverter by an LCL filter. The design of the filter is validated in both simulation and experimental scenarios. Also, the version of the detection algorithm will be updated by analyzing both $VH2$ & I_{in} . In order to study a grid interconnected system under fault, the main schematic structure of an modern distribution grid integrating renewable energies sources is presented in Fig. 6.13. In this configuration the main DC sources can be an arrangement of PV panels, as well as wind turbines, or a combination both. Considering this scenario the structure will include a DC-DC conversion stage (immediately after the source), accomplishing the regulation of voltage levels required by the DC-AC converter. This regulation stage also integrates the MPPT tracking system. The DC-AC converter is coupled to the electrical grid by using a special conceived filter, the selection of both topologies used will depend of the local regulations for interconnection.

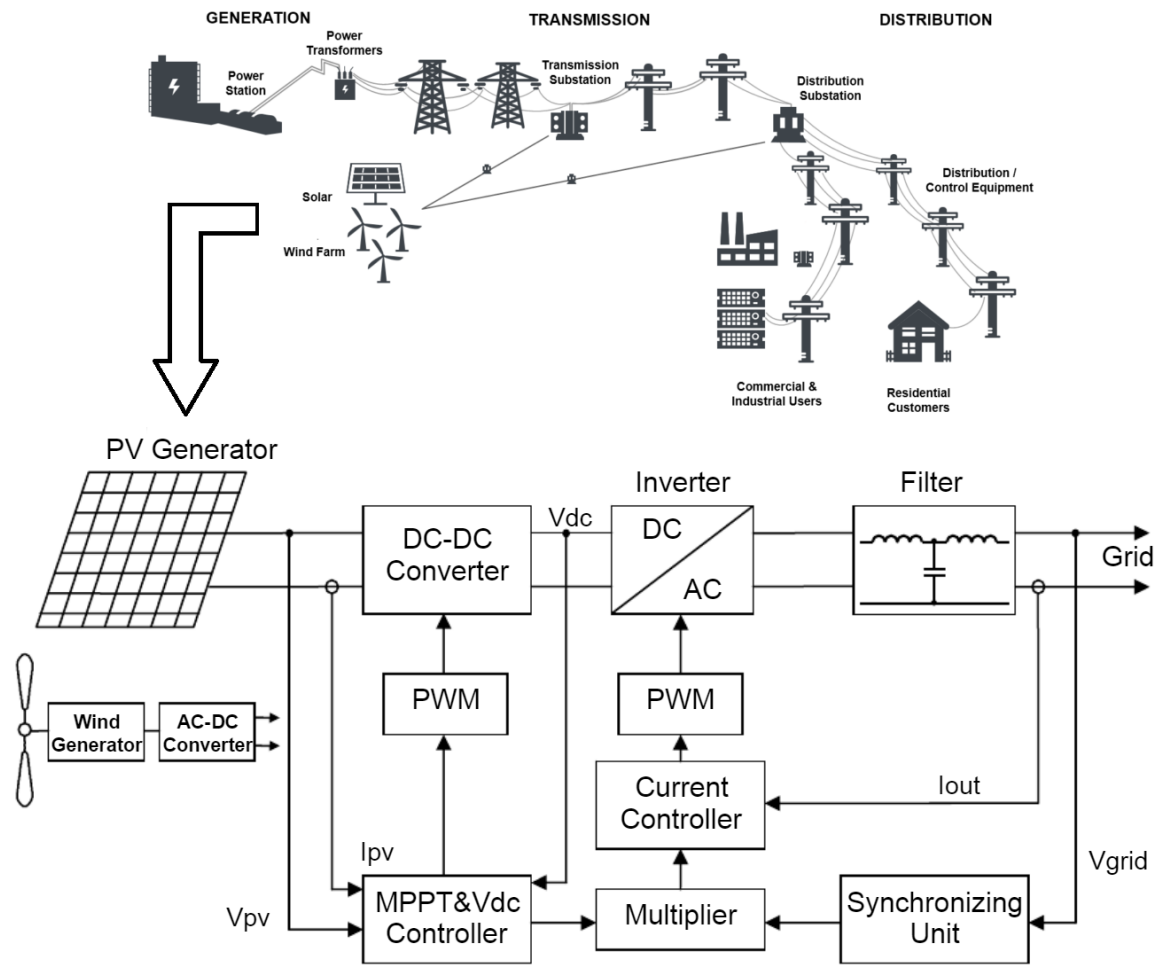


Figure 6.13. Distribution Grid arrangement.

6.5.2 Grid Interconnection Concepts and Filtering Theory

Grid Interconnection

For the smallest power outputs (under 10kW) the most used inverters are the single-phase inverters [82]. The photovoltaic plants connected to the power network must operate in maximum power output mode of the PV panels. This is achieved by using Maximum Power Point Tracking (MPPT) algorithm integrated in the inverter [83]. Usually the inverter consists of two parts [84]: a DC-DC converter with MPPT controller and a DC-AC module (inverter and filter) that produces current with a sinusoidal shape supplied to the power grid as presented in Fig 6.13.

The main directions of improving the performance of power inverters are: low harmonics in the output current, elimination of the direct current in the output, control of the active and reactive power supplied by the inverter and a digital inverter control [82]. The described converter configuration is not only used with photovoltaic panels but also with small wind turbines [85], gas or water turbines and fuel cells for auxiliary power.

In the small single-phase inverters usually control of the reactive power output is not needed. For this reason they operate with a unity power factor, which means that the current supplied to the grid is in phase with the grid voltage [84–86]. This simplifies the control and also makes the production cheaper. The detailed general schematic of a renewable energy-based generator connected to the grid through a single-phase inverter is shown on Fig. 6.13.

Since the main goal of this configuration is to transfer the produced energy to the grid, an additional factor to be considered in the analysis, is the coupling filter influence in the system and how it affects the detection technique performance.

With the addition of this filter, the nine levels multilevel output generated by the DC/AC stage will be smoothed making it suitable for interconnection. In order to achieve this transfer the inverter current must have a phase angle of less than 90° from the grid voltage. This can be accomplished when the inverter voltage phase is ahead from the grid voltage. In Fig. 6.14 is presented a simplified schematic of an H bridge inverter power unit. This inverter produces an approximative sinusoidal voltage waveform by a PWM control explained in Chapter 3. The filter at the grid terminals employs a small inductance which also determines the first harmonic of the current supplied to the grid. At low powers, the active resistance between the inverter and grid cannot be neglected. It is determined by the active resistance of the inductive coil the conductors and also by the resistances of the power bridge's transistors. In this case the output grid current is determined by the impedance \dot{Z} between the inverter and the grid and by the difference between the two voltages:

$$\dot{V}_z = \dot{V}_{inv} - \dot{V}_{grid}, \quad \dot{I}_{out} = \frac{\dot{V}_{inv} - \dot{V}_{grid}}{\dot{Z}} \quad (6.7)$$

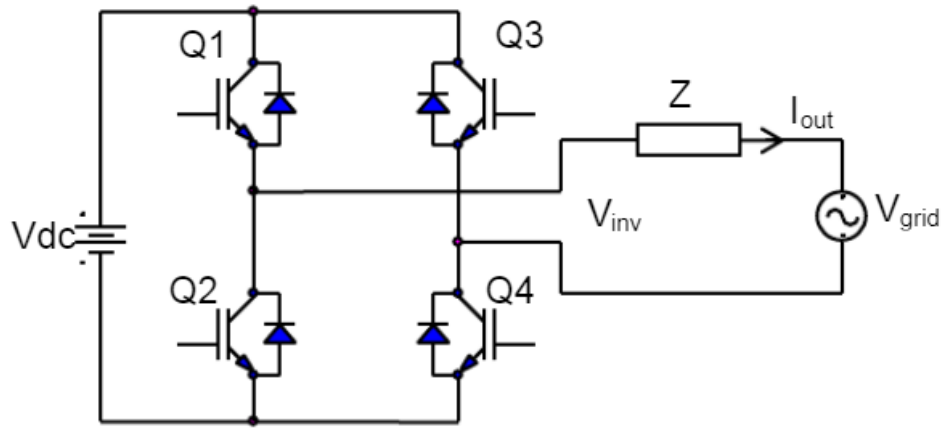


Figure 6.14. Schematic diagram of impedance between the converter and the grid.

where \dot{V}_z is the voltage drop on the impedance \dot{Z} , \dot{V}_{inv} is the RMS value of the first harmonic of the inverter's output voltage and \dot{V}_{grid} is the grid voltage. The phasor-diagram corresponding to eq. 6.7 is shown on Fig. 6.15.

In this figure, the phase angle between the current \dot{I}_{out} and the voltage \dot{V}_{grid} is less than 90 because of the active-inductive character of the impedance \dot{Z} . In real conditions $\varphi = 0$, so the current and the grid voltage are in phase. In this case the phasor-diagram is as shown of Fig. 6.15 b.

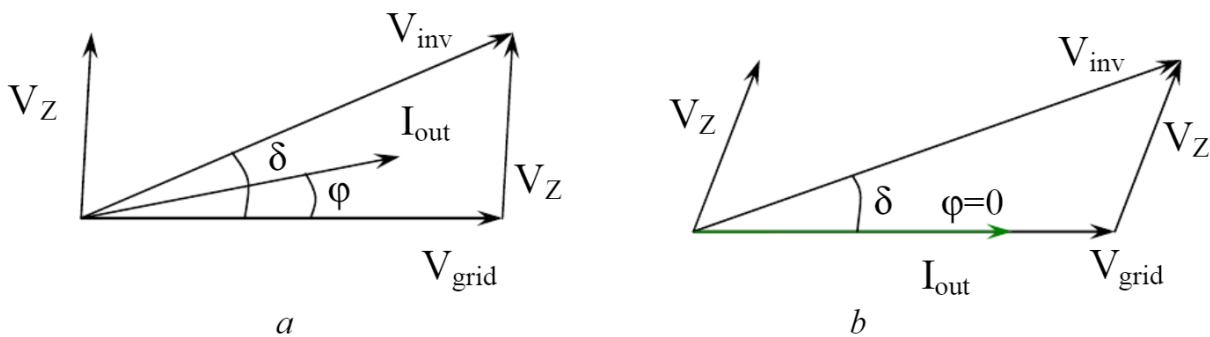


Figure 6.15. Phasor-diagram of the voltages and currents of the single-phase inverter.

In order to perform the coupling to the grid, numerous parameters have to be considered and depending of this calculation the arrangement for the coupling filter can be determined. The theory behind this calculation will be presented in the next section of this chapter.

6.5.3 Coupling LCL Filter Design Procedure

In this section is described step by step how to proceed with the calculation of each component necessary for the coupling filter. To do this, several characteristics must be considered in the design, such as current ripple, filter size and switching ripple attenuation desired. It's necessary to take into consideration that the reactive power requirements may cause a resonance of the capacitor interacting with the grid, therefore a passive or active damping must be added to the filter, this by including a resistor in series with the capacitor. In this work, passive damping is adopted, but active solutions can also be applied.

To perform the calculation of values for the filter the following parameters are needed: Line to Line RMS voltage U_n (inverter output), rated active power P_n , link voltage V_{DC} , grid frequency f_g , switching frequency f_{sw} , resonance frequency f_{res} . Thus, the filter values can be obtained in a percentage of the base values as presented in 6.8 and 6.9, this two values represents the impedance of the grid that can have an predominant inductive or capacitive.

$$Z_b = \frac{U_n^2}{P_n} \quad (6.8)$$

$$C_b = \frac{1}{(\omega_g)(Z_b)} \quad (6.9)$$

Adopting 2.7 % impedance for the converter side [87] [88], a 10 % current ripple can be obtained when using only an L filter. With additional LC part the aim is to reduce the ripple at 2 %:

$$Z_L = Z_b(2.7\%) \quad (6.10)$$

The inverter side inductance (L_i) is then: $L_i = \frac{Z_L}{\omega_g}$.

The design of the filter capacity depends from the maximal power factor variation acceptable by the grid is 5%. The filter capacitance can therefore be calculated from C_b using eq 6.11:

$$C_f = 0.05C_b \quad (6.11)$$

Considering the reduction in effectiveness caused by the chosen value of $r = 165.25\Omega$ the chosen damping resistor value of r is 1.2, the grid side inductance L_g can be calculated as: $L_g = (r)(L_i)$.

The last step in the design is the control of the resonant frequency of the filter. The resonant frequency must be higher than the grid frequency and must be minimally one half of the switching frequency, indeed the filter must have enough attenuation in the switching frequency of the converter. The resonant frequency for the LCL filter can be calculated as:

$$f_{res} = \frac{1}{2\pi} \sqrt{\frac{L_i + L_g}{L_i L_g C_f}} \quad (6.12)$$

In order to reduce oscillations and unstable states of the filter, a capacitor should be added with a resistor connected in series. This solution is sometimes called $\hat{\text{A}}\hat{\text{I}}\hat{\text{J}}$ passive damping. It is simple and reliable, but it increases the heat losses in the system and it greatly decreases the efficiency of the filter. The value of the damping resistor can be calculated as [87] [88]:

$$R_d = \frac{1}{3w_{res}C_f} \quad (6.13)$$

By substituting the parameters of *Table 4.2.2* in the equations described in this section, the values obtained for the coupling LCL filter are:

$$L_i = 18mH, L_g = 21.6mH, C_f = 3.73uF, R_f = 165.25\Omega$$

When this values are calculated, the actual connection is performed following the schematic diagram presented in Fig. 6.16.

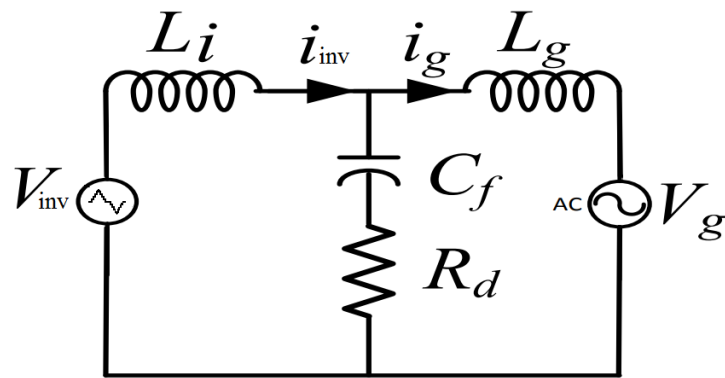


Figure 6.16. LCL coupling filter schematic.

6.5.4 Simulation results of the Designed LCL Filter

In this section the results of simulation using the proposed converter along with the designed coupling filter of section 6.5.3 are presented. Fig. 6.17 shows two signals, in blue color is presented the converters nine level voltage waveform and in magenta color the voltage waveform at the output of the designed LCL filter.

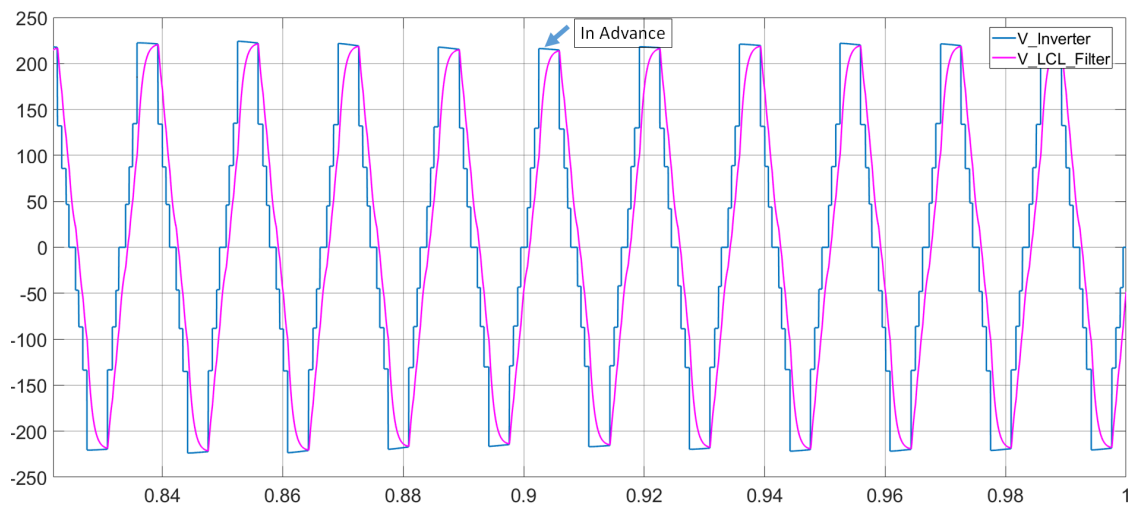


Figure 6.17. Nine level inverter voltage and LCL coupling filter smoothed voltage.

The waveform generated at the output of the filter makes it possible to conclude that the calculations and selection of values for the LCL filter are adequate for this application. With the smoothed voltage waveform. The energy generated is suitable for an synchronized power transfer.

6.6 Sliding Window Decomposition Analysis

In this section are presented the results obtained by employing a improved approach to the study of experiment signals. In order to improve the detection accuracy based in the results obtained in section 6.4.5 the algorithm will benefit from employing a more reliable signal with similar characteristics of *VBridge2*. Additionally to the monitoring of magnitude in *THDe*, the idea of using the number of peaks that surpass the normal operation *THDe* contained within a single period is explored.

The analysis of *VBridge2* remains unchanged and continue to be compared against the predefined experimental normal functioning value of *THDe*, from this data the count of exceeding peaks values is stored. This in order to perform a comparison against the actual period and the precedent, serving as a reference of the evolution in *THDe* from period to period. This process is illustrated in Fig 6.18 and 6.19.

After obtaining the *THD* content, only the first 25 harmonics components are considered, then each value of magnitude for each harmonic is separated in two groups, the pair harmonics (*THDe*) and the odd harmonics (*THDo*) depending of its position in the frequency spectrum. In this study this method of analysis is studied for signals *VH2*, *I_{out}*, *I_{in}*.

Since the detection algorithm will analyze different periodic signals in intervals of one cycle, this means that the length of the proposed analysis sliding window will also correspond to one period, and since the signals under study have a base frequency of 60 Hz the sliding window will posses a length of 16 ms. For the next series of experimental tests the length of the recorded signals *VBridge2* and *I_{in}* is increased from 2.5 sec to 10 sec allowing to generate multiple AF in a single sample.

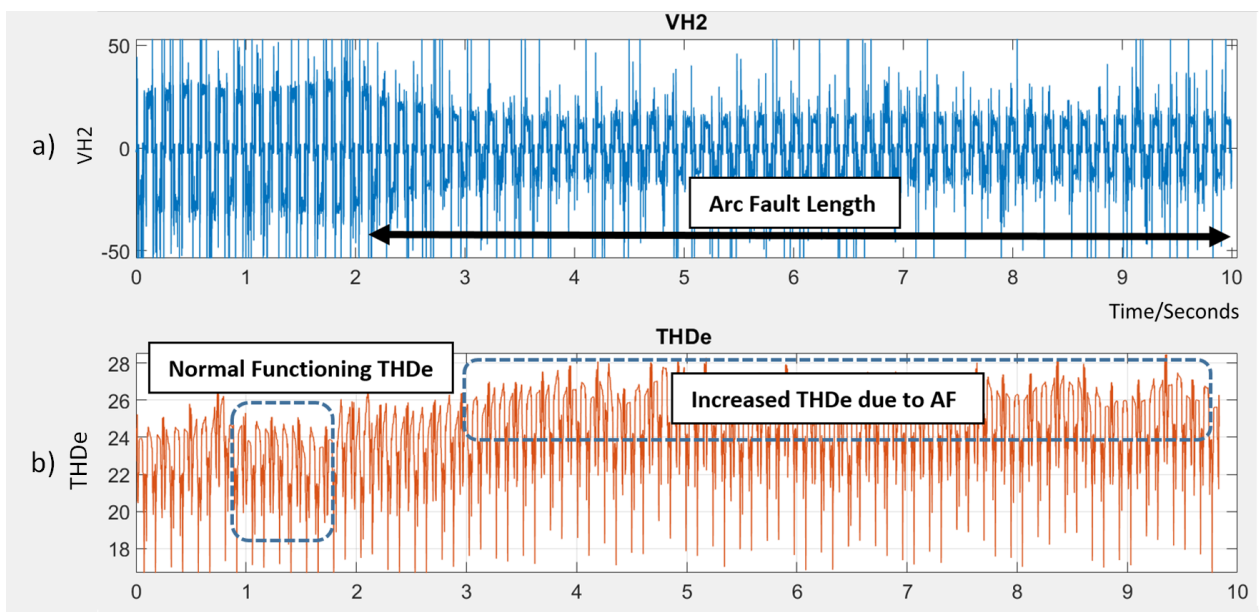


Figure 6.18. *THDe* Analysis of *VH2* before and after an AF.

A *THDe* triggering limit (presented in Fig. 6.19) was determined experimentally based on the average value recorded across the totality of experimental signals employing all the different load types and integrated into the detection algorithm. When the values of *THDe* surpass this limit threshold, the amplitude of the peak and the number of peaks in the present period is acquired. By using this data detection of the AF can be determined accurately. This is presented in Fig. 6.19, where we can observe how the concentration of peaks increases drastically when the AF appears, and continues as long as the AF is sustained. The next step in the strategy to detect AF's is to use the number of *THDe* peaks within a sliding window repeating this process until analyzing the totality of the sampled signal.

The results of employing this approach are presented in Fig. 6.20 where we can observe that once the proper conditions are met (programmed in the algorithm and explained in detail in the next section), an AF flag will be activated. This flag is presented in this series of tests as a logic value with two possible values 0 and 1 indicating the presence of an AF if the value of this flag becomes 1.

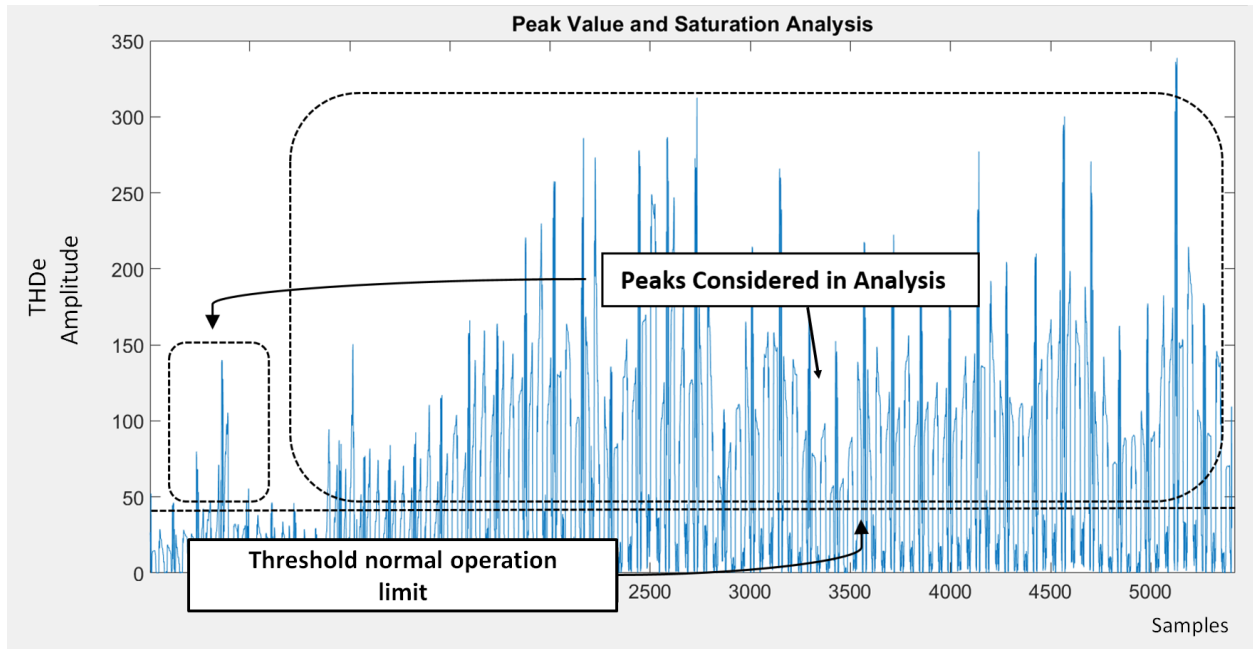


Figure 6.19. *THDe* peak saturation analysis before and after an AF.

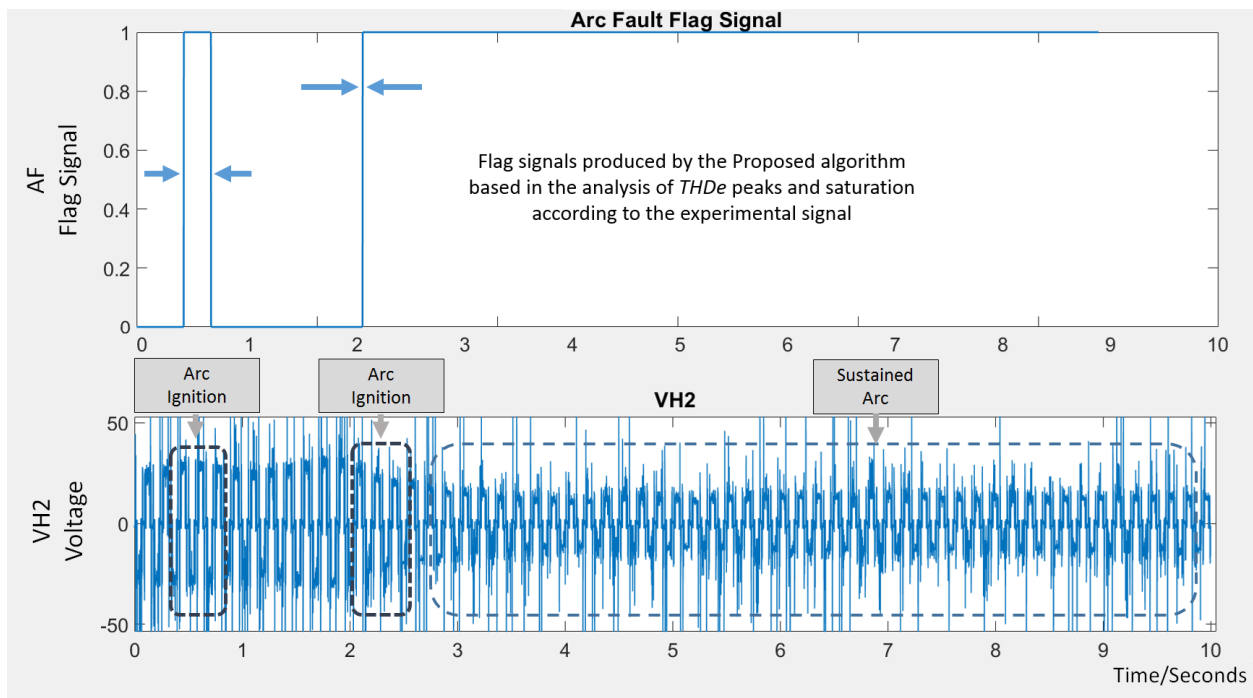


Figure 6.20. *VH2* and AF Flag output comparison.

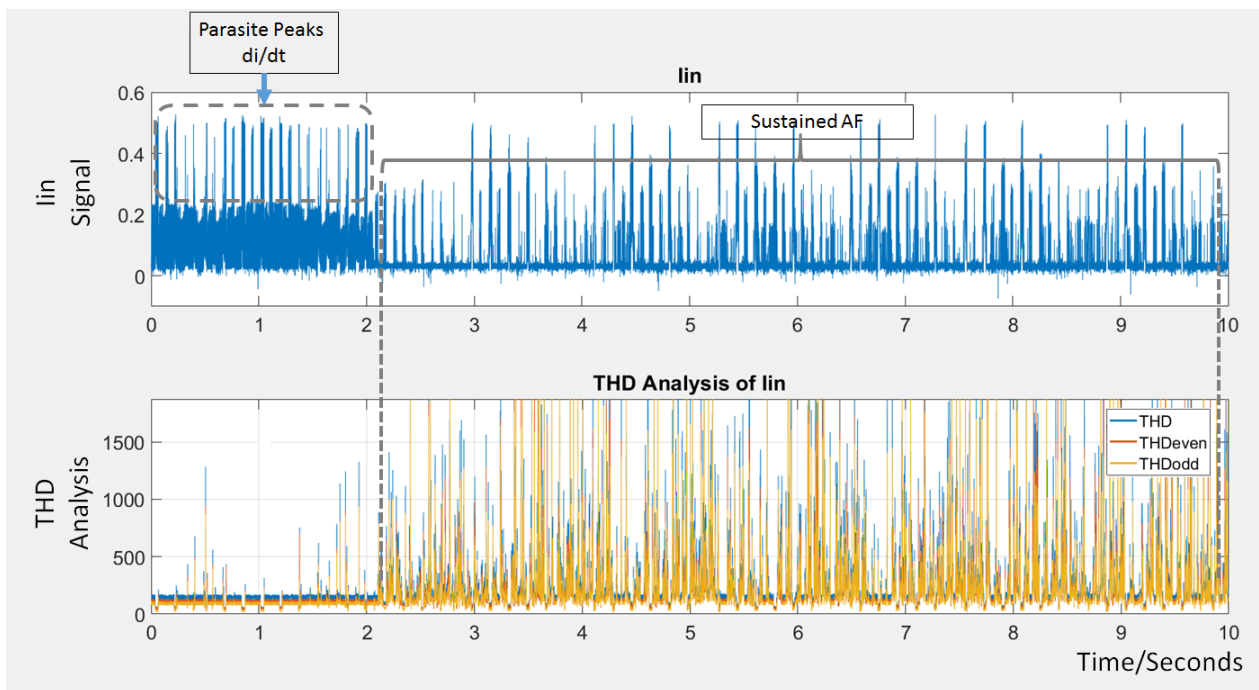


Figure 6.21. *THD* Analysis of I_{in} .

The analysis of signal I_{in} , is also included in this study which allows to evaluate its detection potential as a criteria in both type of systems (Stand alone and Grid Interconnected). The *THD* analysis as presented in Fig. 6.21 validates that the perturbations in this signal are also important when the AF occurs.

The signal treatment employed in this second section of test will validate the bases for the algorithm, that will achieve effective detection even in complex cases of AF where the fault happens for a few milliseconds generating a small amount of distortion or in multiple AF. The first results obtained show that is possible to achieve detection even in complex cases when the AF distortion happens for a few milliseconds. In the next section we consider the results for the stand alone and grid interconnected configurations.

6.7 Performance of the Proposed THD Decomposition Technique with Sliding Window

6.7.1 Introduction

With the results obtained in the stand alone system, its clear that the use of I_{out} for detection purposes is limited. In order to improve detection performance a new approach is adopted. The method explained in this section make use of a sliding window that analyses the $THDe$ of two strategic points of measure $VH2$ and I_{in} . In the experiments presented the $THDe$ of I_{in} is added to the monitoring to illustrate the changes when an AF appears.

The main structure of the detection algorithm "Sliding Window Harmonics Component Decomposition Technique" is presented in Fig. 6.22. The strategy employed by the algorithm consist of periodically analyze the harmonics content in $VH2$ and I_{in} , this operation is repeated for each cycle, defined as the period T of the 60 Hz output. Additional the data of the passed cycle N-1 is stored if the $THDe$ surpass the experimental defined normal operation value.

Its functioning consists firstly in sampling signals $VH2$ and I_{in} at a rate of 250k/s, then the fast Fourier transform is applied to extract the frequency signature of the signals. The next step is the decomposition of THD into its two THD_{even} and THD_{odd} components. This is of essential importance because the converter under normal operation will output a nine level AC output that results from the combination of $VH1$ and $VH2$. The harmonics content of the output voltage is composed exclusively by *odd* harmonics (this given the number of levels generated). When an AF is present in the system it will alter the signal symmetry hence altering harmonics, this produces THD_{even} in the system that the algorithm will detect.

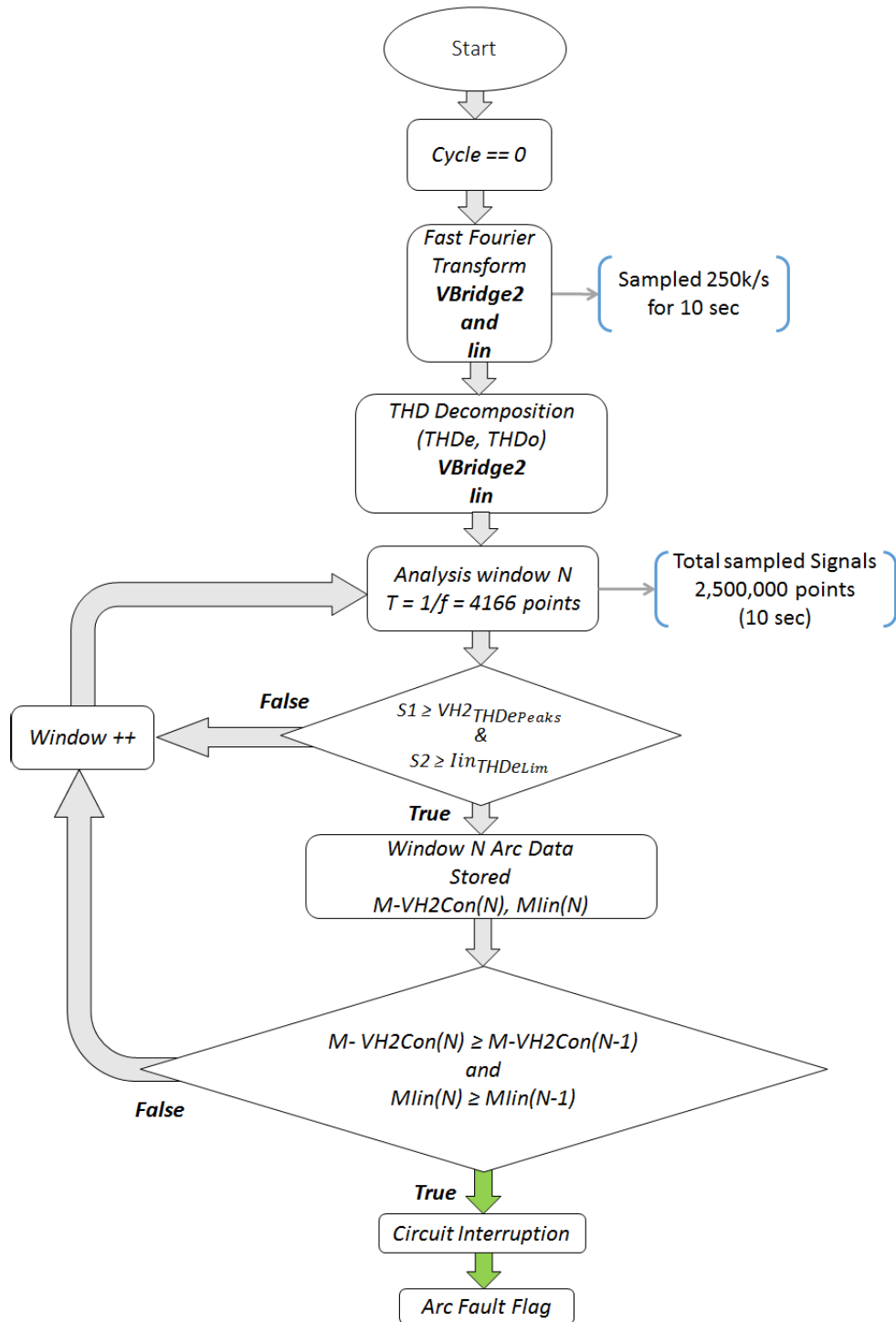


Figure 6.22. Proposed electric DC AF detection algorithm.

Before the algorithm will trigger any AF flag, two conditions have to be meet. First the magnitude value of $THDe$ in $VH2$ is studied to detect any surpass of the experimental normal operation limit ($VH2_{THDeLim}$), if this happens a counter is started to store how many peaks have surpass this threshold value ($S1$) in one cycle. With these informations the comparison of number of peaks $S1$ (hence $VH2_{THDeLim}$ surpassed) against the predefined normal operation peaks quantity value is performed ($VH2_{THDePeaks}$). Since the length of the analysis window in one single period of the 60 Hz signal, this is translated into $T = 1/60 = 4166$ sampling point, that can be expressed as 6.14 for Iin but also applicable to $VH2$.

The second condition ($S2$) to be meet is that the $THDe$ in Iin also surpass the predefined value of normal operation ($Iin_{THDeLim}$). If one of this conditions is not meet the algorithm will jump to analyze the next period of the signals ($Window++$) until it find a AF.

If both conditions are true, the data of the period (4166 samples) will be stored in variables: ($M - VH2Con(N)$) that corresponds to the number of peaks in a period. So the comparison consists in checking if cycle N has more peaks than cycle $N-1$. $MIin(N)$ satisfies equation 6.14 which corresponds to the number of samples above the limit ($Iin_{THDeLim}$). The decision stage performs a comparison sample by sample of the $THDe$ data stored within the precedent ($M - VH2Con(N-1) \& MIin(N-1)$) and present window ($M - VH2Con(N) \& M - Iin(N)$) in order to determine the presence of an AF.

$$MIin(N) = \sum_{j=1}^{4166} Iin_j > Iin_{THDeLim} \quad (6.14)$$

6.7.2 Stand Alone Isolated PV System Study

In this section are presented the final results obtained using the upgraded algorithm using Iin , in both a stand alone and an interconnected system. This results are obtained thanks to the numerous experimental signals generated in the test bench of Fig. 4.13. The processing of data from this signals is performed with the algorithm programed in Matlab.

The algorithm effectiveness is tested under different AF situation, with varied load types, the complete list of experimental signals obtained is presented in Table 6.7.1, which study the common load cases in an stand alone operation.

6.7.3 AF Detection performance in a stand alone scenario

In an stand alone configuration the converter will perform the energy transformation in order to feed the different loads, hence the detection algorithm has to be capable of achieving detection when complex loads are presented in the system.

In addition to this challenge the algorithm as to be capable of differentiate an AF from change in radiation of the PV panels and sudden switching of loads. For this reason the proposed approach rely in the processed signals of $VH2$ and I_{in} to display the AF flag.

As can be seen in Fig. 6.23 two different AF signatures are presented in order to validate the detection capabilities of the algorithm. In (a) the AF voltage is stable across the time, which generated the strongest fluctuation of distortion at the beginning of fault. Contrary in (b) the separation between electrodes wasn't constant during the fault which generates strong perturbations in the analyzed signals. This phenomena probe to be a useful factor for detection as can be seen across the different experimentations performed.

6.7.4 Detection Results for Stand Alone and Grid Connected Systems

In this chapter the experimental results of both configurations (stand alone and interconnected systems) are tested by implementing the detection algorithm presented in this section. In Fig. 6.23 three signals are displayed: AF Flag, Experimental AF Voltage and the THD ($THDe, THDo$) decomposition signatures of I_{in} . The first signal represents the resulting AF flag generated by the proposed detection algorithm presented in Fig. 6.22. This flag helps with the interpretation of results.

The second signal presented, is the measured experimental AF voltage and as mentioned before, is a fundamental signal that helps to accurately evaluate the response of the algorithm. Finally the third signal presented is the frequency signature of I_{in} , this signal is presented in each figure in order to visualize the changes in THD when the AF appears.

The summary of the different test performed for the evaluation of the algorithm is presented in Table 6.7.1. The table includes the main characteristics of the experiment such as, type of load employed followed by the number of AF tests. A total of 55 tests are performed in this section.

TABLE 6.7.1. AF Algorithm testing with different loads.

<i>Loads & Number of AF tested</i>	<i>Value of Load</i>
<i>Resistance – 5</i>	<i>47Ω</i>
<i>Resistance – 5</i>	<i>22Ω</i>
<i>Resistive 47Ω Inductive – 5 each = 15</i>	<i>5mH, 30mH, 58mH</i>
<i>Resistive 22Ω Inductive – 5 each = 15</i>	<i>5mH, 30mH, 58mH</i>
<i>Resistive 22Ω + 1200W Vacuum – 5</i>	<i>Fast speed</i>
<i>Resistive 22Ω + 1200W Vacuum – 5</i>	<i>Slow speed</i>
<i>LCL Couplin Filter 5</i>	
<i>Total – 55</i>	

Resistive Load AF scenario

In order to test the detection capabilities of the algorithm using I_{in} . The first results using resistive loads of 22Ω and 47Ω are presented below. In Figs. 6.23 and 6.24 we observe two different cases of AF. In 6.23 the AF is generated with a small spacing distance between electrodes (noted 'short'). Which will produce an overall constant AF that generates relatively low noise across the frequency spectrum as can be confirmed in I_{in} THD signature. This short distance AF will have a voltage of approximately 35 V.

In Fig. 6.24 the gap between electrodes is increased (noted 'long') to a distance where the AF is still stable, this gap change will cause a strong variations in the AF voltage, hence increase the noise generated. This long gap AF will have an average voltage of around 55 V.

When the AF starts, a peak in the THD of I_{in} also is triggered, this phenomena repeats across the tests presented in this section. This disturbance is employed in the detection algorithm instead of I_{out} signal, since its not affected by the type of load feed as well as $VH2$. By using both $VH2$ and I_{in} the algorithm generates the AF flag correctly for both cases.

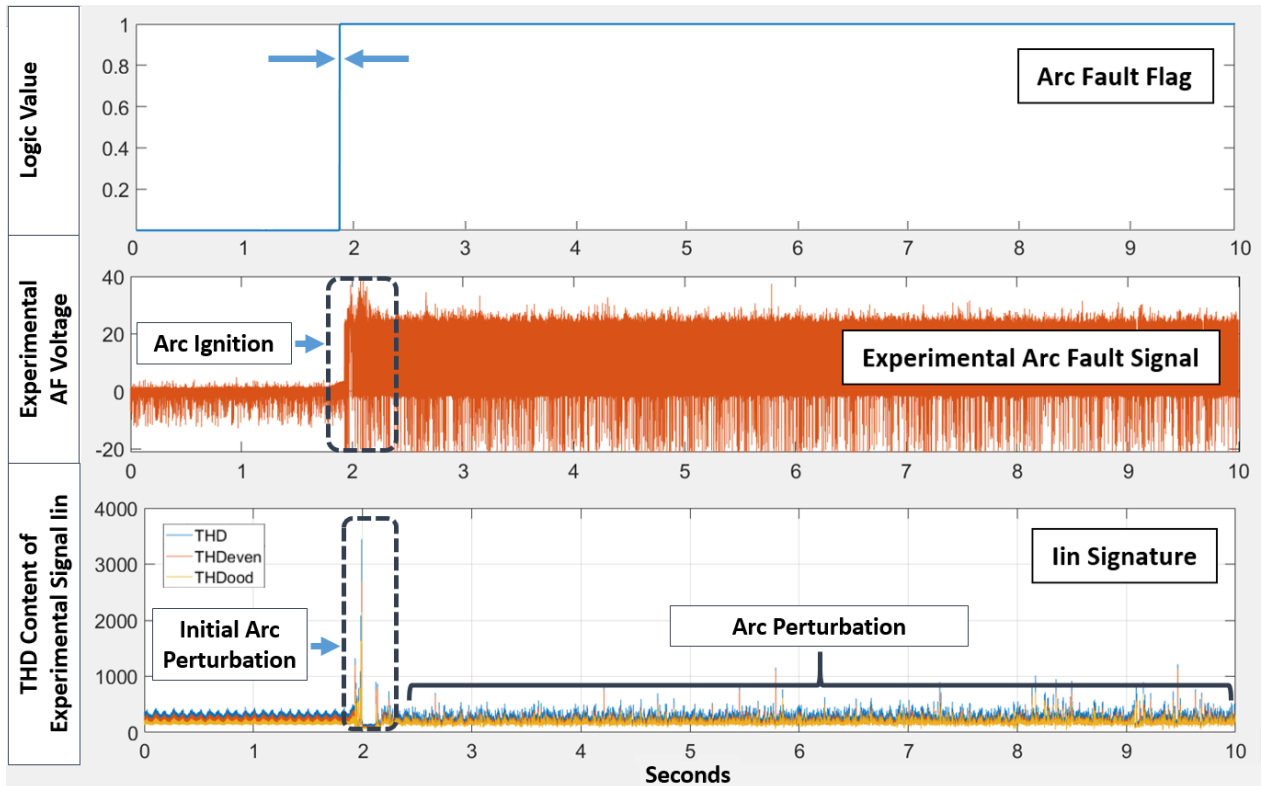


Figure 6.23. Single AF with a 22Ω load, constant electrodes spacing, detection algorithm result.

In Figs. 6.25 and 6.26 the AF is generated using the two distance gaps between electrodes as mentioned above, the same protocol is adopted for the following tests. This aim to study the response in more challenging situations for the detection algorithm.

For the study of signals presented the algorithm is configure to stop the AF flag when the AF disappear, in a real application scenario a circuit break will be triggered when the first AF flag is activated so further AF will not be able to detect since the system will stop functioning.

The AF flag appears at the instant the fault appears in the system. Nevertheless, in both cases it should be noted that only resistors that constitute the simplest of loads employed.

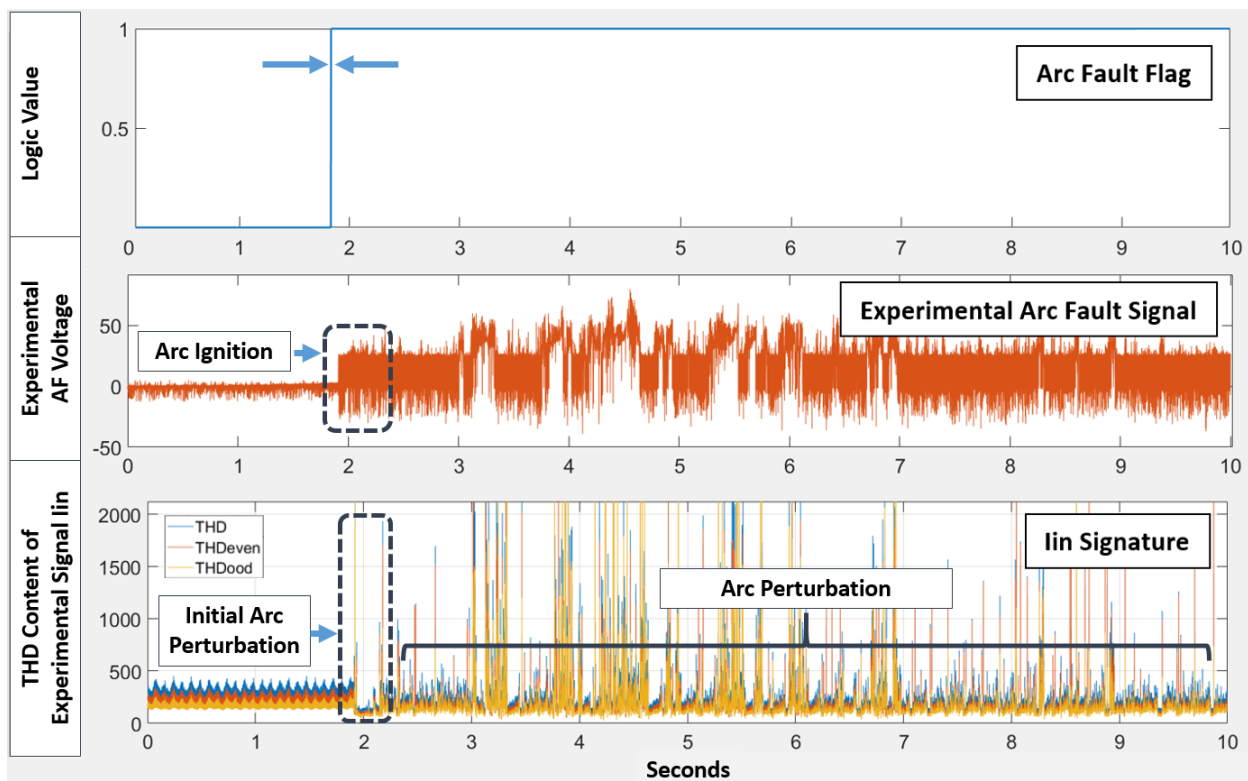


Figure 6.24. Single AF with a 22Ω load, variable electrodes spacing, detection algorithm result.

In the next test the algorithm capabilities will be analyzed with a various values of RL load.

Resistive-Inductive Load AF scenario

The detection algorithm is tested with a resistive-inductive load as presented in Fig. 6.27, 6.28, 6.29, 6.30, 6.31 and 6.32. The results of Fig. 6.27 and 6.28 are generated with a constant distance between electrodes. As a result the noise level generated by the fault is less important compared to the rest of tests for this type of load. In this results is observed that I_{in} increase hence the perturbation the AF generated.

In this case the algorithm is capable to perform detection accurately by using both signatures $VH2$ and I_{in} . Nonetheless it can be seen that the AF flag suffers a small delay at the end of some cases, this is due to the fact that the I_{in} signature takes a approximately 10 ms to regain its periodic waveform when the AF disappears from the system. This delay will be

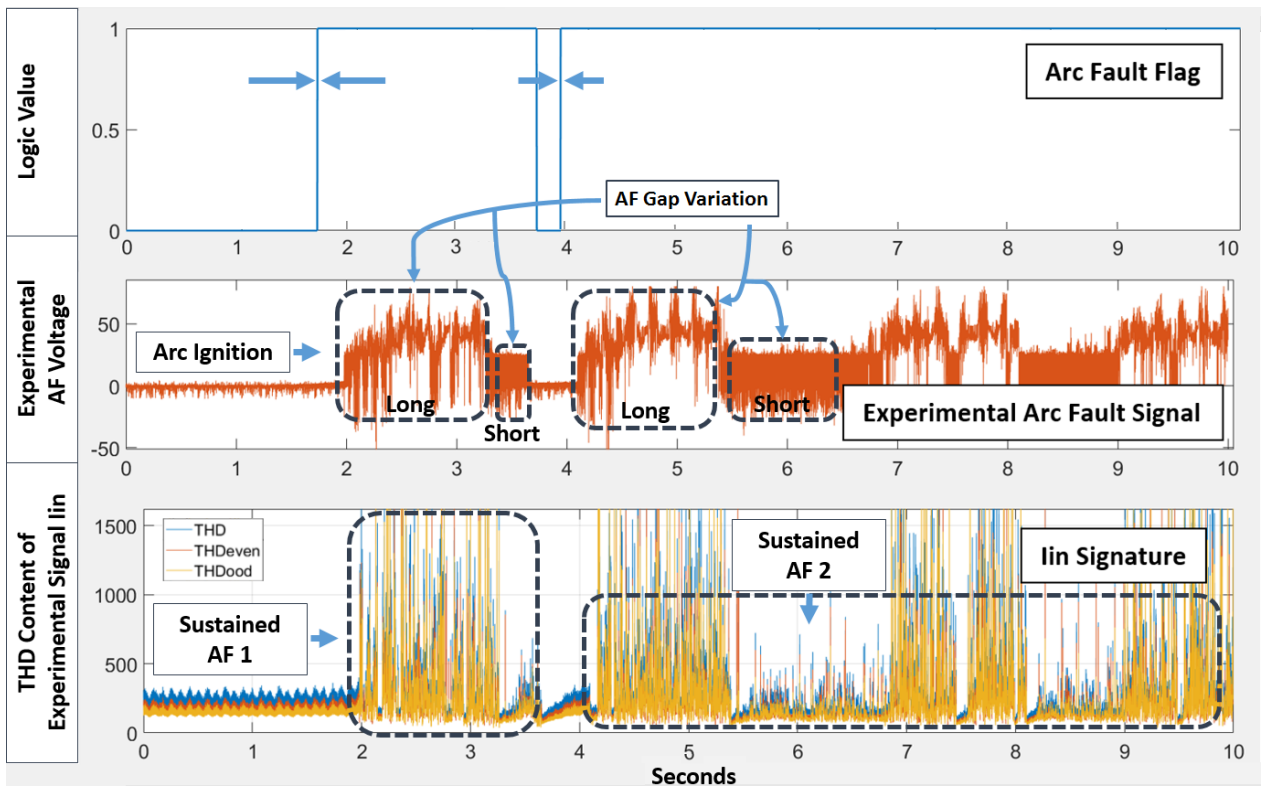


Figure 6.25. Multiple AF scenario with a 47Ω load.

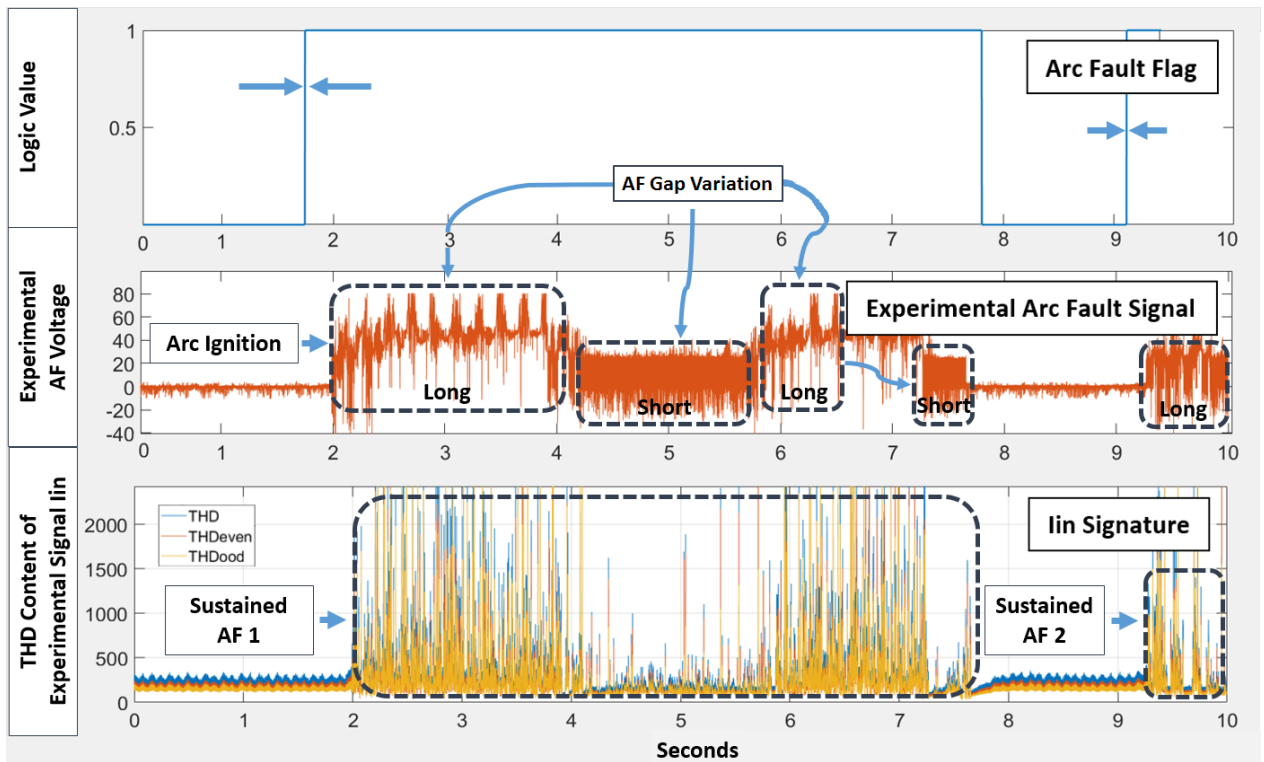


Figure 6.26. Multiple AF scenario with a 47Ω load.

extended if the inductive value increase, because the distortion will be greater hence the time for the signal to recover its original waveform as observed in cases of 31 mH and 51mH.

In Fig. 6.29 and 6.30 the inductive value of 31mH is employed, this will modify considerably the output signal generated by the converter and also increase the distortion levels when an AF appears. Nonetheless the algorithm still detect even with multiple AF as presented in Fig. 6.29 and 6.30.

In order to test the algorithm in a extreme condition the value of inductance is elevated to 51mH. In this case the output signal of the converter is completely sinusoidal and even under this circumstances the detection algorithm achieves detection accurately as can be seen in Fig. 6.31 and 6.32. Until this point it can be concluded that both signals $VH2$ and I_{in} are reliable signals to perform AF detection.

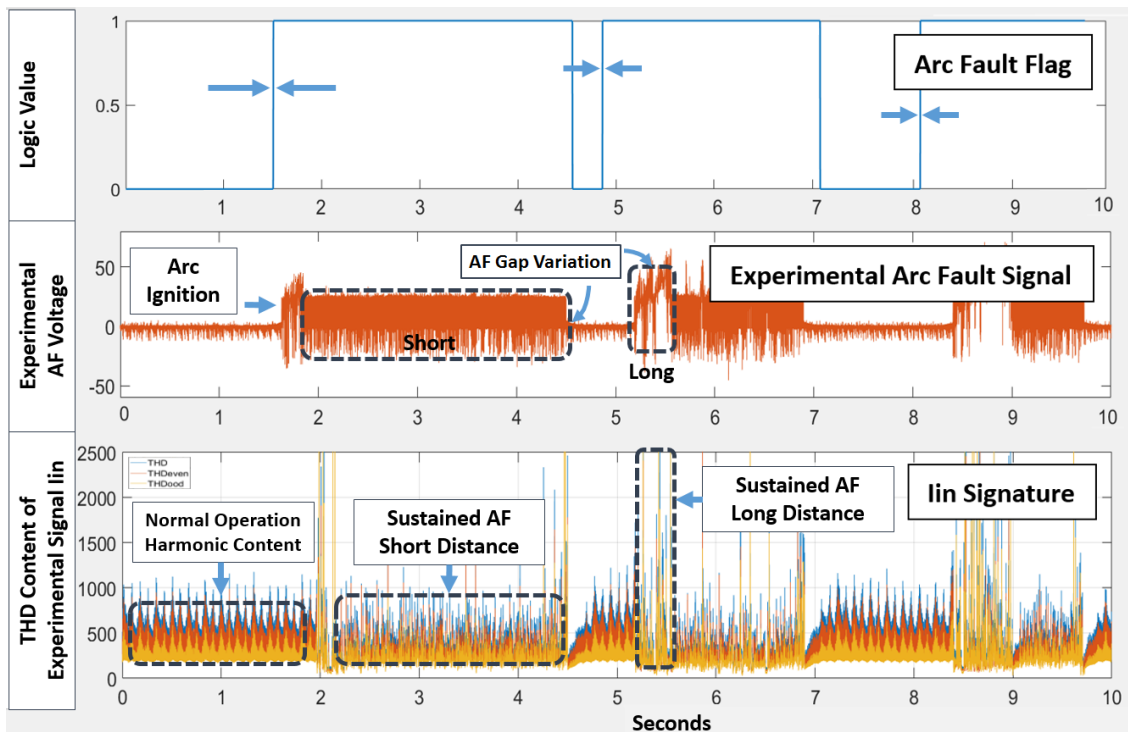


Figure 6.27. Test 1 with RL of 22Ω and $5mH$ load.

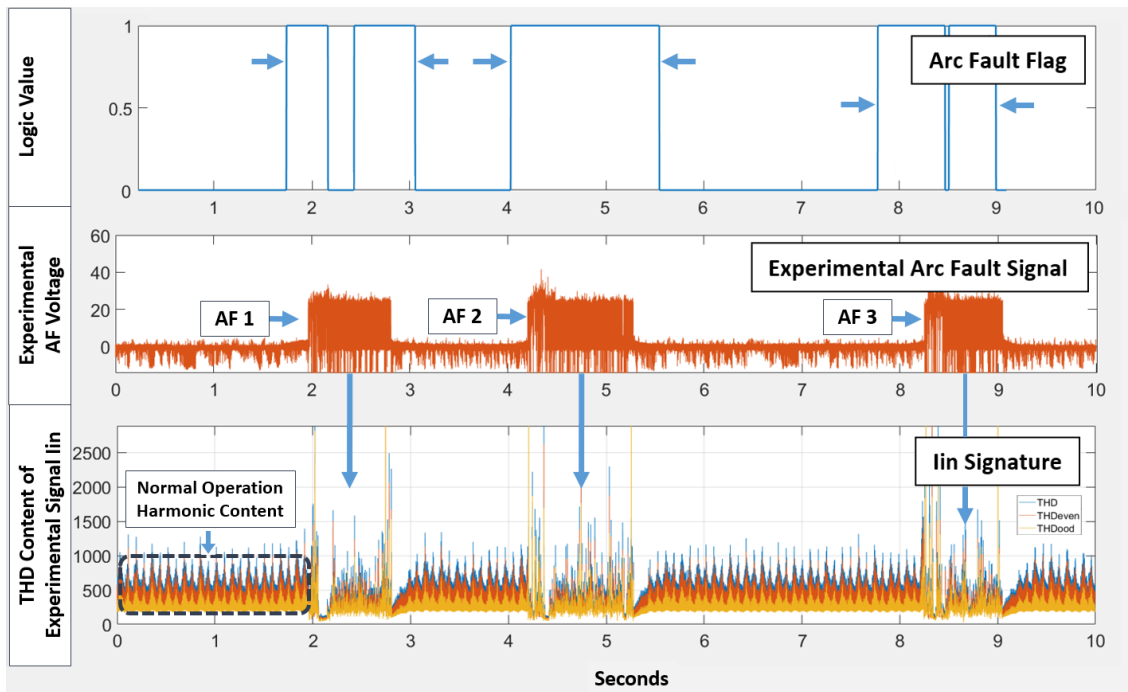


Figure 6.28. Test 2 with RL of 22Ω and $5mH$ load.

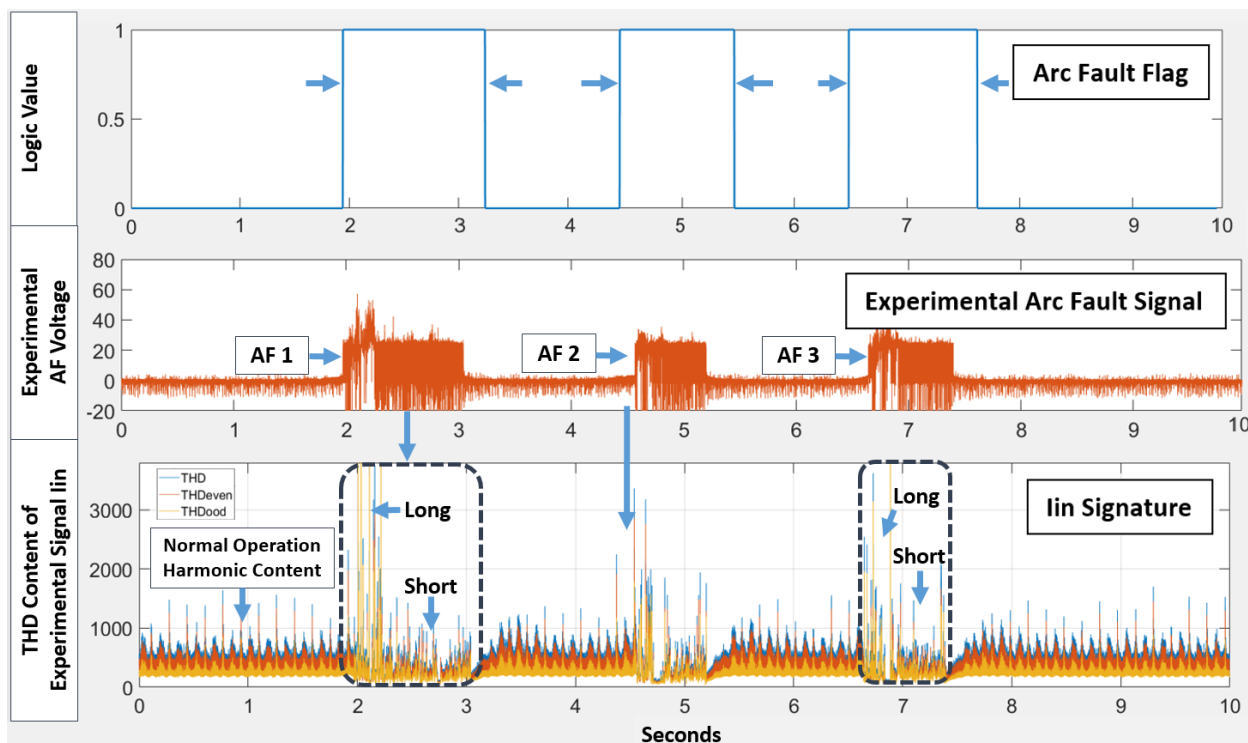


Figure 6.29. Test 3 with RL of 22Ω and $31mH$ load.

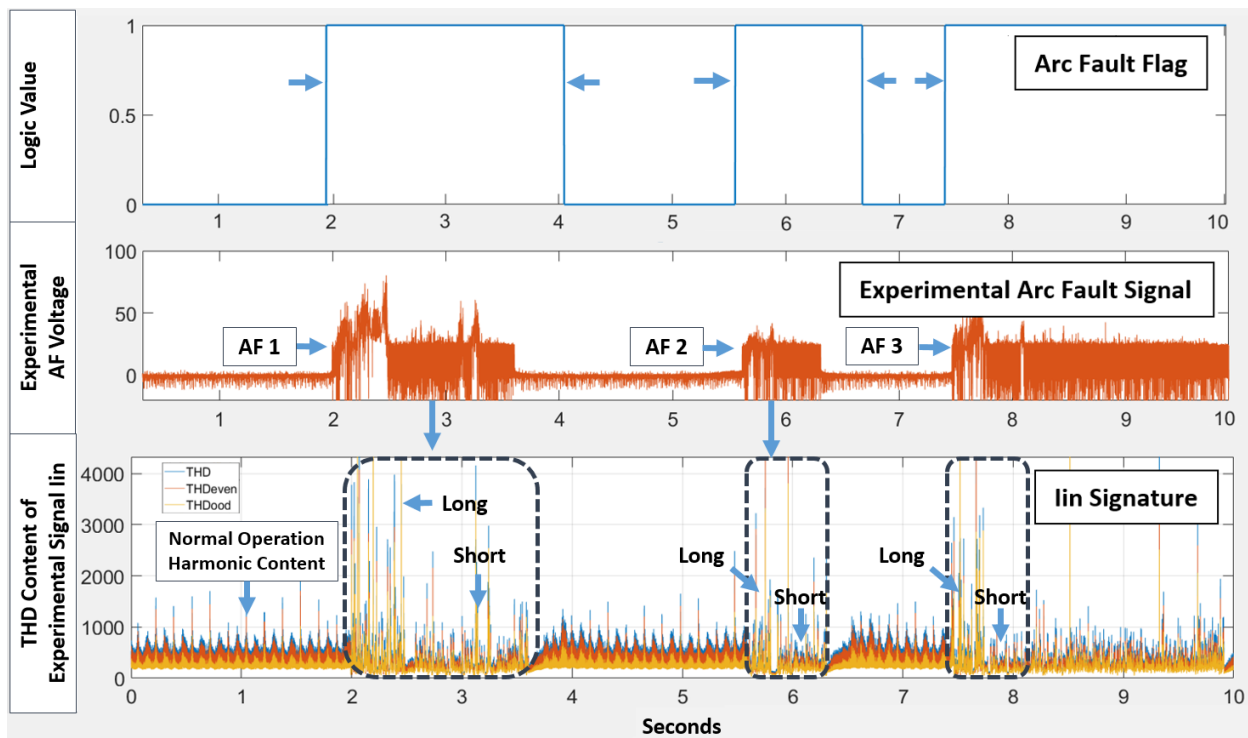


Figure 6.30. Test 4 with RL of 22Ω and $31mH$ load.

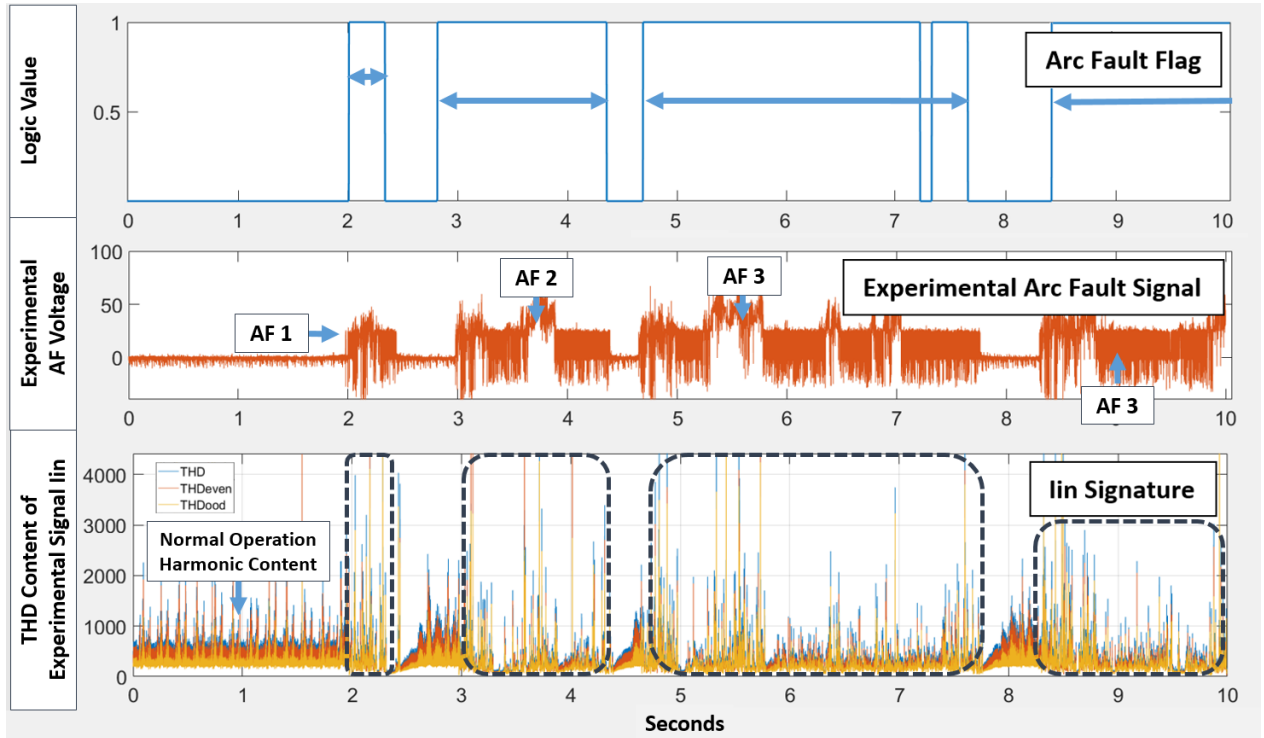


Figure 6.31. Test 5 with RL of 22Ω and $51mH$ load.

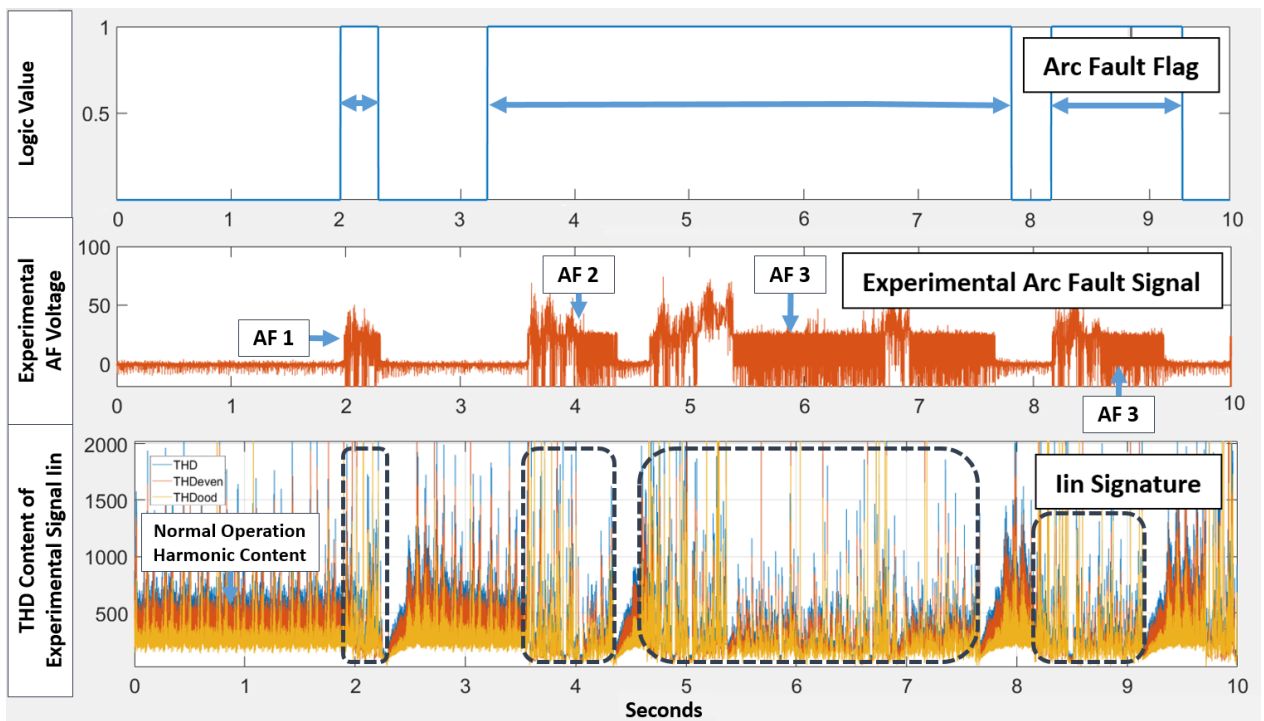


Figure 6.32. Test 6 with RL of 22Ω and $51mH$ load.

AF scenario Vacuum Cleaner

In a stand alone operation the system will also need to perform detection while feeding complex loads such as motors. For this reason the algorithm is tested with a 1200 W vacuum cleaner, the results are presented in Fig. 6.33 - 6.35. In Fig. 6.33 the algorithm manages to detect.

When using a vacuum cleaner as load a peculiar effect is produced, when the AF is present the vacuum cleaner start and stops repeatedly during the AF. This explains why the small and repeatedly AF flags across Fig. 6.33 - Fig. 6.35. As can be seen in this challenging case of detection, the algorithm based in $VH2$ and I_{in} performs detection successfully.

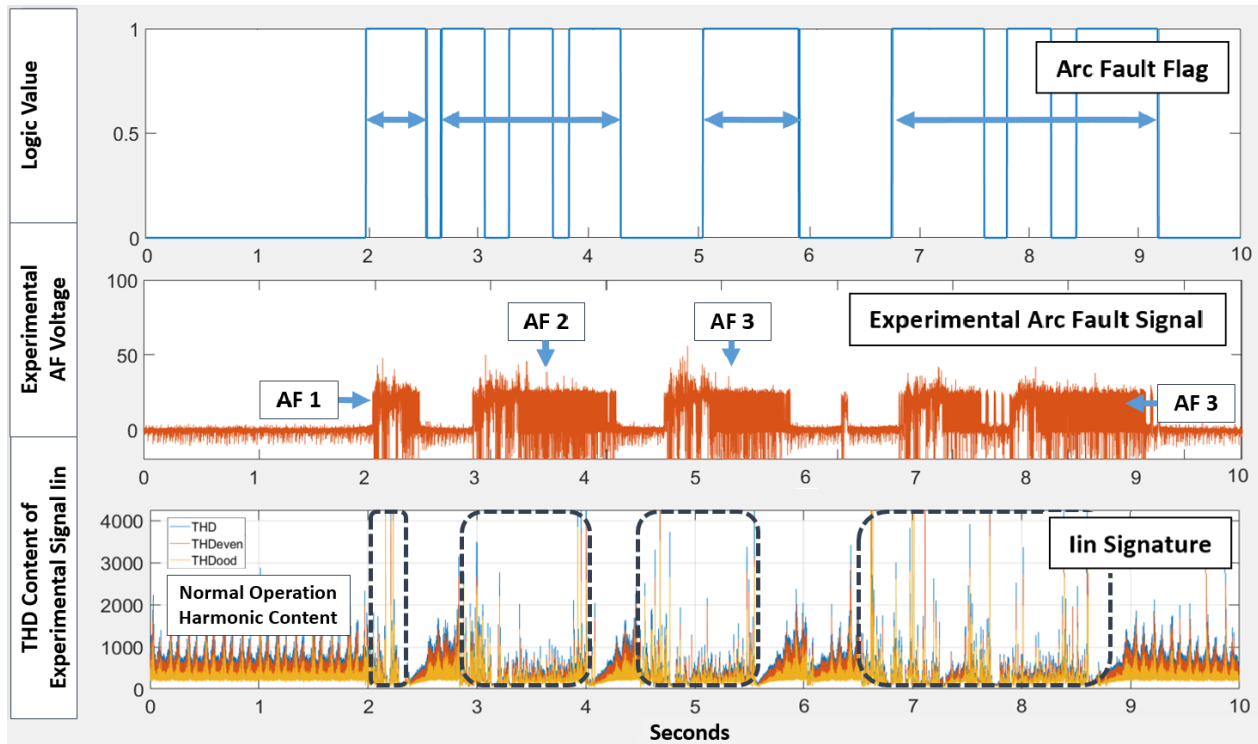


Figure 6.33. Test 1 algorithm results, 1200 W vacuum load.

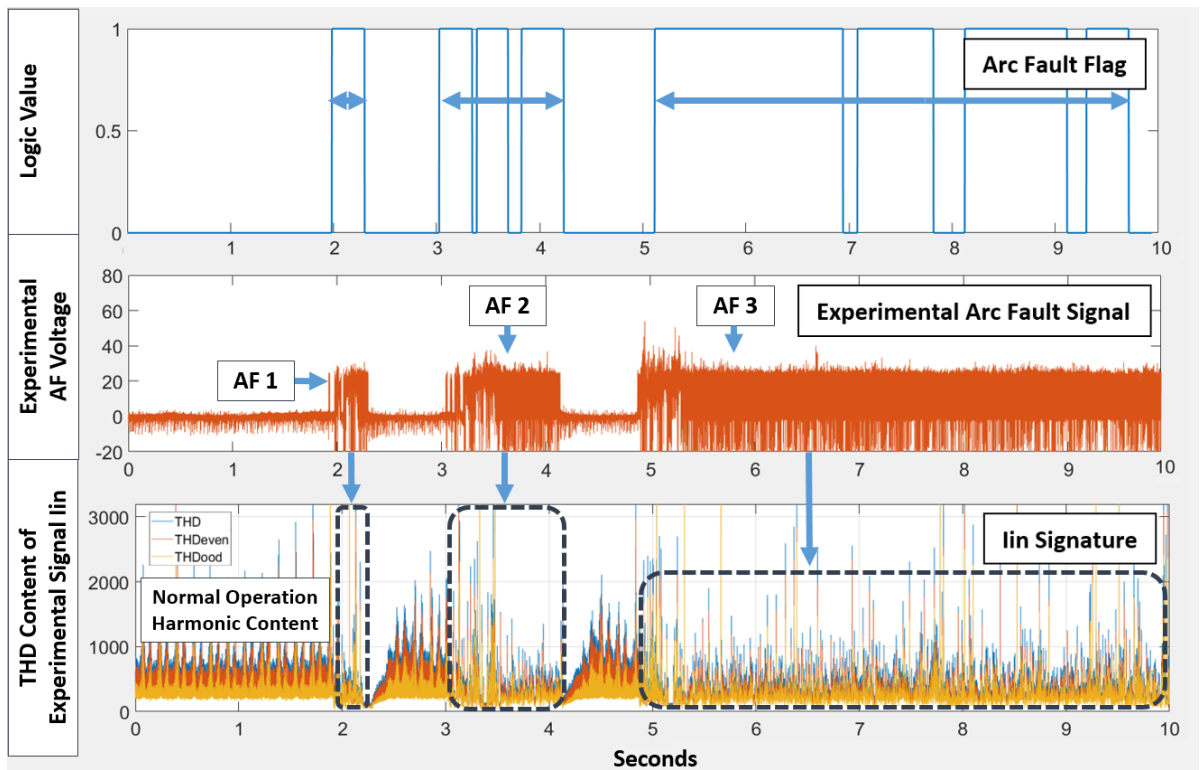


Figure 6.34. Test 2 algorithm results, 1200 W vacuum load.

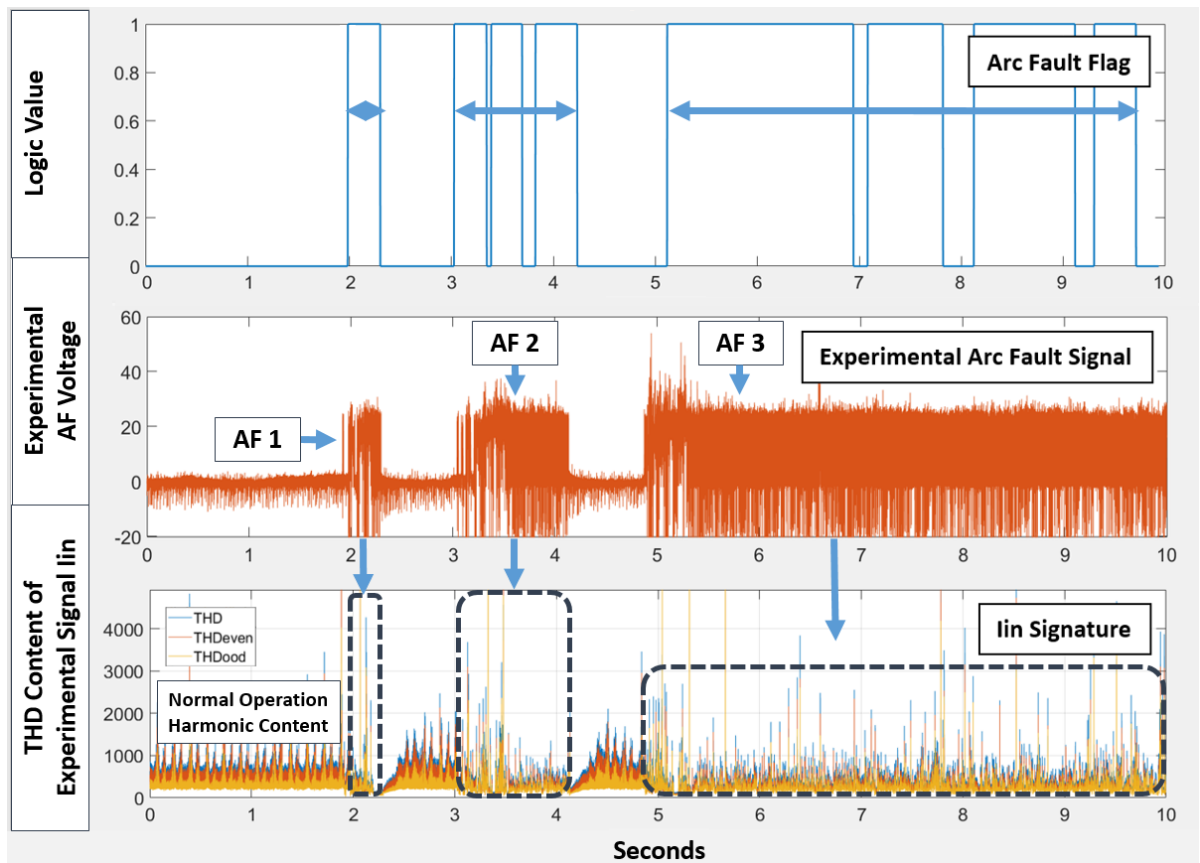


Figure 6.35. Test 3 for Vacuum cleaner of 1200W.

6.7.5 Resistive variation Load AF scenario

Another case, that is tested is the resistive real time load switching. In this test, in the first time a instant change of load is performed in order to evaluate the algorithm capability of distinguish between the switching of loads and a real AF. In a second time after the load switching a real AF is produced.

The case presented in Fig. 6.36 shows the change in the load value. This doesn't alter the harmonic signature of the signals analyzed by the algorithm as can be seen in the 'Load Switched' highlighted. We observe a small increase in I_{in} due to the switching of loads, then the algorithm detects only the real AF.

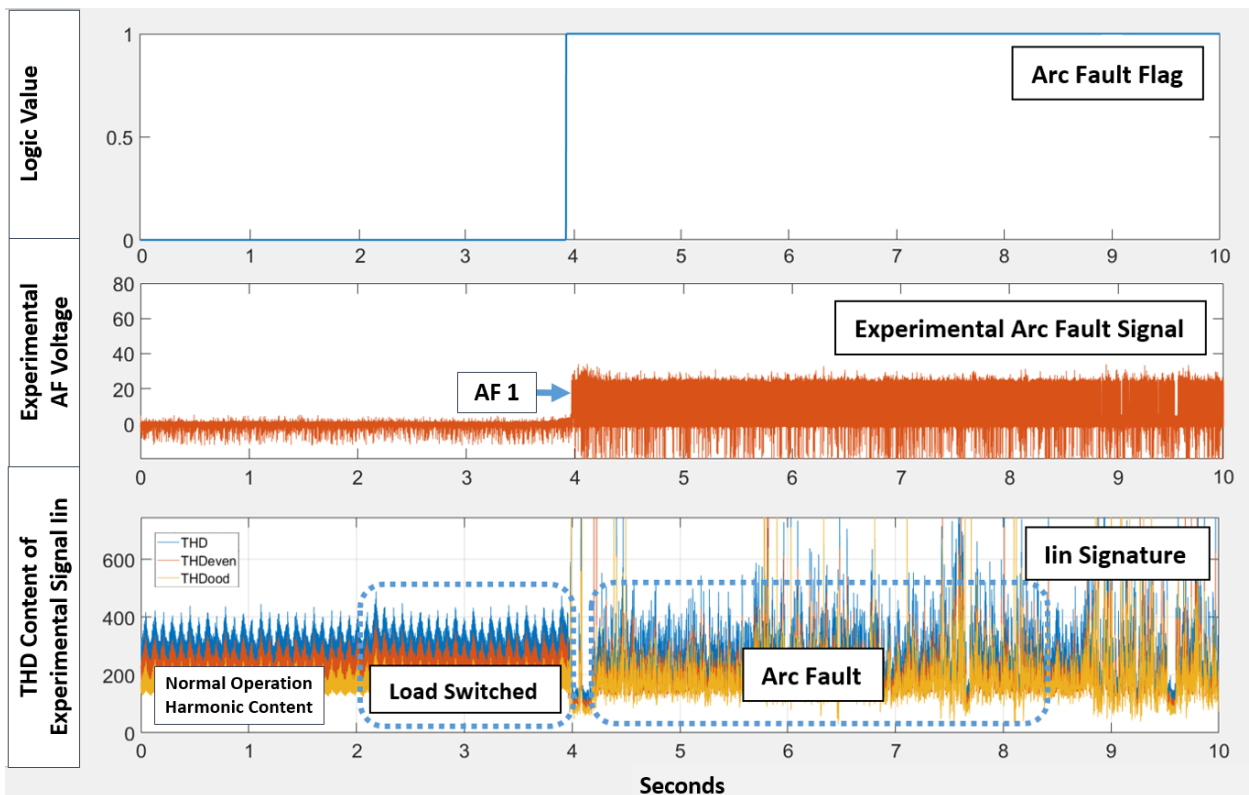


Figure 6.36. AF test side by side with a resistive switched load and its effect in the THD content.

The results presented in this section, validates this detection method across numerous cases of AF in a stand-alone system perform accurate detection without major problems. These results also validate the robustness to sudden load changes as well as to disturbances generated by universal motor loads.

6.7.6 Grid Synchronized PV System Study

In this section will be presented and discussed the result obtained in an experimental scenario by generating an AF in the system, using the calculated coupling filter detailed in section 6.5.3.

LCL Coupling filter AF

For the evaluation of detection performance of the algorithm in an interconnected scenario, the results obtained in Figs. 6.37, 6.38, 6.39 and 6.40 are studied. In this four different AF signatures presented the algorithm is able to correctly detect the apparition of the fault and generate the AF flag. Its necessary to be noted that the apparition of the flag is delayed between 15 and 40 ms. These presence of a delay is similar to the delays encountered in the case of an RL load.

The response of the algorithm can be increased with a modification of the sliding window. Such change can potentially affect the performance for other types of loads, this action can be adopted only in the case of a single well known load.

The AF flag correctly indicate the apparition of the AF in the four cases implemented and presented in this section despite the change in the signals due to the additional filter. These results validate the functioning of the proposed detection approach also in a system interconnected with the electrical grid.

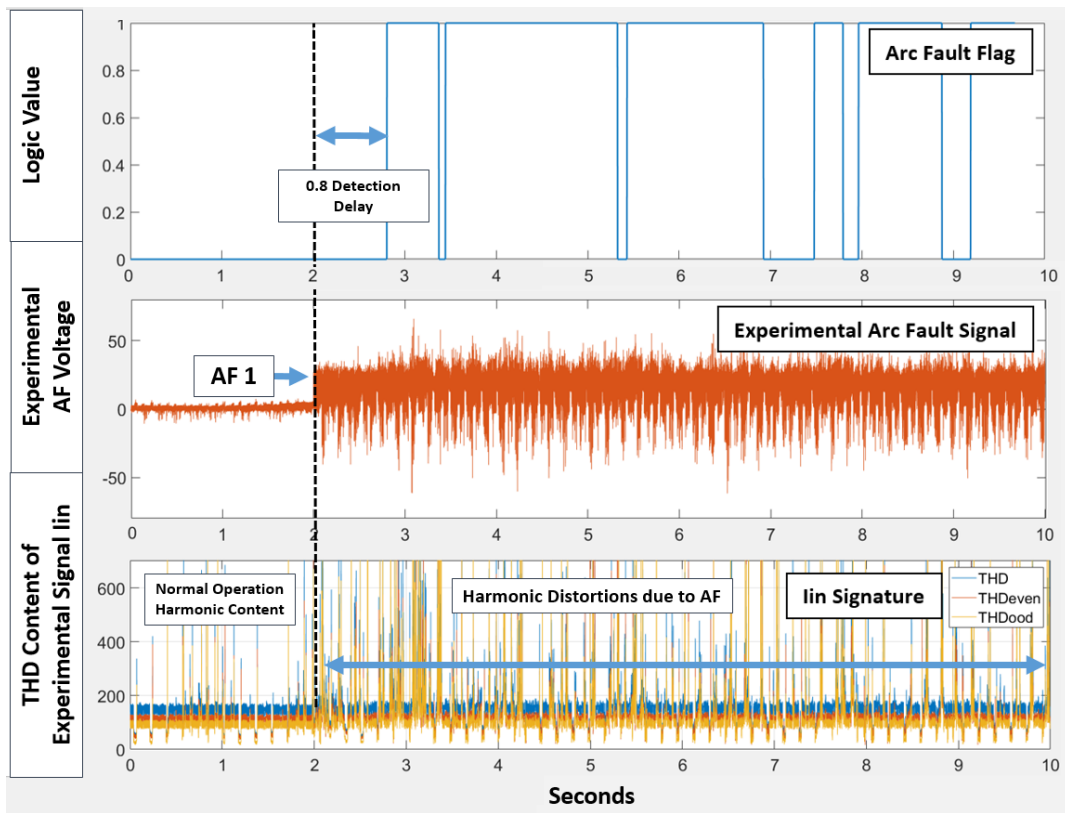


Figure 6.37. AF test 1 with coupling LCL filter.

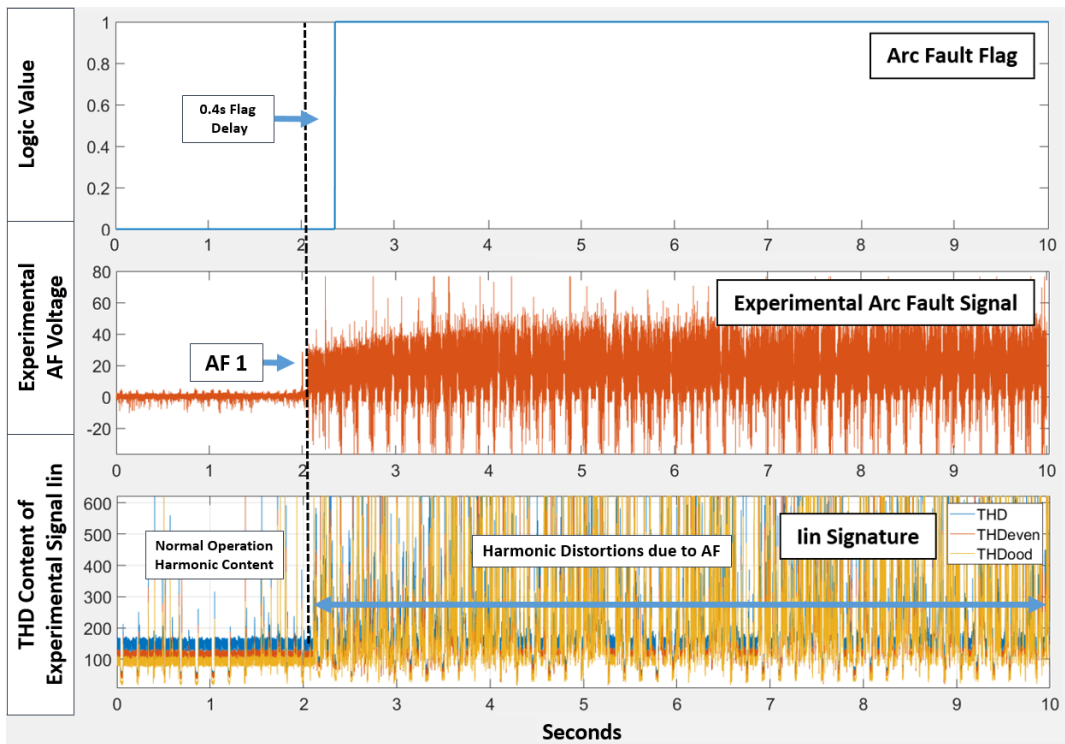


Figure 6.38. AF test 2 with coupling LCL filter.

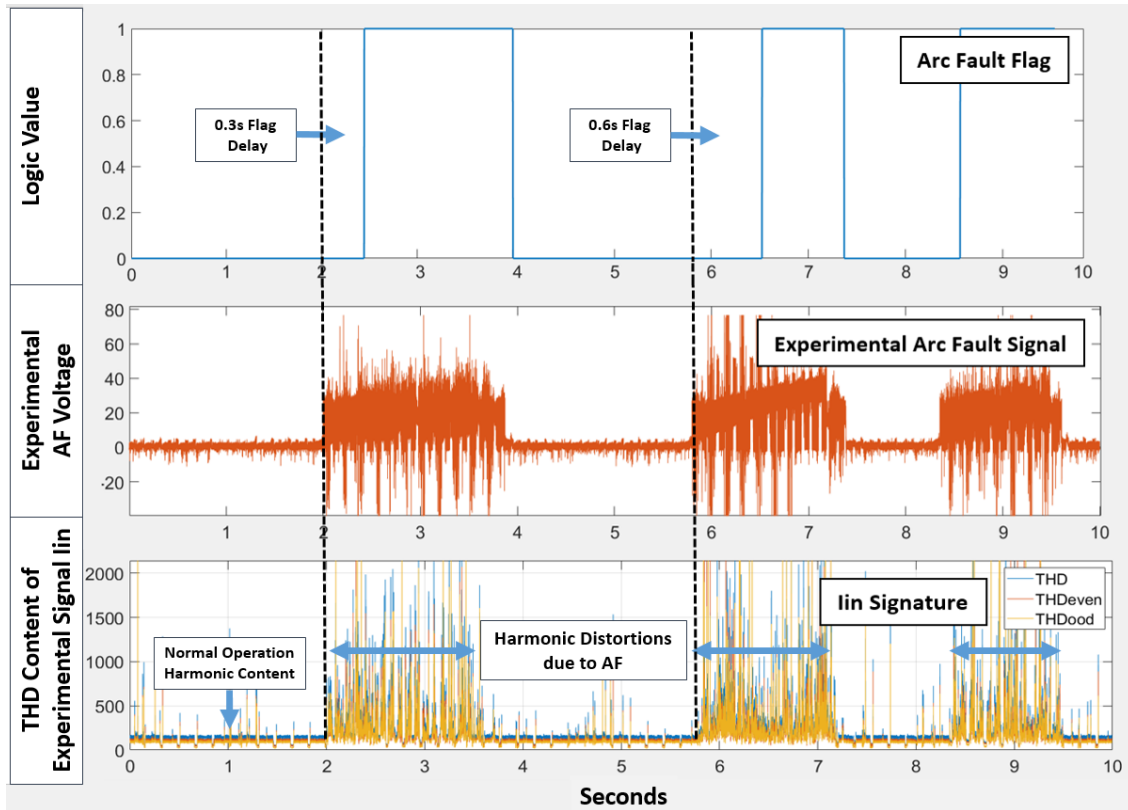


Figure 6.39. AF test 3 with coupling LCL filter.

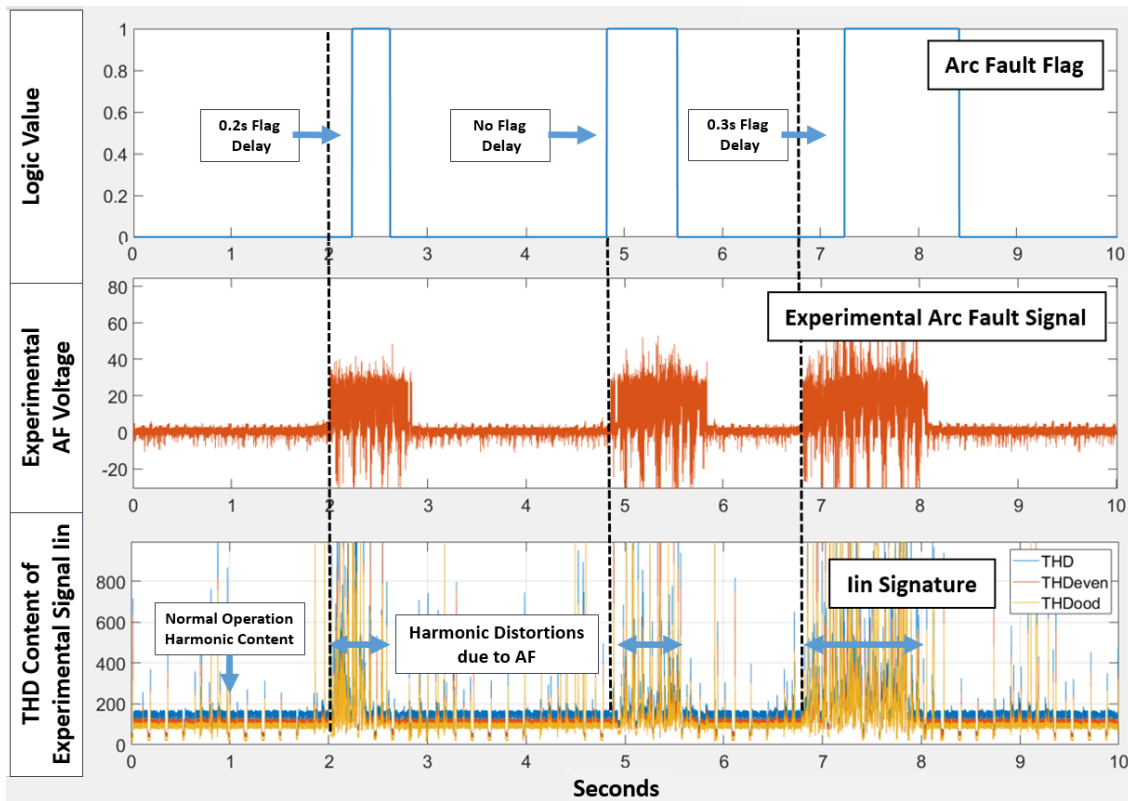


Figure 6.40. AF test 4 with coupling LCL filter.

6.7.7 Irradiation changes in the input source

For grid-connected systems, it is also important to test the robustness to variations in sunlight. These changes are tested in experimentation by changing the input voltage first at a slow speed and a secondly at a higher speed.

In Fig. 6.41 and 6.42 are presented two examples of fast radiance changes and the response of the detection algorithm, the voltage is modified from 50V to 30V and then adjusted again to the nominal 50V. In Fig. 6.41 one small distortion AF flag is generated by algorithm, the cause is not clear, since none of the signals $VH2$ nor Iin presents a high distortion during this period of time. One possible answer is that the variation in the power input source. Nonetheless in the rest of test presented in Fig. 6.42 and Fig. 6.43 and 6.44(b) the signal results are obtained correctly with the algorithm given no AF flag when the change in radiance occurs.

The limit of the maximum 'falling' and 'rising' speed of the voltage under a change of radiation, depends of the capacitor value in the DC/DC converter. Depending of this value the charge and discharge speed will equals the falling and rising speed for this particular case of disturbance.

Since this capacitor value is calculated in order to reduce the converters output ripple voltage, its typically calculated value will not affect in a significant manner the performance of the detection.

Thanks to all the detection results in this thesis, it can be concluded that the approach employed using the peaks value and also the peak concentration within the sliding window allow the algorithm to perform accurate detection under a wide range of loads. This is true not only in an stand alone configuration, but also in an interconnected grid scenario.

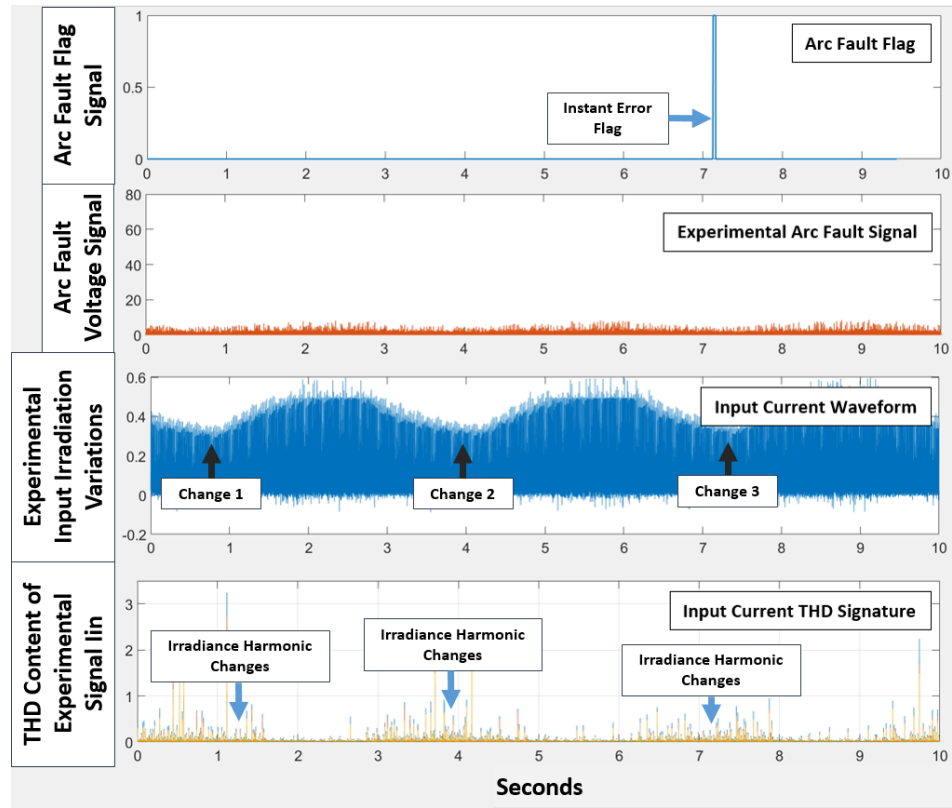


Figure 6.41. Test 1 - fast radiation fluctuation in the DC input source.

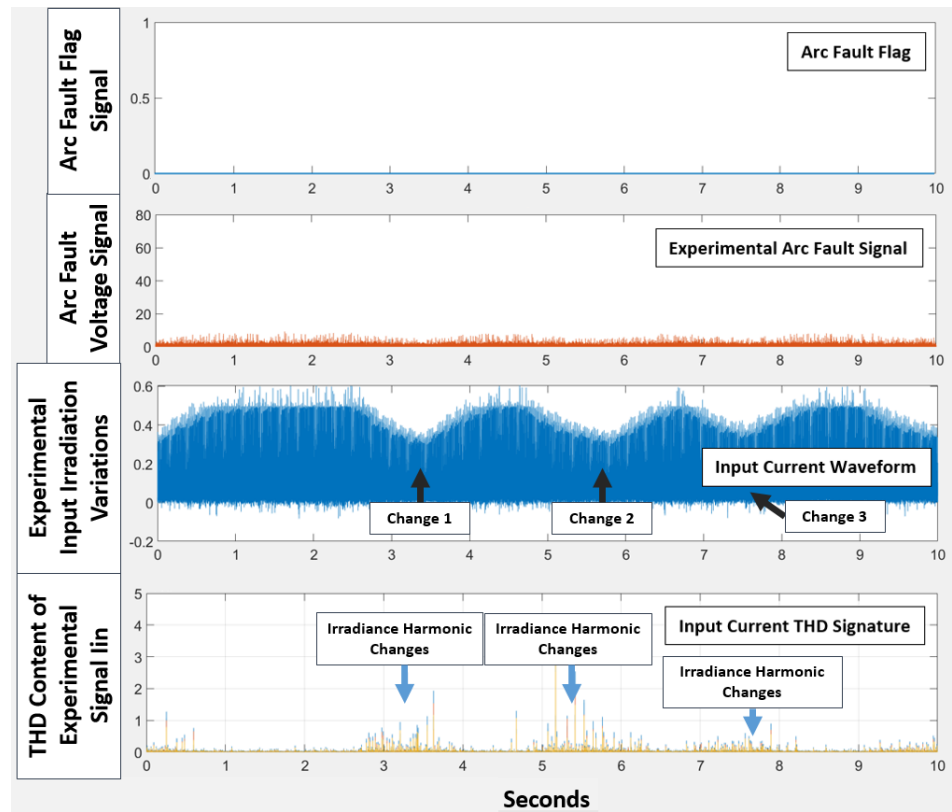


Figure 6.42. Test 2 - fast radiation fluctuation in the DC input source.

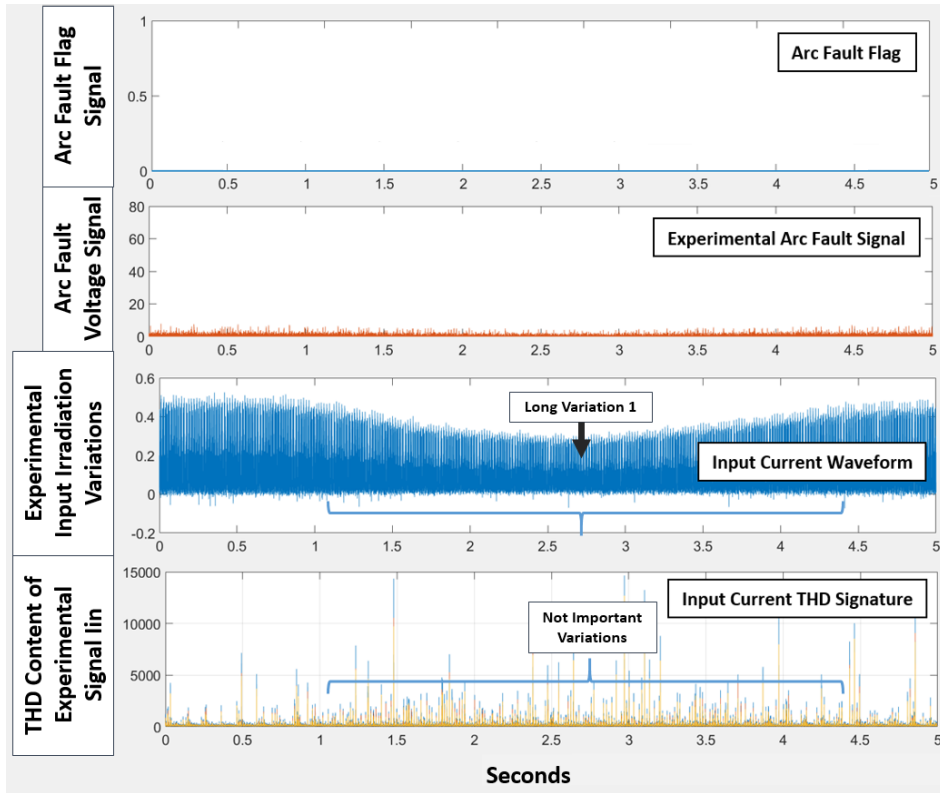


Figure 6.43. Test 3 - slow radiation fluctuation in the DC input source.

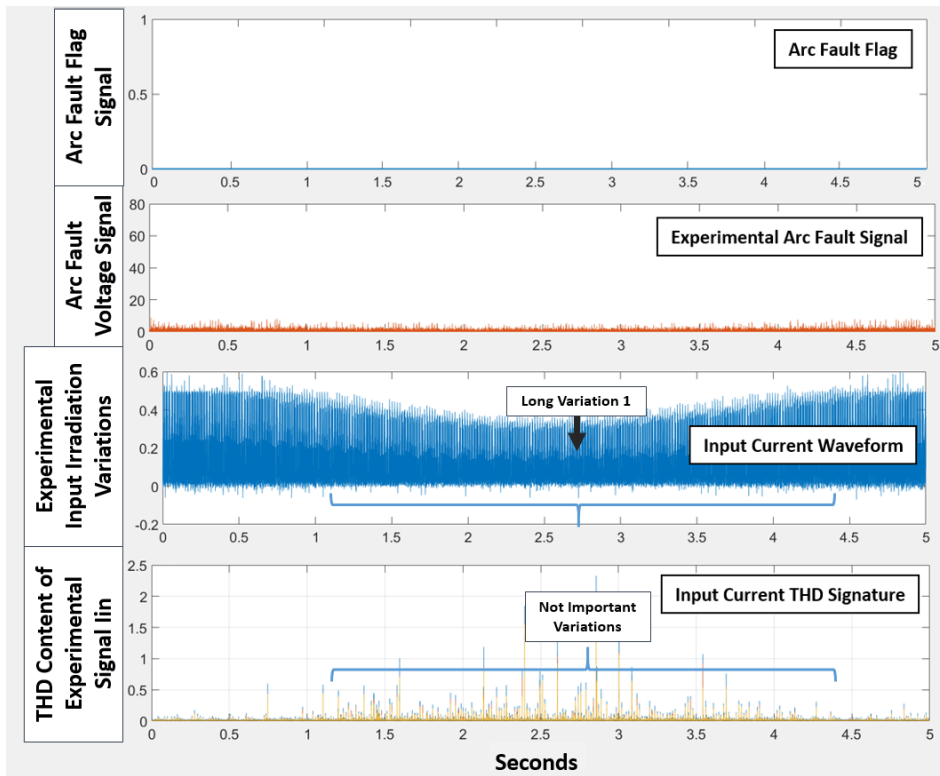


Figure 6.44. Test 4 - slow radiation fluctuation in the DC input source.

Chapter 7

Conclusions

In this research work was achieved the conception and development of a novel PV inverter topology, that posses features highly desired in the modern grid, such as: reduced number of components, nine-level AC output, elevation and reduction capabilities of the DC input, all achieved with a transformerless topology. Nonetheless the main contribution of this research was the development of a novel DC arc fault detection technique based in the signal treatment of the internal PV inverter signals.

This was possible thanks to the initial results obtained for the stand alone system. Next a improve detections strategy is adopted by the use of a sliding window that combines the use of an $THDe$ limit for normal operation in signal $VH2$ and I_{in} . Additionally, the number of $THDe$ peaks withing a period of signal $VH2$ is integrated into the decision stage of the algorithm. This technique was validated in both isolated and grid interconnected configurations with a various types of loads. In the totality of experimental cases presented the proposed algorithm successfully detect the presence of the AF (multiple AF's in certain cases). The effectiveness of detection was not compromised by the load type connected to the inverter or the perturbation related to the changes in PV irradiation. Also, the proposal of real time implementation of the algorithm is described for future development.

7.1 Achievements of this Work

The principal achievements of this thesis are listed below:

- Identification of the main components needed for the conceptualization of the PV inverter.
- Modeling of the novel DC/DC and DC/AC converters in *Simulink*.
- Modeling of the whole inverter topology on *Simulink*.
- Design and fabrication of the prototype boards required for the implementation of the developed DC/DC "boost" variant converter.
- Design and fabrication of the prototype boards required for the implementation of the developed DC/DC "buck" variant converter.
- Design and fabrication of the prototype boards required to implement the asymmetrical cascade cell multilevel inverter.
- Research and acquisition of the needed laboratory equipment (new loads, supply sources, PV panels, artificial illumination system, differential voltage probes, MPPT tracking board, etc.) to successfully test the system.
- Development of the AF generation system according to standard UL1699B.
- Experimental test bench setup and calibration.
- Integration of a *Simulink* method for the use of experimental AF signatures into simulation.
- Conception of a novel approach for arc fault detection, based on the harmonic index.
- Matlab coding of the proposed algorithm.

- Construction of an experimental signal data base of approximately 350 cases.

7.2 Future Research Works

The algorithm is intended to be programmed in a digital signal processor (DSP). The strategy to follow in order to implement the designed algorithm into the DSP, is to adapt the *Matlab* code so that signals can be sampled with a window small enough in order to fulfill the UL 1699B recommended detection time of 1-3 second.

This can be accomplished by employing the DSP toolbox (Matlab), that will allow to read the analog signals of *VH2* and *Iout* in real time and then perform the signal processing to obtain the values needed for both signals. Since the control for both DC/DC and DC/AC stages of the proposed inverter can be accomplished using simulink into the DSP, the detection subroutine can be added to the programming cycle to be downloaded at the same time with the control. This implementation is key factor to achieve the real time detection.

In this research was possible to combine two scientific fields in order to solve rising electrical needs in the renewable energy field. Thanks to this some work remain to be done, the principal ones are enlisted below:

1. The detection algorithm based in the technique presented in this thesis will be implemented in a DSP.
2. The evaluation of the inverter employing a seven-levels single bridge multilevel DC/AC inverter, remains to be studied and also the capacities of AF detection may be improved with the use of this topology.
3. The implementation of the proposed detection approach into a DSP or a FPGA to evaluate in the test bench the real AF scenario response time.
4. The regulation capacities of the converters are out of scope of this work, nonetheless this feature may prove worthy of testing, considering the fact that if the AF minimum

voltage and current levels are not meet the fault will simply disappear from the system.

References

- [1] A. Rahul Sanjeevan, R. S. Kaarthik, K. Gopakumar, P. P. Rajeevan, J. I. Leon and L. G. Franquelo, “Reduced common-mode voltage operation of a new seven-level hybrid multilevel inverter topology with a single dc voltage source,” *IET Power Electronics*, vol. 9, no. 3, pp. 519–528, 2016.
- [2] H. Wu, L. Zhu, F. Yang, T. Mu and H. Ge, “Dual-dc-port asymmetrical multilevel inverters with reduced conversion stages and enhanced conversion efficiency,” *IEEE Transactions on Industrial Electronics*, vol. 64, pp. 2081–2091, March 2017.
- [3] J. Rodriguez-Rodriguez, V. Venegas-Rebollar and E. Moreno-Goytia, “Single dc-sourced 9-level dc/ac topology as transformerless power interface for renewable sources,” *Energies*, vol. 8, pp. 1273–1290, 02 2015.
- [4] G. Buticchi, D. Barater, E. Lorenzani, C. Concari and G. Franceschini, “A nine-level grid-connected converter topology for single-phase transformerless pv systems,” *IEEE Transactions on Industrial Electronics*, vol. 61, pp. 3951–3960, Aug 2014.
- [5] S. G. Song, F. S. Kang and S. J. Park, “Cascaded multilevel inverter employing three-phase transformers and single dc input,” *IEEE Transactions on Industrial Electronics*, vol. 56, pp. 2005–2014, June 2009.
- [6] J. C. Wu and C. W. Chou, “A solar power generation system with a seven-level inverter,” *IEEE Transactions on Power Electronics*, vol. 29, pp. 3454–3462, July 2014.

-
- [7] N. A. Rahim, K. Chaniago and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," *IEEE Transactions on Industrial Electronics*, vol. 58, pp. 2435–2443, June 2011.
- [8] A. Nami, F. Zare, A. Ghosh and F. Blaabjerg, "A hybrid cascade converter topology with series-connected symmetrical and asymmetrical diode-clamped h-bridge cells," *IEEE Transactions on Power Electronics*, vol. 26, pp. 51–65, Jan 2011.
- [9] H. Sepahvand, J. Liao, M. Ferdowsi and K. A. Corzine, "Capacitor voltage regulation in single-dc-source cascaded h-bridge multilevel converters using phase-shift modulation," *IEEE Transactions on Industrial Electronics*, vol. 60, pp. 3619–3626, Sept 2013.
- [10] P. Roshankumar, P. P. Rajeevan, K. Mathew, K. Gopakumar, J. I. Leon and L. G. Franquelo, "A five-level inverter topology with single-dc supply by cascading a flying capacitor inverter and an h-bridge," *IEEE Transactions on Power Electronics*, vol. 27, pp. 3505–3512, Aug 2012.
- [11] S. Vazquez, J. I. Leon, L. G. Franquelo, J. J. Padilla and J. M. Carrasco, "Dc voltage ratio control strategy for multilevel cascaded converters fed with a single dc source," *IEEE Transactions on Industrial Electronics*, vol. 56, pp. 2513–2521, July 2009.
- [12] Z. Du, L. M. Tolbert, B. Ozpineci and J. N. Chiasson, "Fundamental frequency switching strategies of a seven-level hybrid cascaded h-bridge multilevel inverter," *IEEE Transactions on Power Electronics*, vol. 24, pp. 25–33, Jan 2009.
- [13] A. Tsunoda, Y. Hinago and H. Koizumi, "Level- and phase-shifted pwm for seven-level switched-capacitor inverter using series/parallel conversion," *IEEE Transactions on Industrial Electronics*, vol. 61, pp. 4011–4021, Aug 2014.
- [14] L. Mackay, A. Shekhar, B. Roodenburg, L. Ramirez Elizondo and P. Bauer, "Series arc extinction in dc microgrids using load side voltage drop detection," pp. 239–244, June 2015.

-
- [15] Underwires Laboratories Inc. 1699b, "Outline of investigation for photovoltaic (pv) dc arc-fault circuit protection," in *Issue Number I*, pp. 239–244, April 29 2011.
- [16] M. K. Alam, F. Khan, J. Johnson and J. Flicker, "A comprehensive review of catastrophic faults in pv arrays: Types, detection, and mitigation techniques," *IEEE Journal of Photovoltaics*, vol. 5, pp. 982–997, May 2015.
- [17] J. Johnson, "Photovoltaic dc arc fault detector testing at sandia national laboratories," in *2011 37th IEEE Photovoltaic Specialists Conference, Seattle, WA, 2011*, pp. 003614-003619.
- [18] U.S. Energy Information Administration, "Annual energy outlook 2019," in *Office of Energy Analysis U.S. Department of Energy Washington, DC 20585*, January 2019.
- [19] J. Holtz and H. P. Wurm, "A new type of voltage fed inverter for the megawatt range," *Elektr. Bahnen*, vol. vol. 80, pp. pp. 214–221, 1982.
- [20] J. Holtz, "Self-commutated three-phase inverters with staircase voltage waveforms for high-power applications at low switching frequency," *Siemens Res. Dev. Rep*, vol. vol. 6, no. 3, pp. pp. 164–171, 1977, 1983.
- [21] A. Nabae, I. Takahashi and H. Akagi, "A new neutral-point-clamped pwm inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, pp. 518–523, Sep. 1981.
- [22] R. H. Baker and L. H. Bannister, "Electric power converter," *U.S. t*, pp. 3 867 643,, Feb. 18, 1975.
- [23] J. Rodriguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 724–738, Aug 2002.
- [24] R. H. Baker, "Switching circuit," *U.S. Patent*, p. 4 210 826, Jul. 1, 1980.
- [25] R. H. Baker, "Bridge converter circuit," *U.S. Patent*, p. 4 270 163, May 26, 1981.

- [26] F. Z. Peng and J. S. Lai, "Multilevel cascade voltage-source inverter with separate dc sources," *U.S. Patent*, p. 5 642 275, Jun. 24, 1997.
- [27] P.W. Hammond, "Four-quadrant ac-ac drive and method," in *U.S. Patent 6 166 513*, Dec. 26, 2000.
- [28] M. F. Aiello, P. W. Hammond, and M. Rastogi, "Modular multi-level adjustable supply with series connected active inputs," in *U.S. Patent 6 236 580*, May 22, 2001.
- [29] T. Meynard, J. P. Lavieville, P. Carrere, J. Gonzalez and O. Bethoux, "Electronic circuit for converting electrical energy," in *U.S. Patent 5 706 188*, Jan. 6, 1998.
- [30] J. P. Lavieville, P. Carrere and T. Meynard, "Electronic circuit for converting electrical energy and a power supply installation making use thereof," in *U.S. Patent 5 668 711*, Sep. 16, 1997.
- [31] K. Corzine, "Operation and design of multilevel inverters," in *Developed for the Office of Naval Research*, Dec. 2003, Rev. Jun. 2005.
- [32] A. Muetze and A. Binder, "Experimental evaluation of mitigation techniques for bearing currents in inverter-supplied drive-systems - investigations on induction motors up to 500 kw," in *IEEE International Electric Machines and Drives Conference, 2003. IEMDC'03.*, vol. 3, pp. 1859–1865 vol.3, June 2003.
- [33] J. D. Barros and J. F. Silva, "Optimal predictive control of three-phase npc multilevel converter for power quality applications," *IEEE Transactions on Industrial Electronics*, vol. 55, pp. 3670–3681, Oct 2008.
- [34] Lei Lin, Yunping Zou, Zhan Wang and Hongyuan Jin, "Modeling and control of neutral-point voltage balancing problem in three-level npc pwm inverters," in *2005 IEEE 36th Power Electronics Specialists Conference*, pp. 861–866, June 2005.
- [35] O. Ojo and S. Konduru, "A discontinuous carrier-based pwm modulation method for the

- control of the neutral point voltage of three-phase three-level diode clamped converters,” in *2005 IEEE 36th Power Electronics Specialists Conference*, pp. 1652–1658, June 2005.
- [36] D. Xu and B. Wu, “Multilevel current source inverters with phase shifted trapezoidal pwm,” in *2005 IEEE 36th Power Electronics Specialists Conference*, pp. 2540–2546, June 2005.
- [37] T. Bruckner and D. G. Holmes, “Optimal pulse-width modulation for three-level inverters,” *IEEE Transactions on Power Electronics*, vol. 20, pp. 82–89, Jan 2005.
- [38] S.S. Fazel, “Investigation and comparison of multi-level converters for medium voltage applications,” in *Ph.D. dissertation, Technische Universität Berlin, Berlin, Germany, 2007*.
- [39] D. Krug, S. Bernet, S. S. Fazel, K. Jalili and M. Malinowski, “Comparison of 2.3-kv medium-voltage multilevel converters for industrial medium-voltage drives,” *IEEE Transactions on Industrial Electronics*, vol. 54, pp. 2979–2992, Dec 2007.
- [40] M. Veenstra and A. Rufer, “Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives,” *IEEE Transactions on Industry Applications*, vol. 41, pp. 655–664, March 2005.
- [41] Jih-Sheng Lai and Fang Zheng Peng, “Multilevel converters—a new breed of power converters,” *IEEE Transactions on Industry Applications*, vol. 32, pp. 509–517, May 1996.
- [42] P. Hammond, “Medium voltage pwm drive and method,” in *U.S. Patent 5 625 545, Apr. 29, 1997*.
- [43] F. Z. Peng, “A generalized multilevel inverter topology with self voltage balancing,” vol. 3, pp. 2024–2031 vol.3, Oct 2000.
- [44] T. A. Meynard, H. Foch, F. Forest, C. Turpin, F. Richardeau, L. Delmas, G. Gateau

- and E. Lefeuvre, "Multicell converters: derived topologies," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 978–987, Oct 2002.
- [45] P. W. Hammond, "A new approach to enhance power quality for medium voltage ac drives," *IEEE Transactions on Industry Applications*, vol. 33, pp. 202–208, Jan 1997.
- [46] L. M. Tolbert, Fang Zheng Peng and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Transactions on Industry Applications*, vol. 35, pp. 36–44, Jan 1999.
- [47] M. F. Escalante, J. Vannier and A. Arzande, "Flying capacitor multilevel inverters and dtc motor drive applications," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 809–815, Aug 2002.
- [48] A. Rufer, "An aid in the teaching of multilevel inverters for high power applications," vol. 1, pp. 347–352 vol.1, June 1995.
- [49] S. Alepuz, S. Busquets-Monge, J. Bordonau, J. Gago, D. Gonzalez and J. Balcells, "Interfacing renewable energy sources to the utility grid using a three-level inverter," *IEEE Transactions on Industrial Electronics*, vol. 53, pp. 1504–1511, Oct 2006.
- [50] L. M. Tolbert and F. Z. Peng, "Multilevel converters as a utility interface for renewable energy systems," in *2000 Power Engineering Society Summer Meeting (Cat. No.00CH37134)*, vol. 2, pp. 1271–1274 vol. 2, July 2000.
- [51] S. Daher, J. Schmid and F. L. M. Antunes, "Multilevel inverter topologies for stand-alone pv systems," *IEEE Transactions on Industrial Electronics*, vol. 55, pp. 2703–2712, July 2008.
- [52] S. J. Lee, H. S. Bae and B. H. Cho, "Modeling and control of the single-phase photovoltaic grid-connected cascaded h-bridge multilevel inverter," in *2009 IEEE Energy Conversion Congress and Exposition*, pp. 43–47, Sep. 2009.

- [53] R. Gonzalez, E. Gubia, J. Lopez and L. Marroyo, "Transformerless single-phase multilevel-based photovoltaic inverter," *IEEE Transactions on Industrial Electronics*, vol. 55, pp. 2694–2702, July 2008.
- [54] L. M. Tolbert, Fang Zheng Peng, and T. G. Habetler, "A multilevel converter-based universal power conditioner," *IEEE Transactions on Industry Applications*, vol. 36, pp. 596–603, March 2000.
- [55] J. I. Leon, S. Vazquez, S. Kouro, L. G. Franquelo, J. M. Carrasco and J. Rodriguez, "Unidimensional modulation technique for cascaded multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 56, pp. 2981–2986, Aug 2009.
- [56] Y. Liu, A. Q. Huang, W. Song, S. Bhattacharya and G. Tan, "Small-signal model-based control strategy for balancing individual dc capacitor voltages in cascade multilevel inverter-based statcom," *IEEE Transactions on Industrial Electronics*, vol. 56, pp. 2259–2269, June 2009.
- [57] O. Lopez, J. Alvarez, J. Doval-Gandoy, F. D. Freijedo, A. Nogueiras, A. Lago and C. M. Penalver, "Comparison of the fpga implementation of two multilevel space vector pwm algorithms," *IEEE Transactions on Industrial Electronics*, vol. 55, pp. 1537–1547, April 2008.
- [58] C. Hochgraf, R. Lasseter, D. Divan and T. A. Lipo, "Comparison of multilevel inverters for static var compensation," vol. 2, pp. 921–928 vol.2, Oct 1994.
- [59] D. G. Holmes and T. A. Lipo, "pulse with modulation for power converters," in *Wiley 2003*.
- [60] M. P. Kazmierkowski and L. Malesani, "Current control techniques for three-phase voltage-source pwm converters: a survey," *IEEE Transactions on Industrial Electronics*, vol. 45, pp. 691–703, Oct 1998.
- [61] G. Beinhold, R. Jacob and M. Nahrstaedt, "A new range of medium voltage multilevel

- inverter drives with floating capacitor technology,” in *in Proc. EPE, Graz, Austria, 2001, [CD-ROM]*.
- [62] J. Holtz and N. Oikonomou, “Neutral point potential balancing algorithm at low modulation index for three-level inverter medium-voltage drives,” *IEEE Transactions on Industry Applications*, vol. 43, pp. 761–768, May 2007.
- [63] P. Enjeti and R. Jakkli, “Optimal power control strategies for neutral point clamped (npc) inverter topology,” in *Conference Record of the IEEE Industry Applications Society Annual Meeting*, pp. 924–930 vol.1, Oct 1989.
- [64] B. Steffen, “State of the art and developments of medium voltage converters - an overview,” *Przegald Elektrotechniczny*, vol. 82, pp. 1–10, 01 2006.
- [65] L. G. Franquelo, J. Rodriguez and J. I. Leon, S. Kouro, R. Portillo and M. A. M. Prats, “The age of multilevel converters arrives,” *IEEE Industrial Electronics Magazine*, vol. 2, pp. 28–39, June 2008.
- [66] R. Klug and N. Klaassen, “High power medium voltage drives - innovations, portfolio, trends,” in *2005 European Conference on Power Electronics and Applications*, pp. 10 pp.–P.10, Sep. 2005.
- [67] R. C. Portillo, M. M. Prats, J. I. Leon, J. A. Sanchez, J. M. Carrasco, E. Galvan and L. G. Franquelo, “Modeling strategy for back-to-back three-level converters applied to high-power wind turbines,” *IEEE Transactions on Industrial Electronics*, vol. 53, pp. 1483–1491, Oct 2006.
- [68] T. A. Meynard, M. Fadel and N. Aouda, “Modeling of multilevel converters,” *IEEE Transactions on Industrial Electronics*, vol. 44, pp. 356–364, June 1997.
- [69] S. S. Fazel, S. Bernet, D. Krug and K. Jalili, “Design and comparison of 4-kv neutral-point-clamped, flying-capacitor, and series-connected h-bridge multilevel converters,” *IEEE Transactions on Industry Applications*, vol. 43, pp. 1032–1040, July 2007.

- [70] J. K. Steinke, "Use of an lc filter to achieve a motor-friendly performance of the pwm voltage source inverter," *IEEE Transactions on Energy Conversion*, vol. 14, pp. 649–654, Sep. 1999.
- [71] S. Pohler, A. Mertens and R. Sommer, "Optimisation of output filters for inverter fed drives," in *IECON 2006 - 32nd Annual Conference on IEEE Industrial Electronics*, pp. 1082–1088, Nov 2006.
- [72] F. Khoucha, S. M. Lagoun, K. Marouani, A. Kheloui and M. E. H. Benbouzid, "Hybrid cascaded h-bridge multilevel inverter motor drive dtc control for electric vehicles," in *2008 18th International Conference on Electrical Machines*, pp. 1–6, Sep. 2008.
- [73] S. Sirisukprasert, Zhenxue Xu and Bin Zhang, J. Lai and A. Q. Huang, "A high-frequency 1.5 mva h-bridge building block for cascaded multilevel converters using emitter turn-off thyristor," in *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335)*, vol. 1, pp. 27–32 vol.1, March 2002.
- [74] L. A. Tolbert, Fang Zheng Peng, T. Cunnyngham and J. N. Chiasson, "Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 1058–1064, Oct 2002.
- [75] M. D. Manjrekar and T. A. Lipo, "A hybrid multilevel inverter topology for drive applications," in *APEC '98 Thirteenth Annual Applied Power Electronics Conference and Exposition*, vol. 2, pp. 523–529 vol.2, Feb 1998.
- [76] Z. Cheng and B. Wu, "A novel switching sequence design for five-level npc/h-bridge inverters with improved output voltage spectrum and minimized device switching frequency," *IEEE Transactions on Power Electronics*, vol. 22, pp. 2138–2145, Nov 2007.
- [77] W. Bower, A. Quintana and J. Johnson, "Electrical and thermal finite element modeling of arc faults in photovoltaic bypass diodes," in *presented at the World Renew. Energy Forum, Denver, CO, USA, May 16, 2012*.

- [78] J. Strauch, "Solar module arc fault modeling at sandia national laboratories," in *Sandia Nat. Lab., Albuquerque NM, USA, Tech. Rep. SAND2010-5881C*, Jun. 2010.
- [79] X. Yao, L. Herrera, S. Ji, K. Zou and J. Wang, "Characteristic study and time-domain discrete- wavelet-transform based hybrid detection of series dc arc faults," *IEEE Transactions on Power Electronics*, vol. 29, pp. 3103–3115, June 2014.
- [80] P. M. Hall and K. Myers, "Arcing faults on direct current trolley systems," in *in Proc. 50th WVU Conf. Coal Mine Electrotechnol., Morgantown*, pp. 1–19, 1978.
- [81] F. Schimpf and L. E. Norum, "Recognition of electric arcing in the dc-wiring of photovoltaic systems," in *INTELEC 2009 - 31st International Telecommunications Energy Conference*, pp. 1–6, Oct 2009.
- [82] C. Nayar, H. Dehbonei, and L. Chang, "A low cost power electronic interface for small scale wind generators in single phase distributed power generation system," 11 2019.
- [83] A. B. Raju, "Applications of power electronic interfaces for grid connected variable speed wind energy conversion systems," in *PhD thesis, Department of Electrical Engineering, Indian Institute of Technology, Bombay, India*, 2005.
- [84] K. Tan and S. Islam, "Optimum control strategies in energy conversion of pmsg wind turbine system without mechanical sensors," *IEEE Transactions on Energy Conversion*, vol. 19, pp. 392–399, June 2004.
- [85] H. D. C. Nayar and L. Chang, "An igt inverter for interfacing small scale wind generators to single phase distributed power generation systems," *IEEE Transactions on Energy Conversion*, vol. Proc. Solar 2004: Life, the Universe and Renewables, 30 November - 3 December, Murdoch University, Western Australia 2004.
- [86] V. Lazarov, Z. Zarkov, and H. Kanchev, "Grid-connected single-phase inverter for renewable energy sources," *Proceedings of the Technical University - Sofia*, vol. Vol.59, pp. 103–111, 11 2009.

- [87] L. Mihet-Popa and V. Groza, "Modeling, control design and simulation of a grid connection control mode for a small variable-speed wind turbine system," in *2009 IEEE Electrical Power Energy Conference (EPEC)*, pp. 1–6, Oct 2009.
- [88] L. Mihet-Popa, V. Groza, O. Prostean, and I. Szeidert, "Modeling and design of a grid connection control mode for a small variable-speed wind turbine system," in *2008 IEEE Instrumentation and Measurement Technology Conference*, pp. 288–293, May 2008.
- [89] W. I. Bower and J. C. Wiles, "Analysis of grounded and ungrounded photovoltaic systems," in *Proceedings of 1994 IEEE 1st World Conference on Photovoltaic Energy Conversion - WCPEC (A Joint Conference of PVSC, PVSEC and PSEC)*, vol. 1, pp. 809–812 vol.1, Dec 1994.
- [90] A. 690, "Solar photovoltaic systems of national electrical code," in *NFPA70*, 2011.
- [91] Y. Zhao and R. Lyons, "Ground-fault analysis and protection in pv arrays," in *in Proc. Photovoltaic Protection*, pp. pp.1–4, 2011.
- [92] Y. Zhao, "Fault analysis in solar photovoltaic arrays," in *M.S. thesis, Dept. Elect. Comput. Eng., Northeastern Univ., Boston, MA, USA*, 2010.
- [93] T. Markvart and L. Castaner, "Practical handbook of photovoltaics: Fundamentals and applications," in *Elsevier Advanced Technology. Amsterdam, The Netherlands: Elsevier Sci.*, 2003.
- [94] T. Markvart and L. Castaner, "Standard for flat plate photovoltaic modules and panels," in *UL 1703*, 2002.
- [95] J. Flicker and J. Johnson, "Photovoltaic ground fault and blind spot electrical simulations," in *Sandia Nat. Lab., Albuquerque NM, USA, Tech. Rep. SAND2013-3459*, Jun. 2013.
- [96] J. Johnson, M. Montoya, S. McCalmont, G. Katzir, F. Fuks, J. Earle, A. Fresquez, S.

- Gonzalez and J. Granata, "Differentiating series and parallel photovoltaic arc-faults," in *2012 38th IEEE Photovoltaic Specialists Conference*, pp. 000720–000726, June 2012.
- [97] J. Johnson, S. Kuzmaul, W. Bower and D. Schoenwald, "Using pv module and line frequency response data to create robust arc fault," in *in Proc. 26th Eur. Photovoltaic Sol. Energy Conf., 2011*, pp. 3745-3750.
- [98] J. Johnson, D. Schoenwald, S. Kuzmaul, J. Strauch and W. Bower, "Creating dynamic equivalent pv circuit models with impedance spectroscopy for arc fault modeling," in *in Proc. 37th IEEE Photovoltaic Spec. Conf., Seattle, WA, USA, Jun. 19-24, 2011*, pp. 2328 - 2333.
- [99] J. Johnson, C. Oberhauser, M. Montoya, A. Fresquez, S. Gonzalez and A. Patel, "Crosstalk nuisance trip testing of photovoltaic dc arc-fault detectors," in *in Proc. 39th IEEE Photovoltaic Spec. Conf., Jun. 3-8, 2012*, pp. 1383-1387.
- [100] J. Johnson and J. Kang, "Arc-fault detector algorithm evaluation method utilizing prerecorded arcing signatures," in *Proc. 38th IEEE Photovoltaic Spec. Conf., Jun. 3-8, 2012*, pp. 1378-1382.
- [101] National Electrical Code(R)(NEC) and H. S. N. 70 in *2014 Edition*.
- [102] H. Ayrton, "The electric arc.," in *London, UK: Electrician*, 1902.
- [103] C. P. Steinmetz, "Electric power into light, section vi. the arc.," in *Trans. Amer. Inst. Elect. Eng.*,, vol. 25, p. 802, 1906.
- [104] W. B. Nottingham, "A new equation for the static characteristic of the normal electric arc," *Journal of the American Institute of Electrical Engineers*, vol. 42, pp. 12–19, Jan 1923.
- [105] A. R. Van and C. Warrington, "Reactance relays negligibly affected by arc impedance," in *Elect. World*, vol. 98, pp. 502–505, Sep 1931.

-
- [106] D. B. Miller and J. L. Hildenbrand, "Dc arc model including circuit constraints," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-92, pp. 1926–1934, Nov 1973.
- [107] R. F. Ammerman, T. Gammon, P. K. Sen and J. P. Nelson, "Dc-arc models and incident-energy calculations," *IEEE Transactions on Industry Applications*, vol. 46, pp. 1810–1819, Sep. 2010.
- [108] V. P. Ignatko, "Electric characteristics of ac open heavy-current arcs," in *in Proc. 3rd Int. Symp. Switching Arc Phenom.*, pp. 98–102, 1977.
- [109] T. E. Browne Jr., "The electric arc as a circuit element," in *in Proc. 3rd Int. Symp. Switching Arc Phenom.*, vol. 102, pp. 27–37, 1955.
- [110] A. D. Stokes and W. T. Oppenlander, "Electric arcs in open air," in *Electric arcs in open air, J. Phys. D, Appl. Phys.*, vol. 24, pp. 26–35, Jan 1991.
- [111] E. Acha and M. Madrigal, "Power systems harmonics computer modeling and analysis," *John Wiley & Sons*, 2001.

Appendix A

A.1 Definition of Ground Faults

Typically, PV array has several exposed Non-Current Carrying (NCC) metal conducting parts such as module frames, mounting racks, metal enclosure, distribution panels, the chassis of end-use appliances and power converters [89]. These conductors do not carry any current during normal operation. However, there is a potential risk of electric shock hazard from these exposed NCC conductors when an electrical connection is established between the Current Carrying Conductors (CCC) and NCC conductors due to a fault (e.g., corrosion, loss or melting of insulation, wire cutoff, and wrong wiring). Therefore, all of these NCC conductors are attached together to the ground or earth through a conductor termed an Equipment Grounding Conductor (EGC). This is shown in Fig. A.1 as green lines. Equipment grounding is required by the National Electrical Code (NEC) Article 690.43 to protect people from receiving an electric shock [90]. In order to be in a position to perform a successful analysis of a ground fault, is needed a mathematical model of a PV panel. The model of a PV can be developed by taking into account the parameters: series isolating resistance, parallel isolating resistance, and leakage capacitance of each module. With these three values is possible to represent the PV panel at a Resistive-Capacitive (RC) circuit as showed in Fig. A.3. The main causes for ground faults to happen in PV systems are enlisted below, which are based in the studies and the results of the works [90–93], the same references highlight the fact that many electrical components present in PV installations are not studied in general schematics,

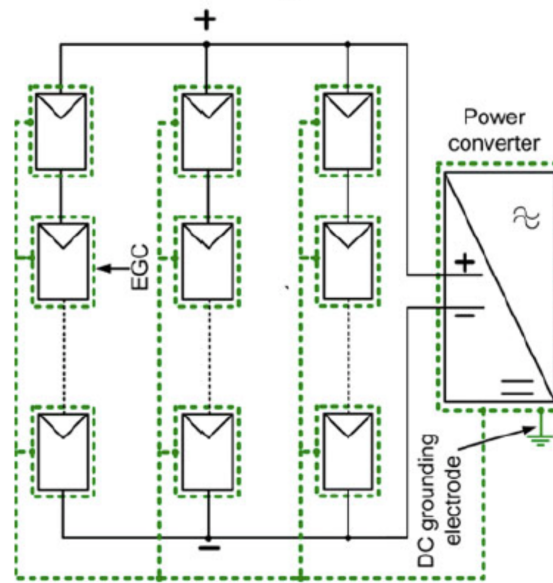


Figure A.1. Schematic diagram of an ungrounded PV system.

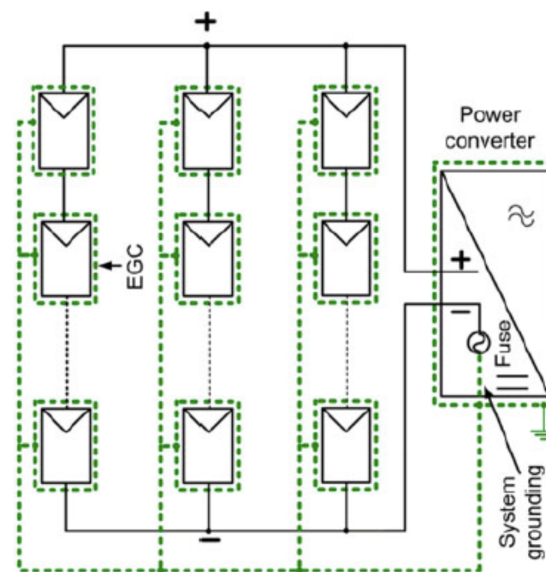


Figure A.2. Schematic diagram of a grounded PV system.

which leaves more variables without modeling and in a real scenario makes difficult the detection and localization of faults. Leading to think that the main reasons behind the fault for each case are: a) Cable insulation damage during the installation due to aging, impact damage, water leakage, and corrosion. b) Ground fault within the PV modules (e.g. degraded sealant and water ingress). c) Insulation damage of cables due to chewing done by rodents. d) Accidental short circuit inside the PV combiner box, often at the time of maintenance.

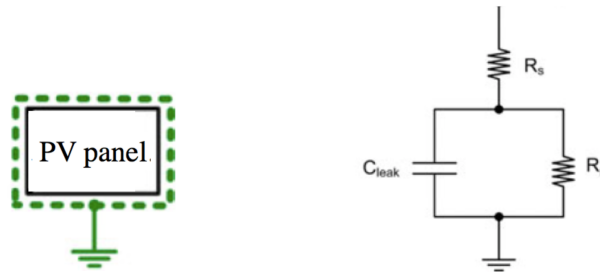


Figure A.3. RC model representation of PV panel.

Various commercial security measures exist to limit the appearance of this fault, although solutions vary from country to country, nonetheless between the solutions that have gain popularity are:

Ground Interruption Fuse: This measure let's drain the current of a fault to the ground and at the same time isolates the PV installation to protect it. There exist some regulations for the sizing of this fuse like the normative UL 1741 published in 2002 [94].

Current leakage monitoring: This method consist of performing a constant current sending, the current that is generated by the PV system is compared to the quantity that is delivered to the load, if exist a difference bigger than a pre-defined window this means that a fault is consuming the rest of the current in some point of the system, and a safety shutdown is performed [95].

Resistance drop Window: This method of detection consists of monitoring the resistance in the ground path, in case of a fault, the resistance will vary its value and if it surpasses a defined limit this means that a fault in the system is present.

A.2 Line to Line Faults

This type of fault is the result of a low impedance current path between two CCCs which often ends in the melting of the conductors due to an excess in the operational current they are designed to work. The magnitude of the current that flows between this two point will be proportional to the number of PV connected in parallel. The maximum current that can flow through the faulty string of a PV array with n number of strings connected in parallel

is $(n-1) \times$ (short-circuit current of each string).

The line to line faults and the line to ground faults share similar causes, this is due that they have similar behavior, thanks to this fact is possible to prevent them by employing strategies like overcurrent protection devices.

A.3 PV Arc Faults

A PV array consists of numerous connections or junctions. All of these joints can be a potential point of arc fault, as presented in Figs. A.4 and A.5.

As an introduction, a current path can be established through the air via arcing due to a discontinuity in a CCCs or due to the insulation breakdown in an adjacent CCCs commonly known as an electric arc fault. If the attention is focus to the case of series AF they occur when there is a fault due to a discontinuity in any of the CCCs resulting from a solder disjoint, cell damage, corrosion of connectors, rodent damage, abrasion from different sources, between other.

Parallel arc fault in adjacent CCCs occur most of the time due to an insulation breakdown. Series and parallel points of arc faults are illustrated in Fig. A.5. Any form of an arc fault is harmful and potentially dangerous for the PV array since it may initiate a fire, especially if the presence of a flammable substance or material is close to the PV. [77, 96–100].

Unlike AC systems, current through the DC arc does not possess a periodic zero crossing, and therefore, it is much more likely that an arc in a PV system will result in a long sustained arc compared with an AC generation system [96], [17]. The impact of this fault is presented in Fig. A.6, in order to prevent this faults series arc-fault protection devices, known as an Arc Fault Circuit Interrupter (AFCI), are needed in any rooftop PV array with DC operating voltage equal or higher than 80 V [101].

This faults are known to have a particular type of behavior as declare [77], an AF have

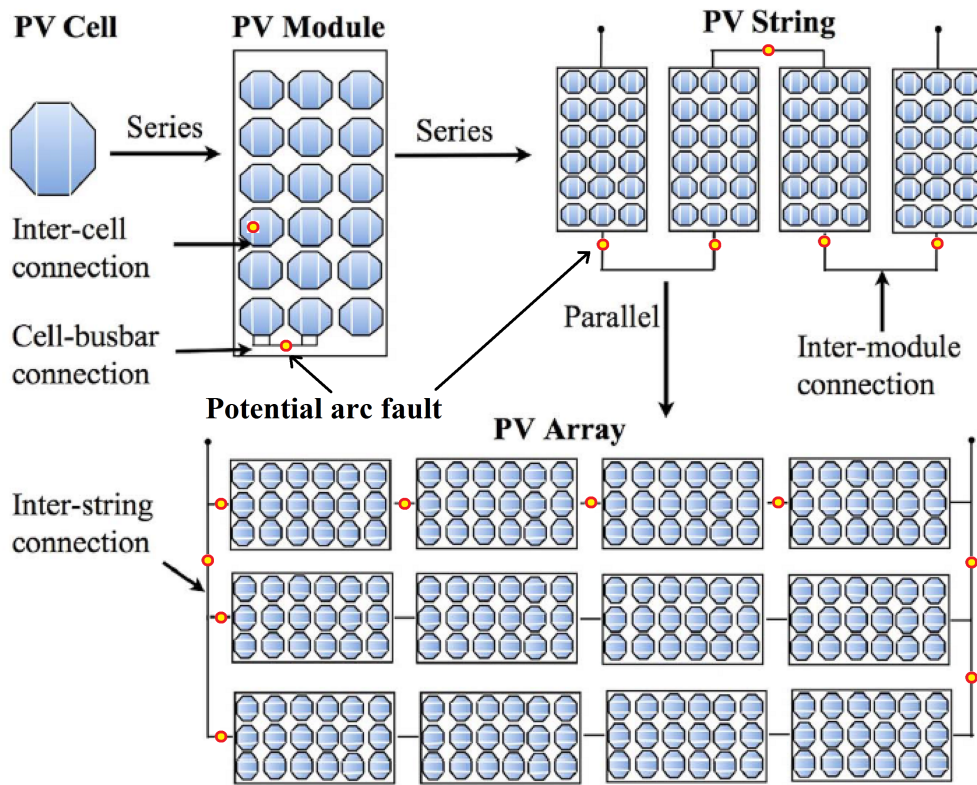


Figure A.4. Potential points of internal fault in a PV panel

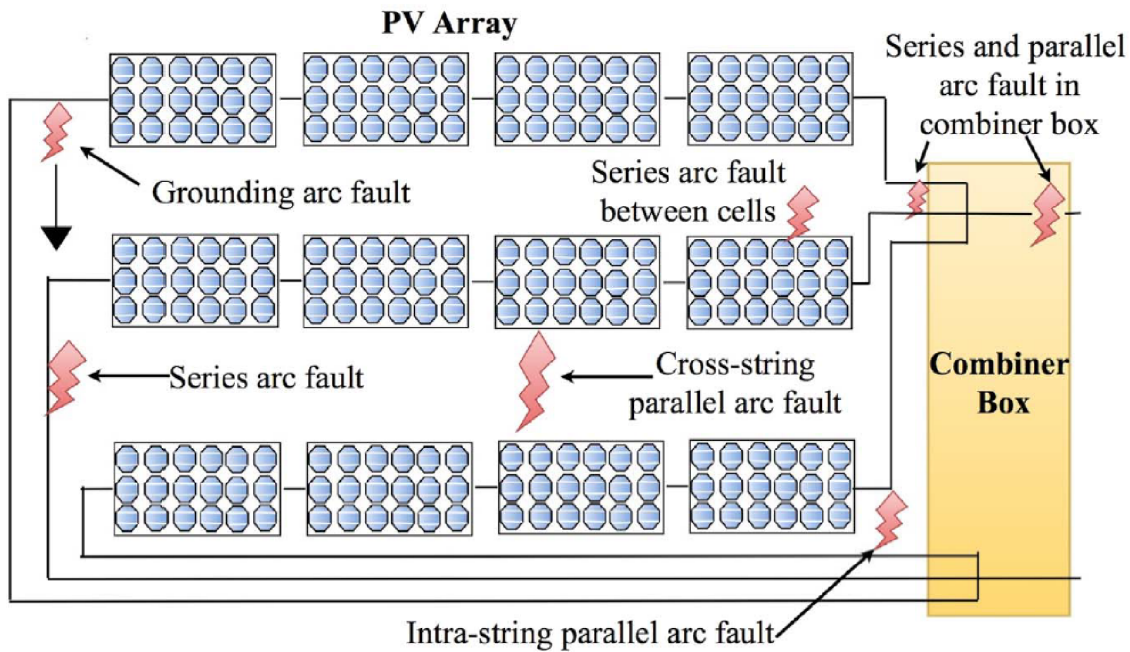


Figure A.5. Potential points of fault in a PV array

a chaotic and not periodical, not stationary behavior, which implies that the development of AFDDs and AFCIs will not only be challenging but commonly adapted for a



Figure A.6. Arc Fault damage in a 10 kW installation, due to inappropriate AF handling.

particular applications which will limit the flexibility of solutions. In case of PV panels the scenario is not different, because each arc faults case posses their own characteristics, each component in the system will play an important role in changing the behavior of the fault, this is the reason why a deeper analysis and modeling of a PV arrangement needs to be accomplished in order to have accurate AFDD. The first standard for AF detection has appeared more than a decade ago as the normative UL 1699, and soon after a second and more detailed revision of it came out and has become the today standard for research and development of AFDD. During the last years with the exponential grown of renewable energy the development of protections in order to have a safe and optimal operation in PV systems has propelled the research of innovative and more efficient AF detection systems.

A.4 Historic Back Ground

The arc theory date back from the early 19th century, were many scientists like A. Ayrton, during different periods of time contribute to the development of the mathematical fundaments for the study of arcs in both AC and DC scenarios.

Ayrton equation Ayrton formulated the first known equation used to model the electrical properties of a steady-state arc [102]. Developed in 1902, was derived for arcs in air initiated between carbon electrodes separated by a few millimeters.

$$V_{arc} = A + BL \frac{C + DL}{I_{arc}} \quad (\text{A.1})$$

The constant A represents the electrode voltage drop, B describes the voltage gradient, and L is the arc length; C and D are constants, which model the arc's nonlinear characteristic.

Steinmetz equation In 1906, Steinmetz derived a semi-empirical V - I equation based on carbon and magnetite arc experiments [103].

$$V_{arc} = A + \frac{C + (L + D)}{I_{arc}^{0.5}} \quad (\text{A.2})$$

In the equation, A , C , and D are constants, and L is the arc length. For a 25.4 mm (1 in) arc with carbon electrodes, the equation is defined as

$$V_{arc} = 36 + \frac{130(1 + 0.33)}{I_{arc}^{0.5}} \quad (\text{A.3})$$

Nottingham equation In the mid 1920s, Nottingham conducted arc research that produced a similar inverse characteristic [104]:

$$V_{arc} = A + \frac{B}{I_{arc}^n} \quad (\text{A.4})$$

The constants A and B are dependent on the arc length and the electrode material. The arc current is raised to a power n , where n varies as a function of the electrode material. For arc lengths ranging from 1.0 to 10.0 mm (0.0394 to 0.394 in), the equation for copper electrodes is specified in the next equation. Also, note that the exponent n is different from the previous two equations.

$$V_{arc} = 27,5 + \frac{44}{I_{arc}^{0.67}} \quad (\text{A.5})$$

Fig. A.7 shows a sample of some typical V–I characteristics of arcs with 6 mm (0.236 in) arc lengths and different electrodes. For constant arc lengths, the Nottingham equation has the exact same general structure as the Ayrton and Steinmetz formulas. The initial arc formulas are based on a limited number of low-current test results. The empirical constants were actually dependent on electrode materials, gap lengths, and gaseous mediums. At this time, there exist no standard procedure to perform experimental tests, and experimental procedures did not follow consistent testing protocols. Consequently, many of the findings have been considered inconclusive.

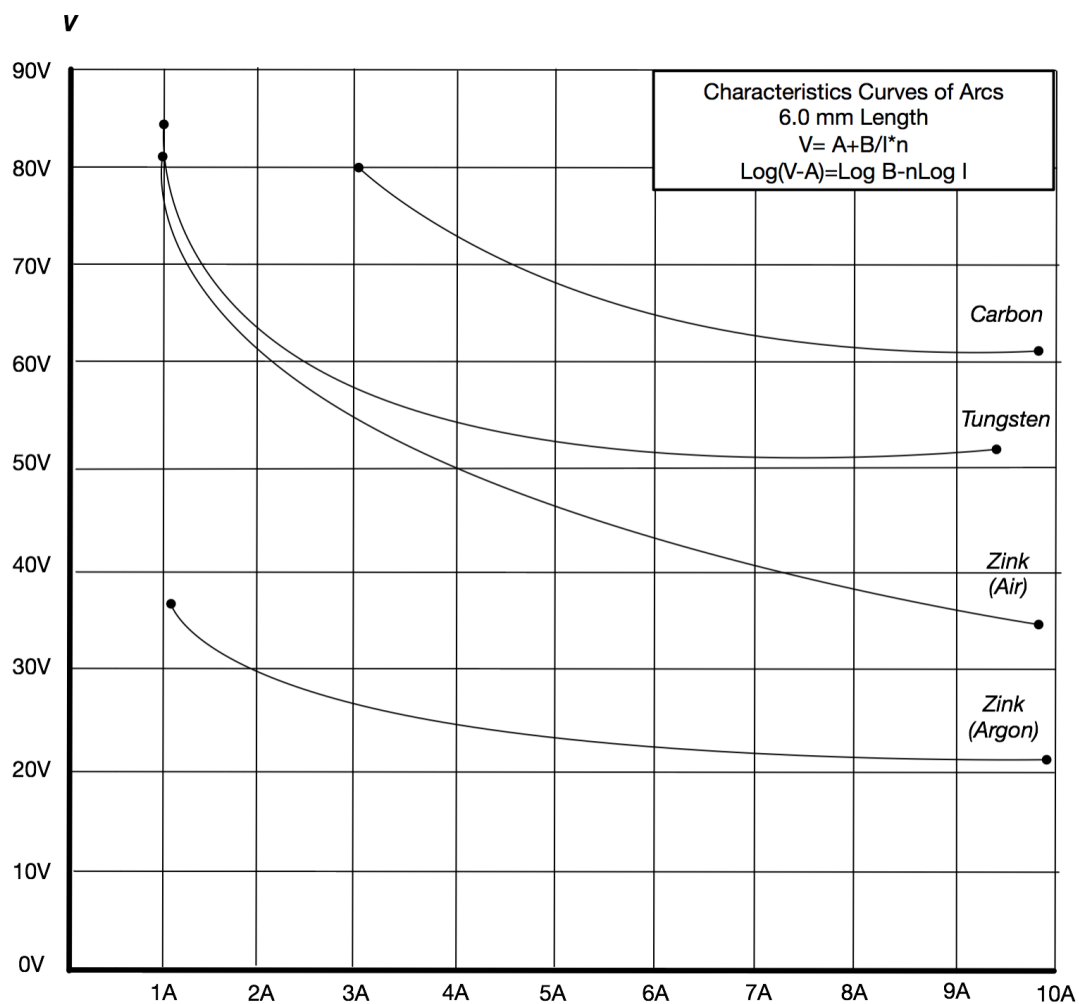


Figure A.7. V-I characteristics curves of AF for different materials of electrodes.

Van and Warrington equation In 1931, Van and Warrington performed a series of tests on high-voltage ac systems for arcing currents between 100 and 1000 A and electrode distances

which spanned several feet [105]. The V–I characteristic of a stable arc was determined as.

$$V_{arc} = \frac{8750L}{I_{arc}^{0.4}} \quad (\text{A.6})$$

In the equation of Warrington L is the arc length in feet. Van and Warrington confirmed the early research performed by Ayrton and Steinmetz by showing that arc voltages are proportional to the arc length and decrease with increasing arcing current. The inverse characteristic was probably exhibited in this current range because of the large gap distance between the electrodes.

Miller and Hildenbrand equations In 1972, Miller and Hildenbrand published a dc-arc model based on an energy-balance concept [106]. As a first approximation, they recommended using the empirical relationship in developed by Nottingham. They emphasized that A , B , and n is not absolute constants but depend on the arc conditions, specifically, electrode material, arc length, and gas species and pressure.

Furthermore, they referenced Cobine's work with the statement that constants are difficult to accurately determine even for a given set of conditions [107].

Ignatko tests Ignatko conducted a series of ac-arc tests which generated arc currents ranging from 5 to 150 kA for arc gaps between 5 and 200 mm (0.197 and 7.87 in). He determined that the total electrode (cathode and anode) drop remained practically constant and measured 23.5 V for copper, 26.5 V for steel, and 36 V for tungsten [108]. Ignatko's results confirm earlier work reporting a 20 V to 40 V drop at the electrodes [109].

Hall, Myers, and Vilicheck equations In 1978, a group of researchers conducted tests to evaluate faults on DC trolley systems [80]. Over 100 DC arc tests were conducted using a 300 V DC supplies. Arcing currents ranged from 300 to 2400 A, and electrode gap widths ranged from 4.8 to 152 mm (3/16 to 6 in). The relationship between the arc voltage and the arc current, is illustrated in Fig. A.8, is based on a number of arc tests with a 9.5-mm (3/8 in) gap. The relationship between the arc current and the arc voltage in a DC trolley

system was committed to match the form defined in Nothinham work. G. Stokes, Oppenlander and Stokes performed perhaps the most exhaustive study of free-burning vertical and horizontal arcs between series electrodes in open air [110]. Current and voltage signals have been recorded for arcs burning with exponentially decaying currents from 1000 to 0.1 A, and 50 Hz arcs for sinusoidal currents with amplitudes decaying from 20 kA to 30 A [110].

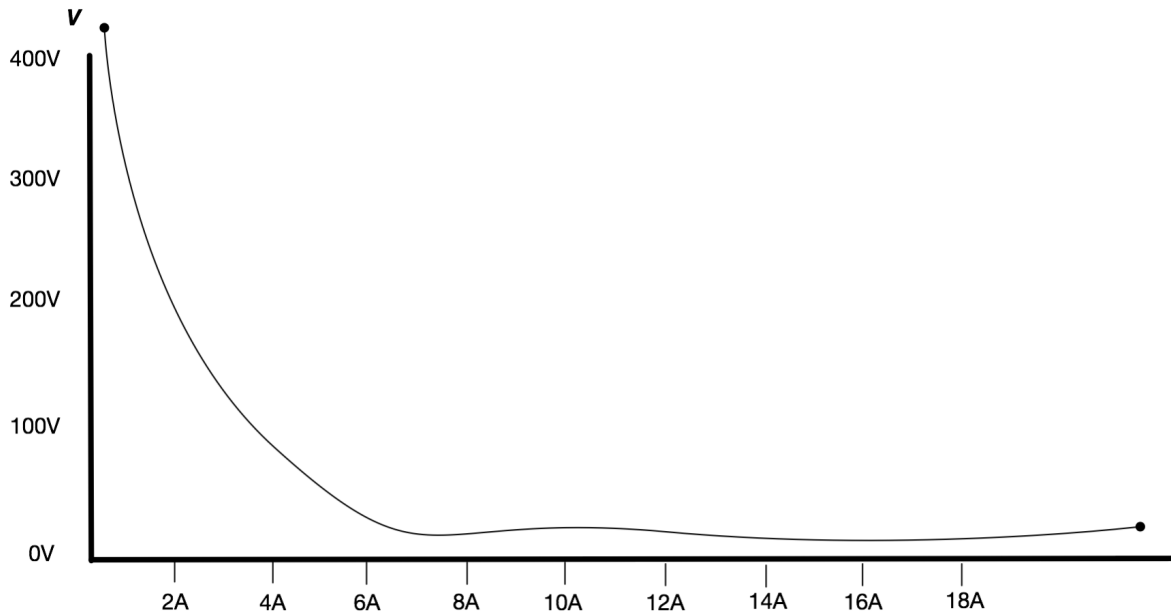


Figure A.8. V-I AF ignition curve.

All of the models presented and developed this early years studies share in common the following characteristics:

- Arc resistance is nonlinear.
- Arc resistance is dependent on multiple factors: a) gap length, b) electrode material, c) arc-current magnitude, d) electrode configuration.

The models proposed by the precedent authors have been based on tests conducted over more than a century by different researchers across different countries and under very different protocols. However despite the wide range of testing methods and conditions, the results are remarkably similar.

At low current levels, the V–I characteristic is inversely proportional and nonlinear. At high arcing-current levels, the analysis shows that the arc-resistance voltage-drop approaches a constant value. In an effort to quantify the risks associated with high-current DC systems.

Arcing behavior is highly variable, and the existing DC arc models cannot be accurately and reliably assess all the characteristics of dc arcs. Additional arc testing is needed to develop more accurate V–I characteristics and better DC arc resistance models. Extensive testing in a controlled environment is needed to study the incident-energy levels associated with DC arcing faults. A hazard risk assessment is needed to identify where DC arcing faults might be initiated in industrial power systems.

Appendix B

B.1 Smart Inverter PCB Conception

In this chapter will be presented with details, the construction and developments of the experimental boards that allow to obtain the results presented throughout this chapter, for both variants of the smart inverter.

B.1.1 Conception of the Isolated Double Buck Converter Board

In order to experimentally evaluate the performance of the smart inverter, a series of PCB's have been developed, two of them, one for each DC/DC stage variant, and two PCB's, for the full bridge for cascade cells DC/AC multilevel stage. In Fig. B.1, is presented the designed layout for the DC/DC Buck variant of the smart inverter, IN Fig. B.1 a) is presented the bottom layer of the PCB, and in Fig. B.1 b) is presented the 3D generated physical appearance of the converter. For this development the main switching devices chosen is an IGBT, model *IRG4PC50FD* which is a 4 generation IGBT that reduces the disturbances of commutation in a effective way without the use of a calculated snubber circuitry, with this the loses and the possible points of failure of the PCB are reduced.

In order to control each IGBT, a strategy employing an interface that make use of a high frequency optical insulator (*TLP250*) and a micro DC/DC converter (*TracoPowerTME0512S*) that increase the voltage of the interface from 5v to 12v, with

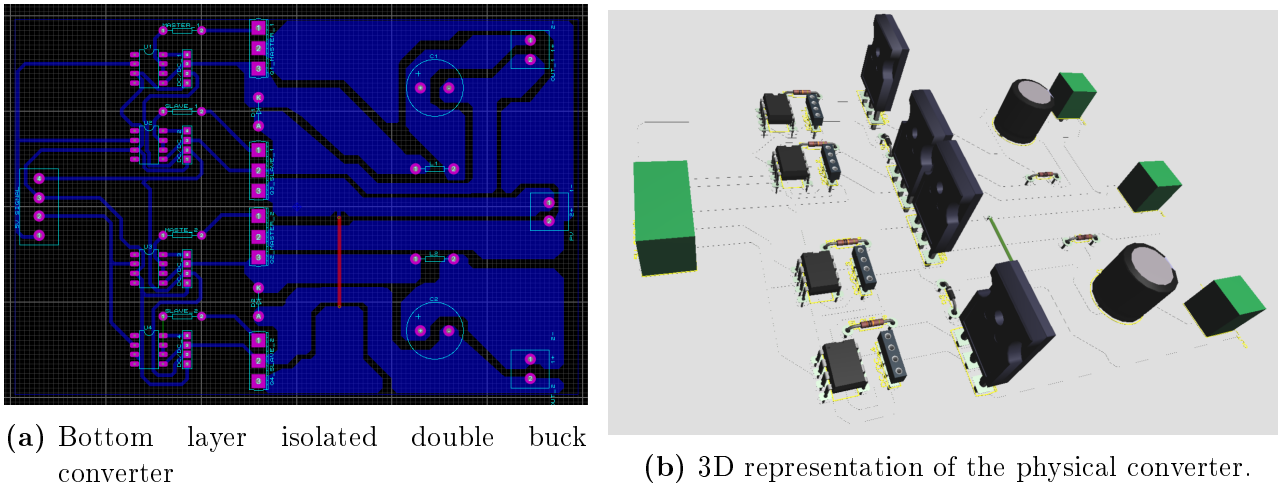


Figure B.1. Design of isolated double buck converter.

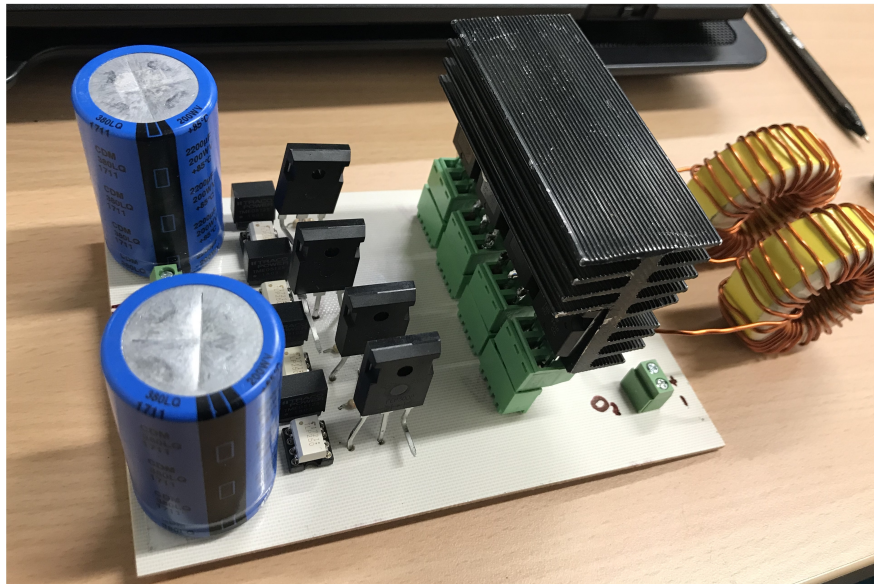


Figure B.2. Developed double DC/DC buck converter.

this measure a proper voltage and current rating for the IGBT's is assured. One of this interfaces is needed Each of this micro converters generate an isolated ground, that allow for the combination of the different switching states of the designed topologies.

B.1.2 Conception of the Isolated Double Boost Converter Board

The second DC/DC variant constructed to test the smart inverter is the double boost converter. The designed PCB bottom layer is presented in Fig. B.3 a), and in B.3 b) is

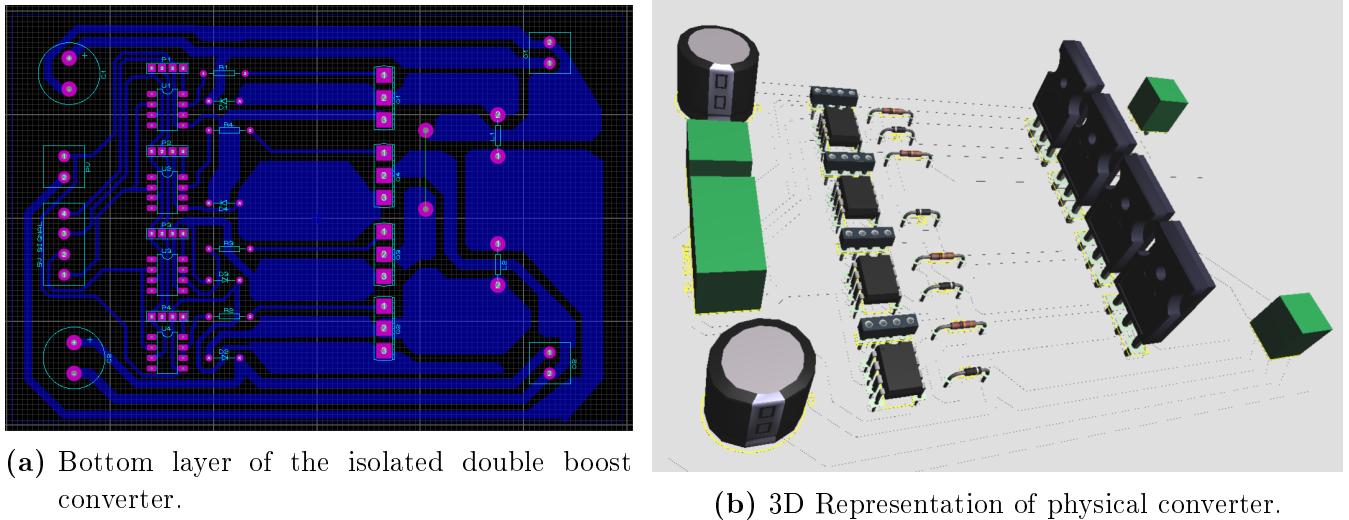


Figure B.3. Design of isolated double boost converter.

presented the 3D modernization of the converter. The same interface employed in section B.1.1 is used to control the IGBT's. After the realization of the DC/DC parts, was developed a PCB for the DC/AC stage, which consist of a conventional full bridge as presented in the next section.

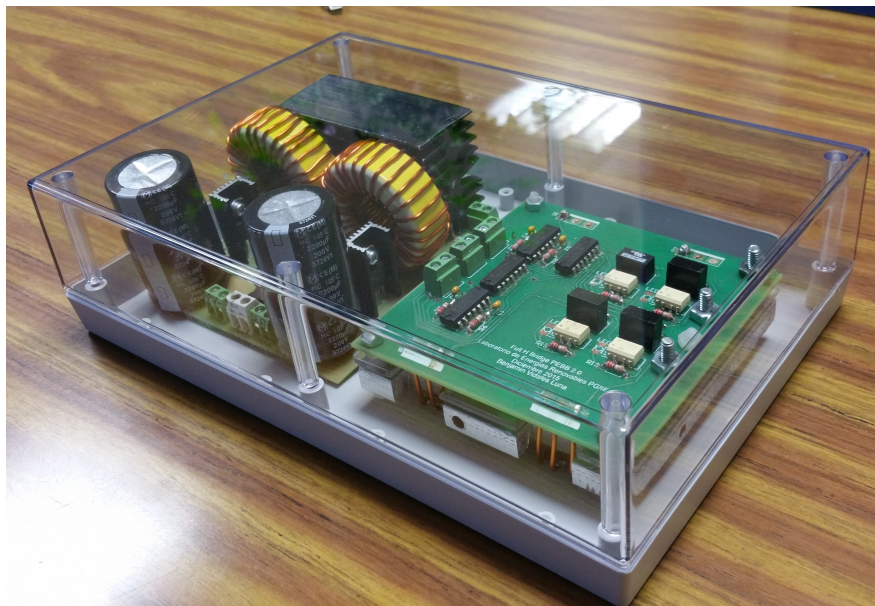
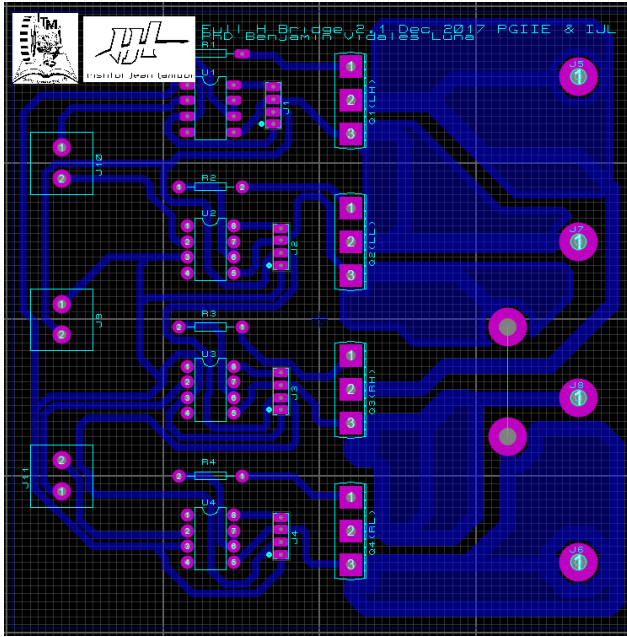
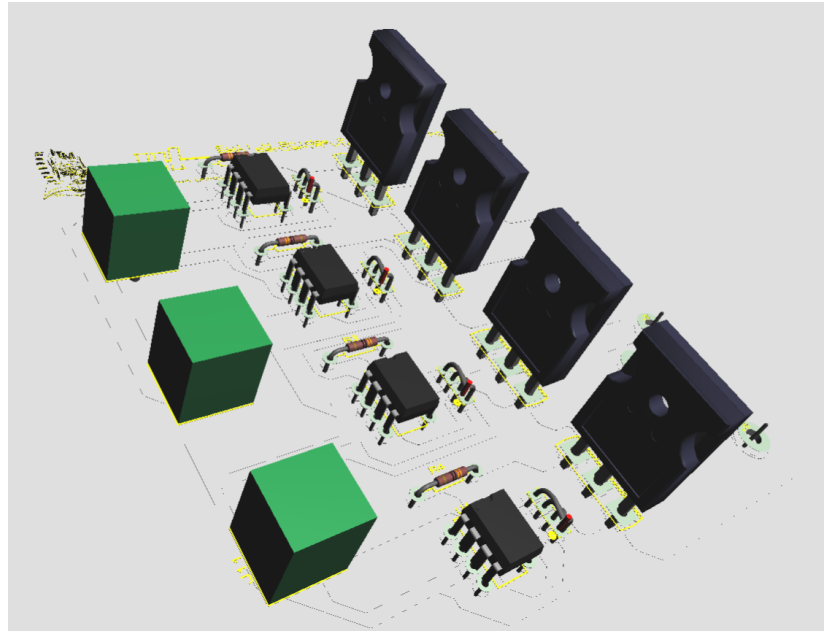


Figure B.5. Developed double DC/DC boost converter (left) and full H bridge (Right).



(a) Bottom layer of the full bridge PCB.



(b) 3D Representation of the physical bridge.

Figure B.4. PCB Design of the full bridge for the DC/AC stage.

B.1.3 Conception of Full H Bridge for DC/AC Stage Board

In order to complete the cascade cell multilevel topology employed for the smart inverter, the construction of a modular PCB was performed, following the design guidelines for control of IGBT's as presented in the precedent sections B.1.1 and B.1.2. The PCB design is presented in Fig. B.4 a), and the 3D model is presented in Fig. B.4 b).

With the designed PCB's, all the components needed to test the implementation of the smart Inverter are present, and the results will be described in the next section.

Appendix C

C.1 Fourier Series

Orthogonal series expansions play a key role in solving a wide range of problems encountered in physics and engineering. Fourier, Hartley, Walsh, etc., have used to approximately non linear characteristics with good results. They can also be used to solve differential equations, resorting only to algebraic means. Because of their very interesting characteristics an high efficiency as integration solvers, they have been researched widely in the fields of system identification, model reduction and control.

A basic understanding of the theory behind orthogonal series expansions is essential for learning the concepts of harmonic domain modeling. In this section the most relevant aspects of Fourier series are reviewed [111].

C.1.1 Periodic Functions

A periodic function $f(t)$ with frequency f_0 and period T_0 seconds is defined as

$$f(t) = f(t + T_0) \tag{C.1}$$

where $T_0 = 1/f_0$. The sine and cosine functions are examples of periodic functions.

C.1.2 Even and odd Functions

A Periodic function $f(t)$ is said to be *even* if the following relation holds true:

$$f(t) = f(-t) \quad (\text{C.2})$$

and it's said to be an *odd* function if

$$f(t) = -f(-t) \quad (\text{C.3})$$

An arbitrary function $f(t)$ can be represented as

$$f(t) = f_{\text{even}}(t) + f_{\text{odd}}(t) \quad (\text{C.4})$$

Where

$$f_{\text{even}}(t) = \frac{1}{2}f(t) + \frac{1}{2}f(-t) \quad (\text{C.5})$$

$$f_{\text{odd}}(t) = \frac{1}{2}f(t) - \frac{1}{2}f(-t) \quad (\text{C.6})$$

It's not difficult to see that $f_{\text{even}}(t)$ and $f_{\text{odd}}(t)$ are, respectively, even and odd functions. This means that any arbitrary function $f(t)$ can be represented as a sum of even and odd components. It should be mentioned that the function $\cos n\omega_0 t$ and $\sin n\omega_0 t$ are respectively, even and odd functions of time.

Half-wave Symmetry

A periodic Function $f(t)$ has half-wave symmetry if it satisfies the following property:

$$f(t) = -f\left(t + \frac{T_0}{2}\right) \quad (\text{C.7})$$

Given the nature of function with a half wave symmetry, the harmonic content of this signal will contain only even harmonics. This feature is used to develop the detection technique detailed in the next sections.

Quarter-wave Symmetry

If a periodic function $f(t)$ has half-wave symmetry and is an even function, then $f(t)$ is said to have even quarter symmetry.

If a periodic function $f(t)$ has half-wave symmetry and is an odd function, then $f(t)$ is said to have odd quarter-wave symmetry.

C.1.3 Trigonometrical Fourier Series

A periodic signal $f(t)$ of period T_0 can be expanded into a trigonometric Fourier series of the form

$$f(t) = \frac{1}{2}\alpha_0 + \sum_{n=1}^{\infty} (\alpha_n \cos n\omega_0 t + \beta_n \sin n\omega_0 t) \quad (\text{C.8})$$

Where $\omega_0 = \frac{2\pi}{T_0}$ and the coefficients of the series are given as

$$\alpha_0 = \frac{2}{T_0} \int_{-T_0/2}^{T_0/2} f(t) dt \quad (\text{C.9})$$

$$\alpha_n = \frac{2}{T_0} \int_{-T_0/2}^{T_0/2} f(t) \cos n\omega_0 t dt \quad (\text{C.10})$$

$$\beta_n = \frac{2}{T_0} \int_{-T_0/2}^{T_0/2} f(t) \sin n\omega_0 t dt \quad (\text{C.11})$$

Equation (C.8) can also be represented as

$$f(t) = A_0 + \sum_{n=1}^{\infty} (A_n \cos(n\omega_0 t + \theta_n)) \quad (\text{C.12})$$

Where

$$A_0 = \frac{1}{2} \alpha_0 \quad (\text{C.13})$$

$$A_n = \sqrt{\alpha_n^2 + \beta_n^2} \quad (\text{C.14})$$

$$\theta_n = \arctan - \frac{\beta_n}{\alpha_n} \quad (\text{C.15})$$

In electric circuit theory, the coefficient A_0 is referred to as the DC component, A_n and θ_n are the magnitude and angle of the n harmonic component.

Fig. C.1 shows the graphical representation of the Fourier series. This figure shows how a rectangular waveform can be regarded as the addition of sinusoidal waves of different frequencies, plus a constant term. It's usual to represent the set of sinusoidal waveforms as phasors of different harmonics frequencies, like those shown at the far end of Fig. C.1.

The property introduced by waveform symmetry in a Fourier series is summarized in Table

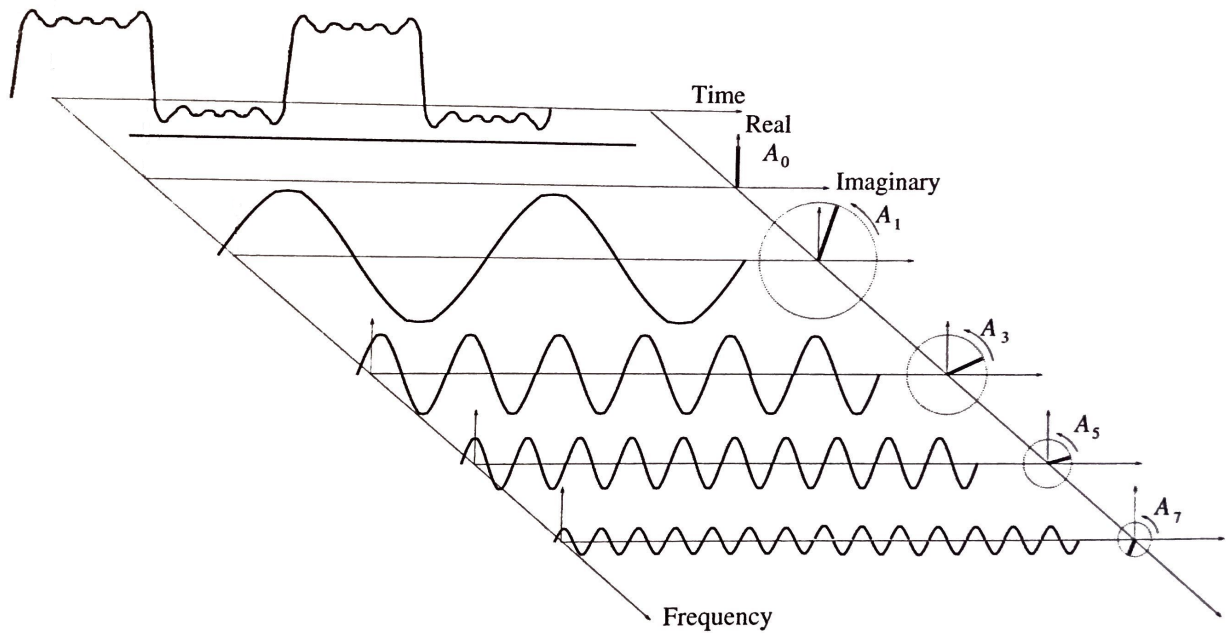


Figure C.1. Fourier representation of a square waveform as the sum of a series of sinusoidal waves.

C.1.1.

TABLE C.1.1. Waveform Symmetry Characteristics.

Waveform Symmetry	Definition	Fouriercoeff. Diff. from zero for $n = 1, 2, 3, \dots$	Fouriercoeff. equal to zero for $n = 1, 2, 3, \dots$
Even	$f(-t) = f(t)$	α_n	β_n
Odd	$f(-t) = -f(t)$	β_n	α_n
Half-Wave	$f(t) = -f(t + \frac{T_0}{2})$	α_{2n-1} β_{2n-1}	β_{2n-1} α_{2n-1}
Even Quarter-Wave	$f(-t) = f(t)$ and $f(t) = -f(t + \frac{T_0}{2})$	α_{2n-1}	α_{2n} β_n
Odd Quarter-Wave	$f(-t) = -f(t)$ and $f(t) = -f(t + \frac{T_0}{2})$	β_{2n-1}	β_{2n} α_n